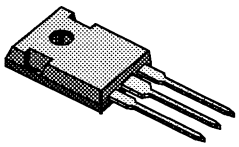
Siliconix incorporated

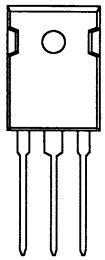
SMW12P20

P-Channel Enhancement Mode Transistor

TO-247 AD



TOP VIEW



1 GATE
2 DRAIN
3 SOURCE

1 2 3

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
-200	0.50	-12

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)[1]

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	12	A
	T_C = 100°C		7.5	
Pulsed Drain Current[2]		I_{DM}	48	
Avalanche Current (See Figure 9)		I_{AR}	12	
Repetitive Avalanche Energy[3]	L = 0.1 mH	E_{AR}	7.2	mJ
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS[1]

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		0.83	K/W
Junction-to-Ambient	R_{thJA}		40	
Case-to-Sink	R_{thCS}	0.35		

[1]Negative signs for current and voltage ratings have been omitted for the sake of clarity.
[2]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[3]Duty cycle ≤ 1%.

SMW12P20

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)
P-Channel Device – Negative Signs Have Been Omitted for Clarity

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		200		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V		12		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 7.5 A	0.28		0.50	Ω
		V_{GS} = 10 V, I_D = 7.5 A, T_J = 125°C	0.50		0.90	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 7.5 A	5	4.0		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1300			pF
Output Capacitance	C_{oss}		500			
Reverse Transfer Capacitance	C_{rss}		250			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 12 A	55		90	nC
Gate-Source Charge[2]	Q_{gs}		8		15	
Gate-Drain Charge[2]	Q_{gd}		30		50	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 100 V, R_L = 8.3 Ω, I_D ≃ 12 A, V_{GEN} = 10 V, R_G = 4.7 Ω	10		30	ns
Rise Time[2]	t_r		30		80	
Turn-Off Delay Time[2]	$t_{d(off)}$		35		80	
Fall Time[2]	t_f		16		60	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)						
Continuous Current	I_S				12	A
Pulsed Current[3]	I_{SM}				48	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.0	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	200			ns
Reverse Recovery Charge	Q_{rr}		1.0			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

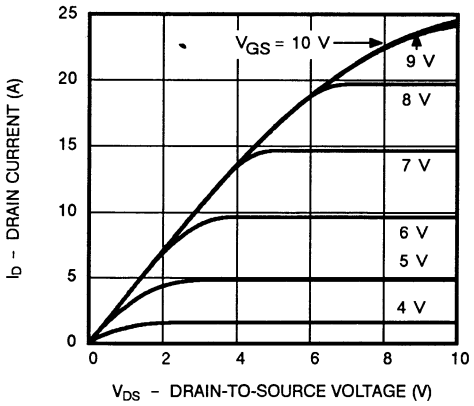


Figure 2. Transfer Characteristics

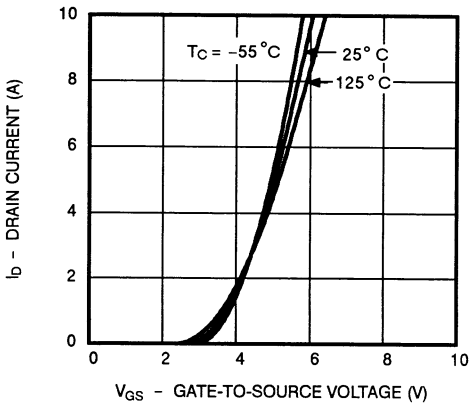


Figure 3. Transconductance

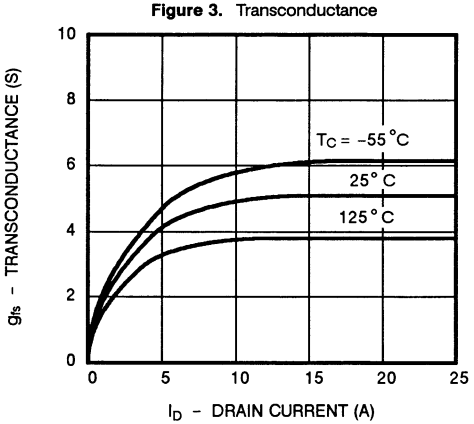


Figure 4. On-Resistance

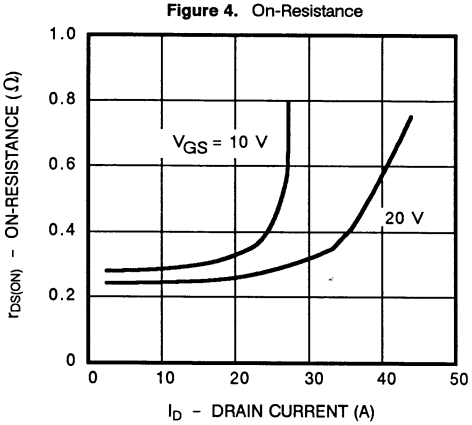


Figure 5. Capacitance

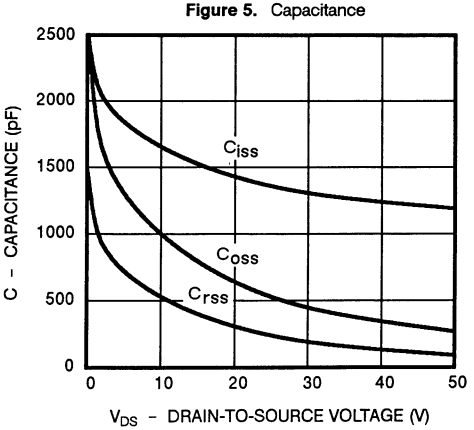
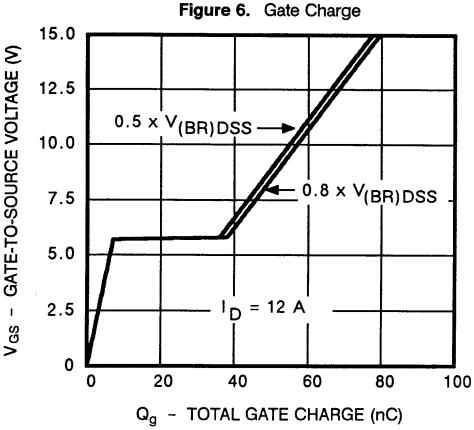


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

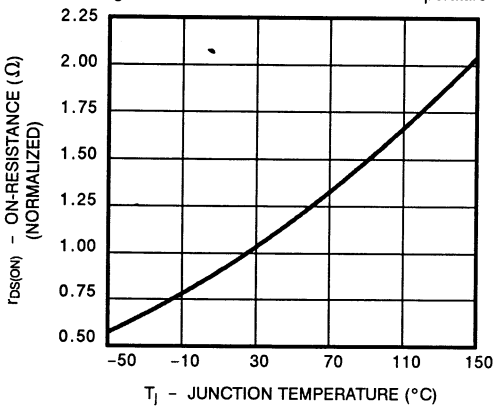
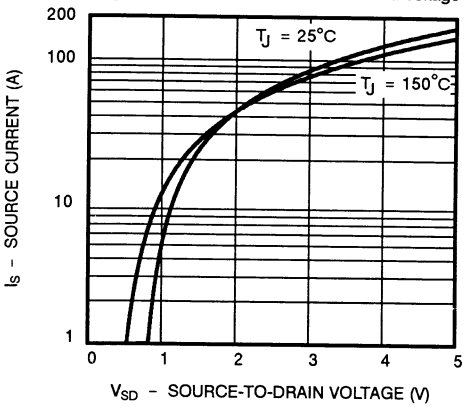


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

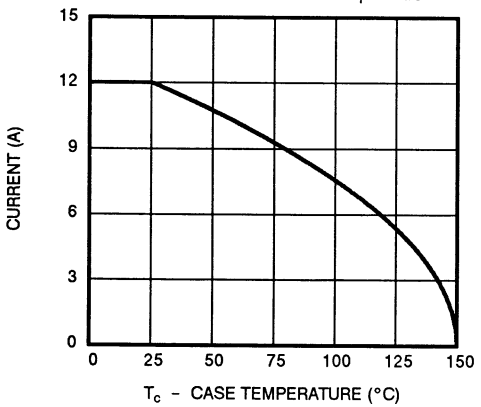
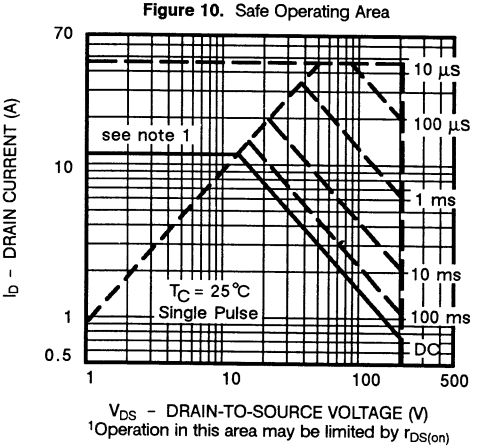
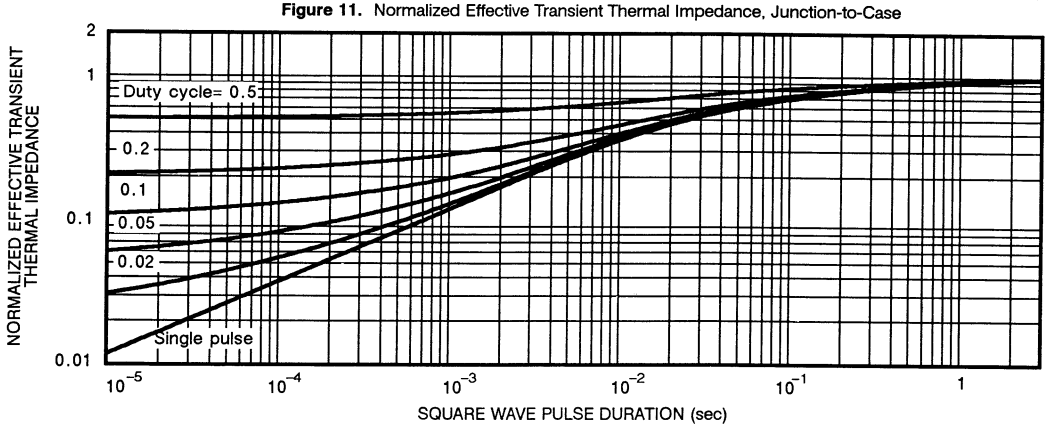


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case

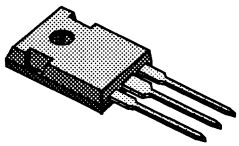


Siliconix incorporated

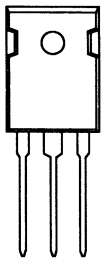
SMW14N50F

N-Channel Enhancement Mode Transistor
Fast Reverse Recovery

TO-247 AD



TOP VIEW



1 GATE
2 DRAIN
3 SOURCE

1 2 3

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	t_{rr} (ns)
500	0.4	14	250

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	14	A
	T_C = 100°C		8.8	
Pulsed Drain Current[1]		I_{DM}	56	
Avalanche Current (See Figure 9)		I_{AR}	14	
Repetitive Avalanche Energy[2]	L = 0.3 mH	E_{AR}	30	mJ
Power Dissipation	T_C = 25°C	P_D	180	W
	T_C = 100°C		75	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		0.70	K/W
Junction-to-Ambient	R_{thJA}		40	
Case-to-Sink	R_{thCS}	0.35		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[2]Duty cycle ≤ 1%.

SMW14N50F

Siliconix incorporated

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS		TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA			500		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1000 µA			2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V				250	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C				1000	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 10 V			14		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 7 A		0.32		0.40	Ω
		V_{GS} = 10 V, I_D = 7 A, T_J = 125°C		0.70		0.88	
Forward Transconductance[1]	g_{fs}	V_{DS} = 15 V, I_D = 7 A		6.2	5		S
DYNAMIC							
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		2500			pF
Output Capacitance	C_{oss}			460			
Reverse Transfer Capacitance	C_{rss}			140			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 14 A		73		130	nC
Gate-Source Charge[2]	Q_{gs}			15		22	
Gate-Drain Charge[2]	Q_{gd}			40		64	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 250 V, R_L = 17 Ω $I_D \simeq$ 14 A, V_{GEN} = 10 V, R_G = 4.7 Ω		16		27	ns
Rise Time[2]	t_r			44		66	
Turn-Off Delay Time[2]	$t_{d(off)}$			60		100	
Fall Time[2]	t_f			35		60	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)							
Continuous Current	I_S					14	A
Pulsed Current[3]	I_{SM}					56	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V				1.4	V
Reverse Recovery Time	t_{rr}	I_F = 14 A, dI_F/dt = 150 A/µs V_{DD} = 250 V	T_J = 25°C	205		250	ns
			T_J = 125°C	275		350	
Peak Reverse Recovery Current	$I_{RM(REC)}$		T_J = 25°C	13			A
			T_J = 125°C	18			
Reverse Recovery Charge	Q_{rr}		T_J = 25°C	1.4		2.2	µC
			T_J = 125°C	2.5		4.0	

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

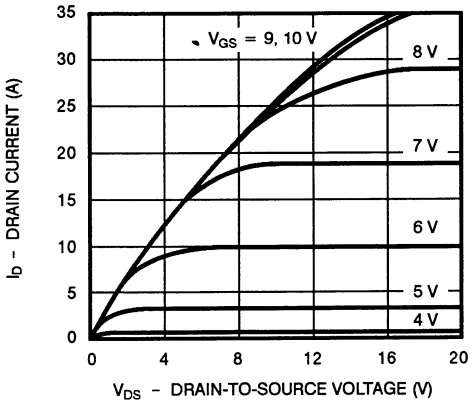


Figure 2. Transfer Characteristics

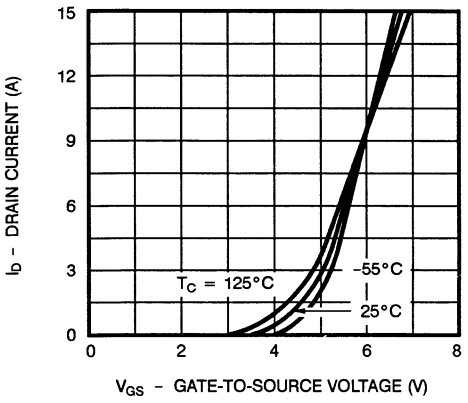


Figure 3. Transconductance

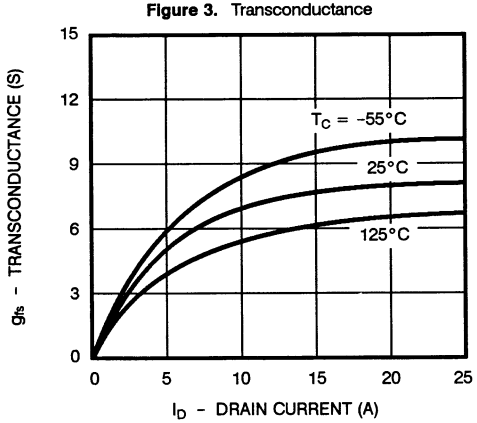


Figure 4. On-Resistance

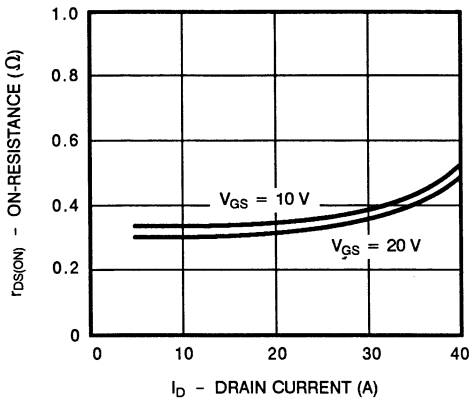


Figure 5. Capacitance

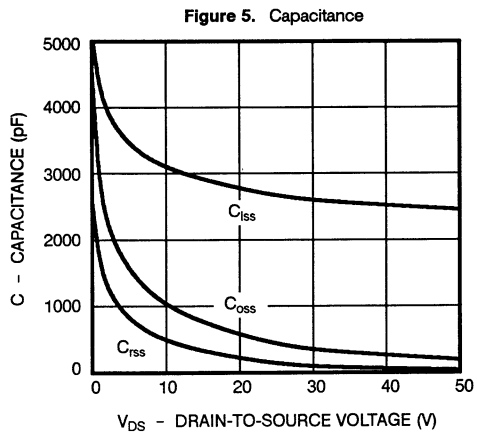
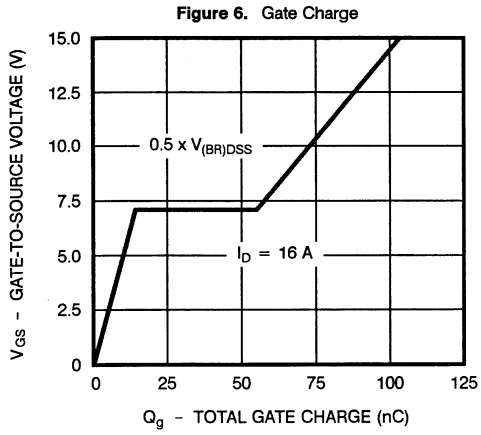


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

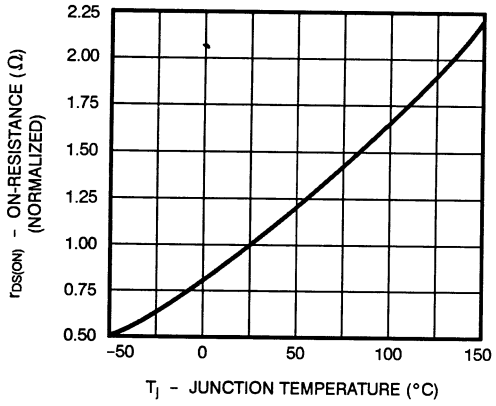
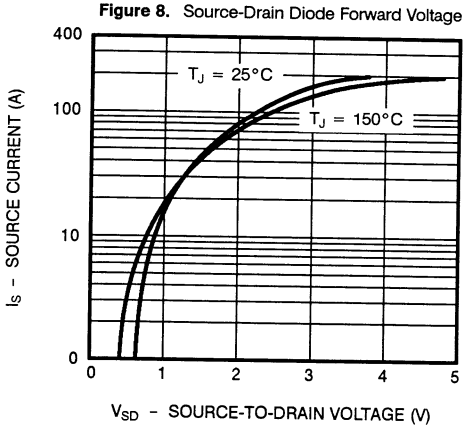


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

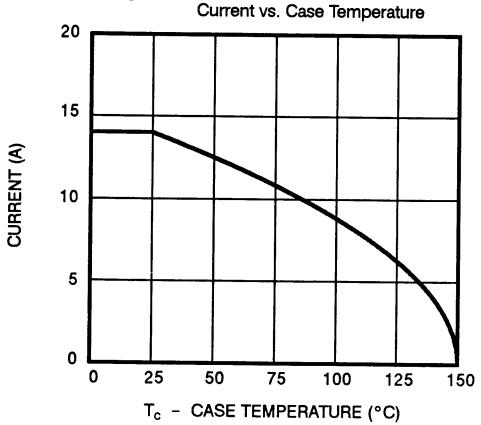


Figure 10. Safe Operating Area

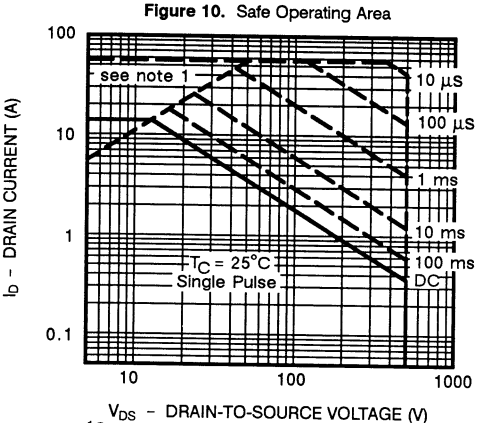
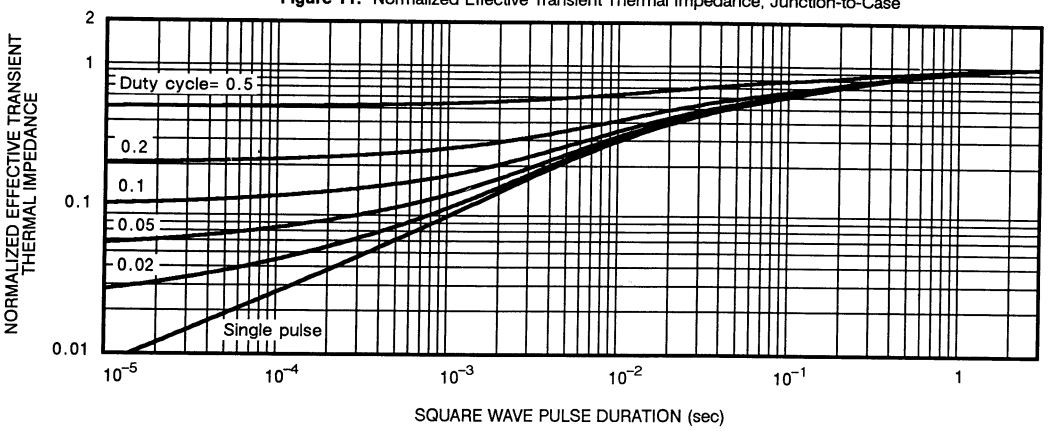


Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case



DIODE CHARACTERISTICS

Figure 12. Typical Reverse Recovery Time vs. di/dt

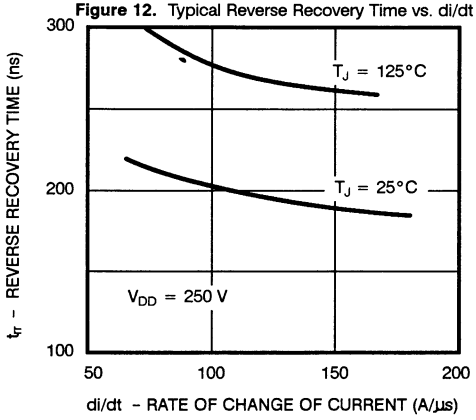


Figure 13. Typical Peak Reverse Recovery Current vs. di/dt

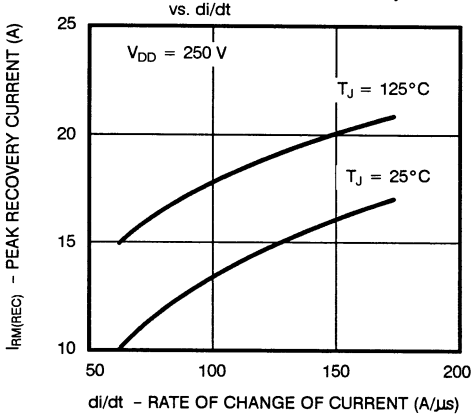


Figure 14. Commutating Safe Operating Area

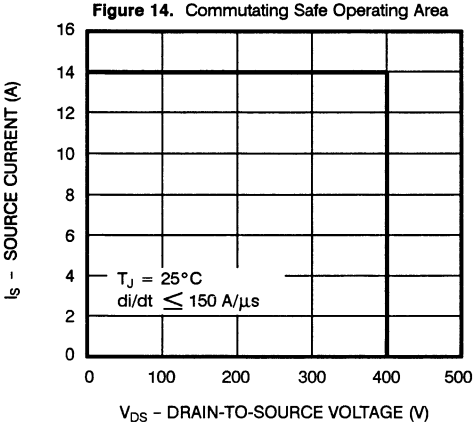


Figure 15. Typical dv/dt vs. di/dt

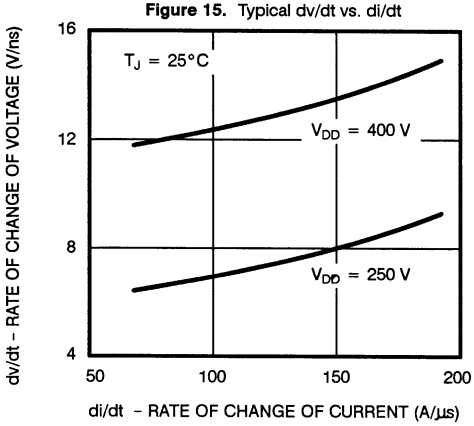
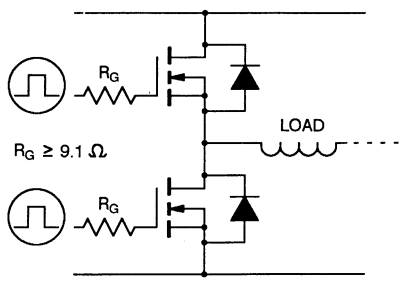
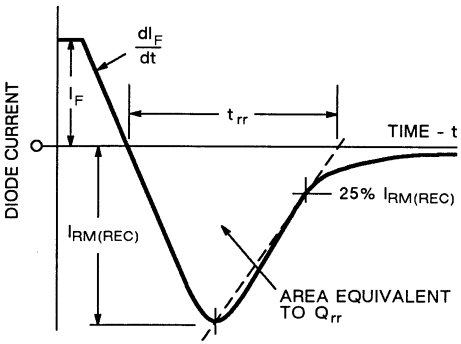


Figure 16. Minimum Value of Gate Resistor



Suggested Minimum Value of Gate Resistor to Operate within Commutating Safe Operating Area (See Figure 14).

Figure 17. Diode Reverse Recovery



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