Telmos

TMF120, TMF121
TMF122, TMF123

Monolithic Dual N-Channel Enhancement-Mode Lateral D-MOS FETs

Ordering Information

Differential Gate-Source Voltage	5mV	10mV	25mV	50mV
Differential Drift	25μV/°C	25μV/°C	25μV/°C	25μV/°C
TO-99 Hermetic Package	TMF120HD	TMF121HD	TMF122HD	TMF123HD
TO-99 Package with Shorting Ring	TMF120HD/R	TMF121HD/R	TMF122HD/R	TMF123HD/R
Sorted Chips in Waffle Pack	TMF120CHP	TMF121CHP	TMF122CHP	TMF123CHP

Note: Handle with care. Use all MOS handling precautions. Devices are extremely sensitive to ESD damage.

Features:

- **Self-Aligning Silicon Gate Structure**
- **Dielectrically Isolated Pair**
- **Low Interelectrode Capacitances**
- **Input (Gate) Leakage Current**
- **Independant of Operating Point**
- **Gate-Source Voltage Differential as low as 5.0mV**

Applications:

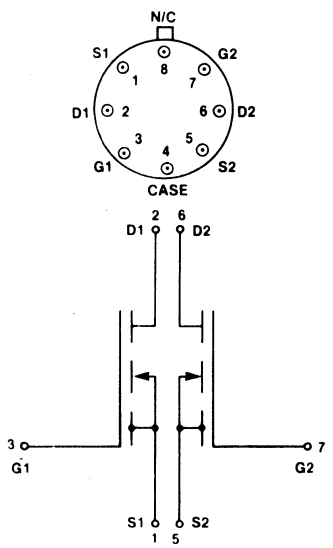
- **High-speed Analog Comparators**
- **Wide-band Differential Amplifiers**
- **Wide-band Source Followers**
- **Sample and Hold Circuits**
- **Undirectional Analog Switches**
- **Wide-band RF Amplifiers**
- **Cascade and Cascode Amplifers**

Absolute Maximum Ratings (T_A = +25°C each side unless otherwise noted)

V_{DS}	Drain-Source Voltage	+25 −0.5	Vdc
V_{DG}	Drain-Gate Voltage	+25 −0.5	Vdc
V_{GS}	Gate-Source Voltage	±25	Vdc
V_{GD}	Gate-Drain Voltage	±25	Vdc
I_D	Drain Current	50	mA
$V_{D_1D_2}$	$Drain_1$-to-$Drain_2$ Voltage	±40	Vdc

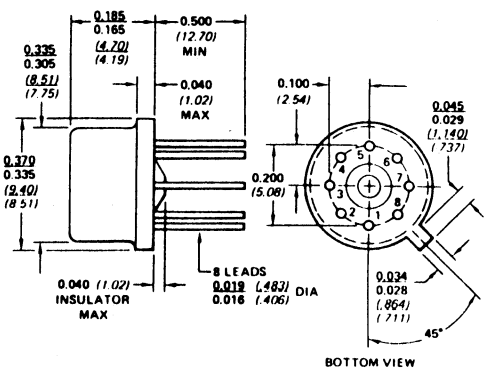
T_S	Storage Temperature Range	−65 to +150°C
T_j	Operating Junction Temperature Range	−55 to +125°C
P_D	Power Dissipation (one side) (Derate at 3.7 mW/°C)	367mW
P_D	Power Dissipation (two sides) (Derate at 5.0 mW/°C)	500 mW

in Configuration (Top View)



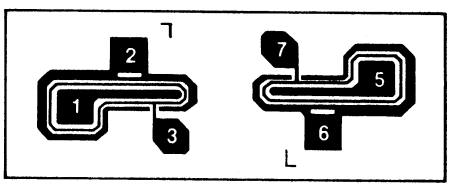
Package Dimensions

TO-99



All dimensions in inches and (millimeters)

Chip Configuration



Pad numbers correspond to Package Pin Assignment.

Body internally connected to source

Dimensions: .022 x .052 x .013 inches

DC Electrical Characteristics ($T_A = +25°C$)

Parameter		Min	Typ	Max	Units	Test Conditions
BV_{DS}	Drain-Source Breakdown Voltage	25	45		V	$I_D = 1.0\mu A$, $V_{GS} = 0$
I_{GSS}	Forward Gate Leakage Current		**	1.0	nA	$V_{GS} = 20V$, $V_{DS} = 0$
$V_{GS(th)}$	Gate-Source Threshold Voltage	0.5	0.9	1.5	V	$V_{DS} = V_{GS}$, $I_D = 1.0\mu A$
V_{GS}	Gate-Source ON Voltage	1.5	2.2	3.0		$V_{DS} = 10V$, $I_D = 5.0mA$
$I_{D(off)}$	OF Drain Current		2.0	100	nA	$V_{DS} = 20V$, $V_{GS} = 0$
$r_{DS(on)}$	Drain-Source ON Resistance		60	100	ohms	$I_D = 5.0mA$, $V_{GS} = 10V$

** Actual value is less than 1.0 pA.

AC Electrical Characteristics ($T_A = +25°C$)

Parameter		Min	Typ	Max	Units	Test Conditions	
g_{fs}	Common Source Forward Transconductance	7.0	10.5	14	mmhos	$V_{DS} = 10V$ $I_D = 5.0mA$	f = 1KHz
g_{os}	Common Source Output Conductance		13	100	μmhos		
c_{iss}	Common Source Input Capacitance		2.0	3.0	pF	$V_{DS} = 10V$ $V_{GS} = 0$	f = 1MHz
c_{rss}	Common Source Reverse Transfer Capacitance		0.4	0.7			
c_{oss}	Common Source Output Capacitance		1.5	2.5			
c_{DCASE}	Drain to Case Capacitance		1.8		pF	$V_{DCASE} = \pm 20V$, $V_{GS} = 0$ f = 1MHz	

Matching Characteristics ($T_A = +25°C$ unless otherwise specified)

Parameter			Min	Typ	Max	Units	Test Conditions	
$\lvert V_{GS1}-V_{GS2} \rvert$	Gate-Source Voltage Differential	TMF120			5.0	mV		
		TMF121			10			
		TMF122			25			
		TMF123			50			
$\frac{\Delta \lvert V_{GS1}-V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift			25		μV/°C	$V_{DS} = 10V$ $I_D = 5.0mA$	$T_A = -55$ to $+125°C$
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio Note 1		0.95	0.98	1.0			f = 1KHz
$I_{D_1D_2}$	Drain to Drain Leakage Current			1.0	100	pA	$V_{D_1D_2} = \pm 40V$ $V_{G_1S_1} = 0$, $V_{G_2S_2} = 0$	
$c_{D_1D_2}$	Drain to Drain Capacitance			0.9		pF	$V_{D_1D_2} = \pm 40V$, f = 1MHz $V_{G_1S_1} = 0$, $V_{G_2S_2} = 0$	

Note 1: The lower value is side 1.

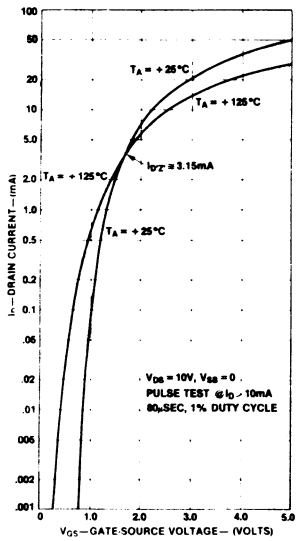
Typical Performance Characteristics

T_A = +25°C unless otherwise noted

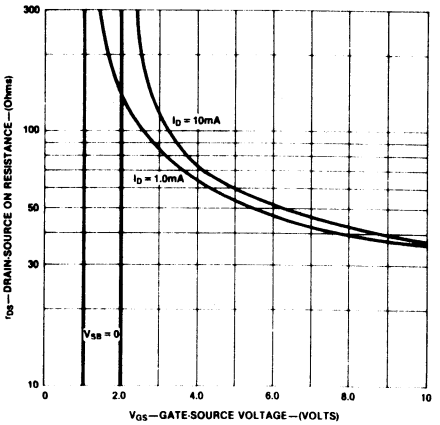
SD210-215, SD5000-5002, SD5100-5101, SD5200

"SD" CURVES

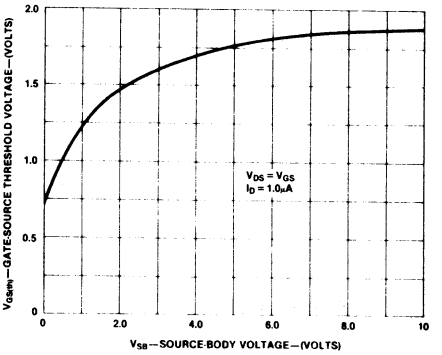
ON DRAIN CURRENT VS GATE-SOURCE VOLTAGE



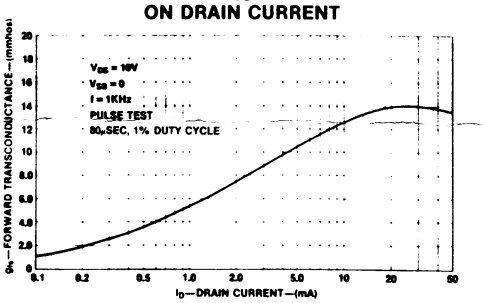
DRAIN-SOURCE ON RESISTANCE VS GATE-SOURCE VOLTAGE



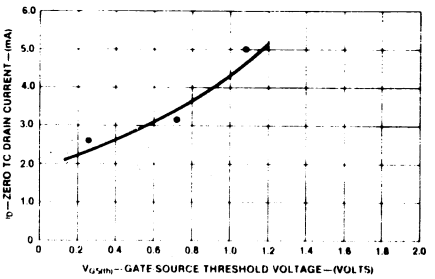
GATE-SOURCE THRESHOLD VOLTAGE VS SOURCE-BODY VOLTAGE



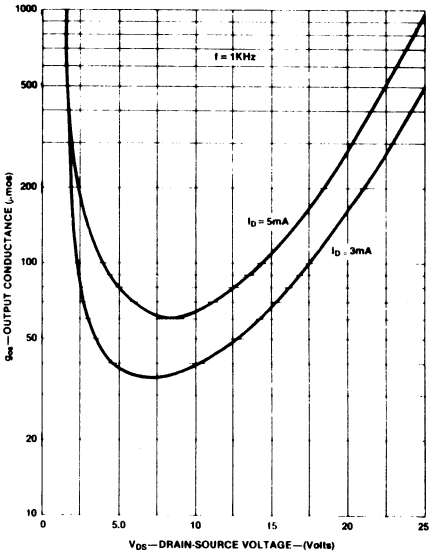
FORWARD TRANSCONDUCTANCE VS ON DRAIN CURRENT



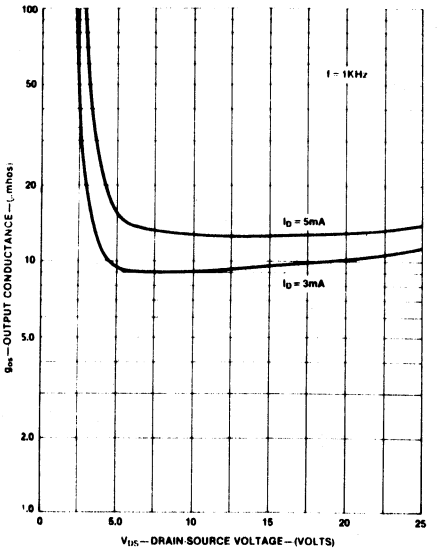
ZERO TEMPERATURE COEFFICIENT POINT OF DRAIN CURRENT VS GATE THRESHOLD VOLTAGE



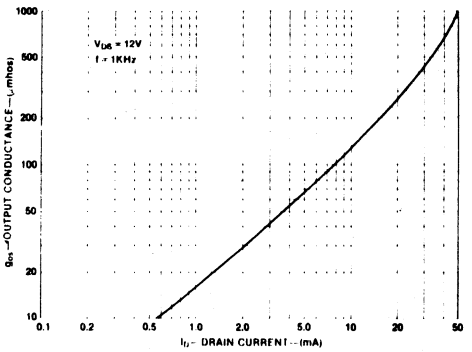
OUTPUT CONDUCTANCE VS DRAIN-SOURCE VOLTAGE



OUTPUT CONDUCTANCE VS DRAIN-SOURCE VOLTAGE



OUTPUT CONDUCTANCE VS DRAIN CURRENT



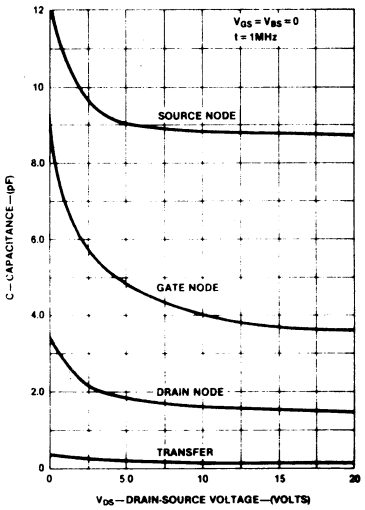
Typical Performance Characteristics

T_A = +25°C unless otherwise noted

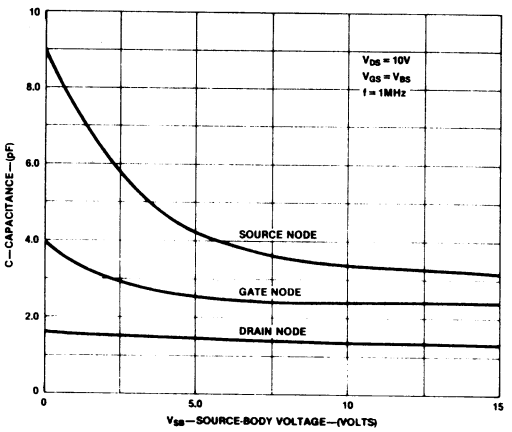
SD210-215, SD5000-5002, SD5100-5101, SD5200

"SD" CURVES

CAPACITANCES VS DRAIN-SOURCE VOLTAGE



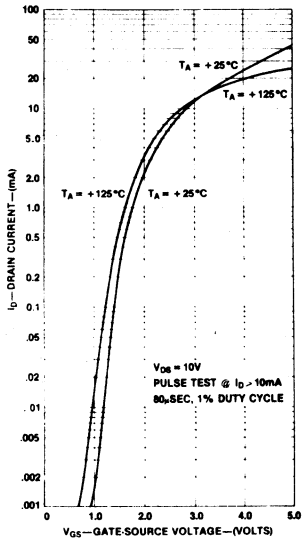
NODE CAPACITANCE VS SOURCE-BODY VOLTAGE



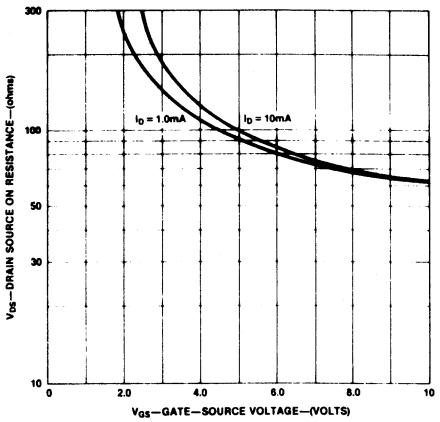
TMF120-123

"TMF" CURVES

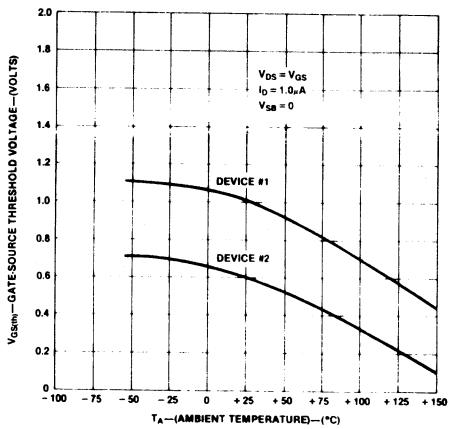
ON DRAIN CURRENT VS GATE-SOURCE VOLTAGE



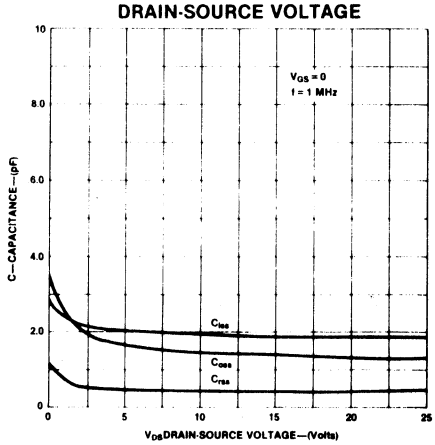
DRAIN-SOURCE ON RESISTANCE VS GATE-SOURCE VOLTAGE



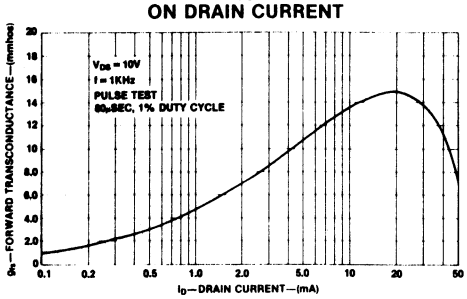
GATE-SOURCE THRESHOLD VOLTAGE VS AMBIENT TEMPERATURE



CAPACITANCES VS DRAIN-SOURCE VOLTAGE



FORWARD TRANSCONDUCTANCE VS ON DRAIN CURRENT



OUTPUT CONDUCTANCE VS DRAIN CURRENT