Siliconix incorporated

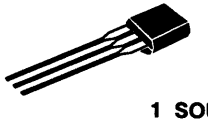
TN0201L, TN0401L
N-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

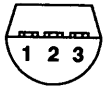
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
TN0201L	20	1.2	0.64
TN0401L	40	1.2	0.64

Performance Curves: VNDQ03

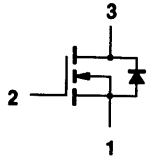
TO-92 (TO-226AA)



BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS TN0201L	LIMITS TN0401L	UNITS
Drain-Source Voltage		V_{DS}	20	40	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current	T_A = 25°C	I_D	±0.64	±0.64	A
	T_A = 100°C		±0.38	±0.38	
Pulsed Drain Current[1]		I_{DM}	±1.5	±1.5	
Maximum Power Dissipation	T_A = 25°C	P_D	0.8	0.8	W
	T_A = 100°C		0.32	0.32	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	156	K/W

[1]Pulse width limited by maximum junction temperature.

6

SPECIFICATIONS[a]				LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	TN0201L	40	20		V
			TN0401L	50	40		
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		1.7	0.5	2	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±10	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x rated $V_{(BR)DSS}$, V_{GS} = 0 V				1	µA
			T_J = 125°C			100	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V		0.8	0.25		A
		V_{DS} = 10 V, V_{GS} = 10 V		1.5	1.0		
Drain-Source On-Resitance[c]	$r_{DS(ON)}$	V_{GS} = 3.5 V, I_D = 50 mA		2.5		4	Ω
		V_{GS} = 4.5 V, I_D = 250 mA		1.4		2.0	
			T_J = 125°C	2.8		4.0	
		V_{GS} = 10 V, I_D = 1 A		0.85		1.2	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.5 A		500	200		mS
DYNAMIC							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		40		60	pF
Output Capacitance	C_{oss}			35		50	
Reverse Transfer Capacitance	C_{rss}			10		15	
SWITCHING							
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1 A, V_{GEN} = 10 V, R_G = 25 Ω		10		30	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)		15		30	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

Siliconix incorporated

TN0601L

N-Channel Enhancement-Mode MOS Transistor

PRODUCT SUMMARY

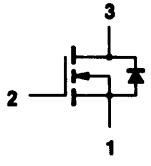
$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
60	1.8	0.47

Performance Curves: VNDQ06

TO-92 (TO-226AA)

BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_A = 25°C	I_D	0.47	A
	T_A = 100°C		0.29	
Pulsed Drain Current[1]		I_{DM}	1.5	
Maximum Power Dissipation	T_A = 25°C	P_D	0.80	W
	T_A = 100°C		0.32	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	156	K/W

[1]Pulse width limited by maximum junction temperature.

6

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, ID = 10 µA	70	60		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.7	0.5	2	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±10	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 48 V, V_{GS} = 0 V			1	µA
		T_J = 125°C			100	
On-State Drain Current [c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V	0.5	0.25		A
		V_{DS} = 10 V, V_{GS} = 10 V	1.5	1		
Drain-Source On-Resitance[c]	$r_{DS(ON)}$	V_{GS} = 4.5 V, I_D = 250 mA	2		3	Ω
		T_J = 125°C	4		6	
		V_{GS} = 3.5 V, I_D = 40 mA	4		5	
		V_{GS} = 10 V, I_D = 1 A	1.3		1.8	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 500 mA	350	200		mS
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	40		60	pF
Output Capacitance	C_{oss}		30		50	
Reverse Transfer Capacitance	C_{rss}		5		10	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 23 Ω, I_D = 1.0 A V_{GEN} = 10 V, R_G = 25 Ω	8		15	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	9		15	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

Siliconix incorporated

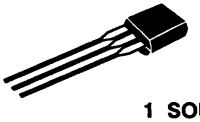
TN1206L
N-Channel Enhancement-Mode MOS Transistor

PRODUCT SUMMARY

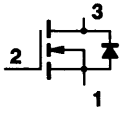
$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
120	6	0.18

Performance Curves: See VNDQ12

TO-92 (TO-226AA) BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	120	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_A = 25°C	I_D	±0.18	A
	T_A = 100°C		±0.11	
Pulsed Drain Current[1]		I_{DM}	±1	
Maximum Power Dissipation	T_A = 25°C	P_D	0.8	W
	T_A = 100°C		0.32	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	156	K/W

[1]Pulse width limited by maximum junction temperature.

TN1206L

Siliconix incorporated

SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, ID = 100 µA	145	120		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.4	0.5	2.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	±1		±10	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 96 V, V_{GS} = 0 V			10	µA
		T_J = 125°C			500	
On-State Drain Current [c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V	0.6	0.2		A
		V_{DS} = 10 V, V_{GS} = 10 V	0.8	0.5		
Drain-Source On-Resitance[c]	$r_{DS(ON)}$	V_{GS} = 3.5 V, I_D = 100 mA	4.5		8	Ω
		V_{GS} = 4.5 V, I_D = 2 mA	3.8		6	
		T_J = 125°C	7.6		12	
		V_{GS} = 10 V, I_D = 300 mA	3.3		6	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 200 mA	400	250		mS
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	35		50	pF
Output Capacitance	C_{oss}		15		25	
Reverse Transfer Capacitance	C_{rss}		2		5	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 60 V, R_L = 150 Ω, I_D = 0. 4 A V_{GEN} = 10 V, R_G = 25 Ω	8		15	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	10		20	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.