N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package	
				TO-92	DICE†
350V	22Ω	250mA	2.0V	TN0535N3	TN0535ND
400V	22Ω	250mA	2.0V	TN0540N3	TN0540ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Low threshold —2.0V max.
- ☐ High input impedance
- ☐ Low input capacitance — 48 pF typical
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Logic level interface – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line driver
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options (Note 1)

TO-92

Note 1: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-92	140mA	750mA	1.0W	170	125	140mA	750mA

* I_D (continuous) is limited by max rated T_j.

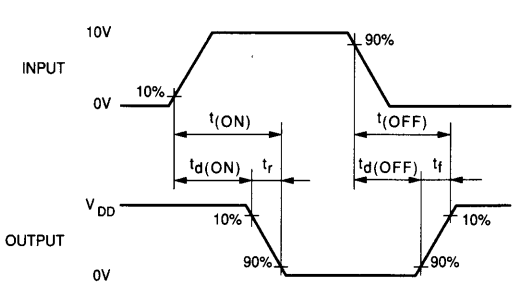
Electrical Characteristics (@ 25°C unless otherwise specified)

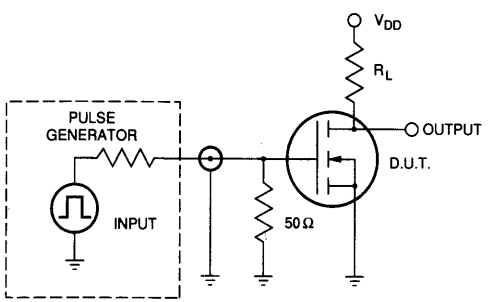
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN0540	400			V	V_{GS} = 0, I_D = 1mA
		TN0535	350				
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.0	V	V_{GS} = V_{DS}, I_D= 1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.5	-4.5	mV/°C	
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	V_{GS} = 0, V_{DS} = Max Rating
					500	µA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current			550		mA	V_{GS} = 5V, V_{DS} = 25V
			250	750			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			20	22	Ω	V_{GS} = 4.5V, I_D = 100mA
				19	22		V_{GS} = 10V, I_D = 150mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.9	1.5	%/°C	V_{GS} = 10V, I_D = 0.1A
G_{FS}	Forward Transconductance		125	200		m℧	V_{DS} = 25V, I_D = 0.1A
C_{ISS}	Input Capacitance			48	60	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			11	15		
C_{RSS}	Reverse Transfer Capacitance			3	8		
$t_{d(ON)}$	Turn-ON Delay Time			5	8	ns	V_{DD} = 25V, I_D = 150mA, R_S = 50Ω
t_r	Rise Time			5	8		
$t_{d(OFF)}$	Turn-OFF Delay Time			5	8		
t_f	Fall Time			5	8		
V_{SD}	Diode Forward Voltage Drop			0.8	1.2	V	V_{GS} = 0, I_{SD} = 150mA
t_{rr}	Reverse Recovery Time			400		ns	V_{GS} = 0, I_{SD} = 150mA

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300ms pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

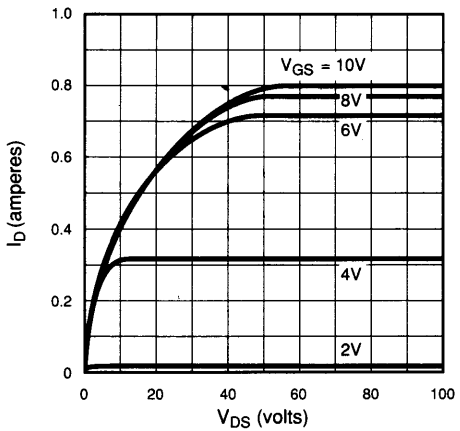
Switching Waveforms and Test Circuit



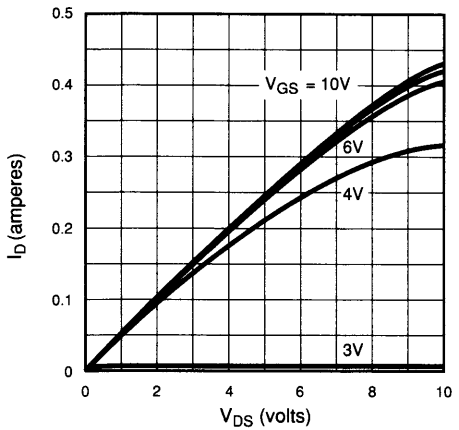


Typical Performance Curves

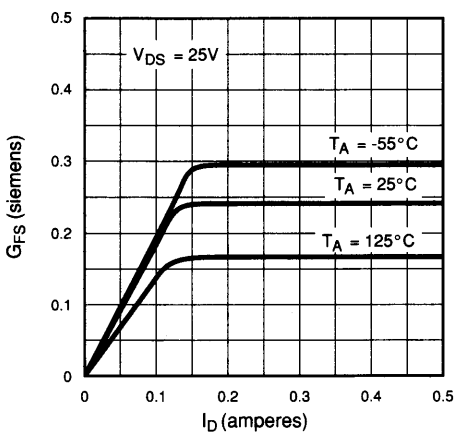
Output Characteristics



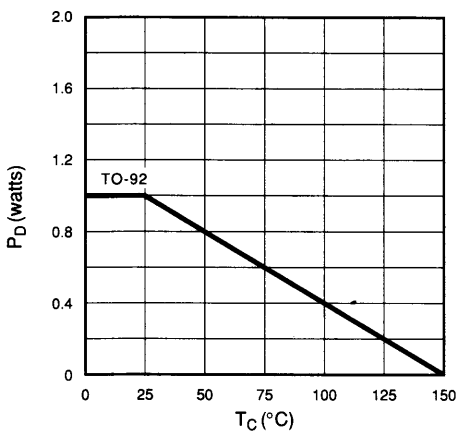
Saturation Characteristics



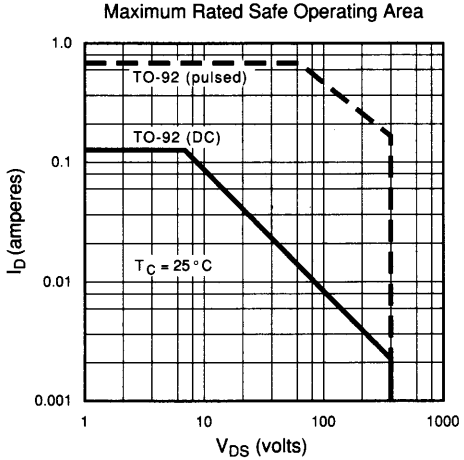
Transconductance vs. Drain Current



Power Dissipation vs. Case Temperature

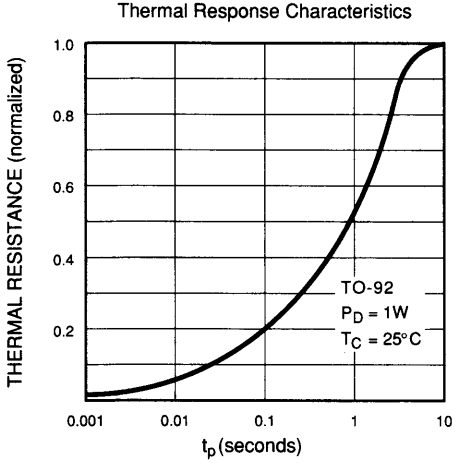


Maximum Rated Safe Operating Area

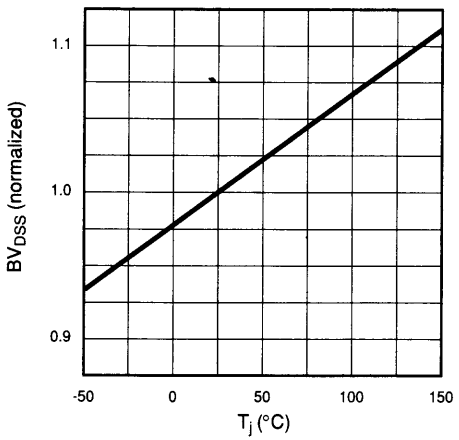


Pulsed Condition: 300µs, 2% dutycycle

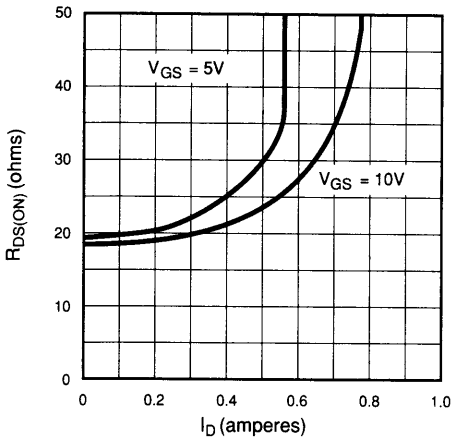
Thermal Response Characteristics



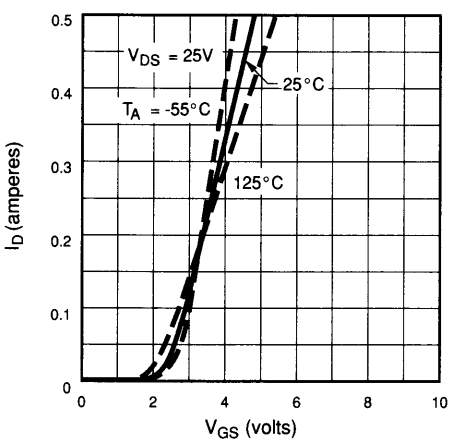
BV$_{DSS}$ Variation with Temperature



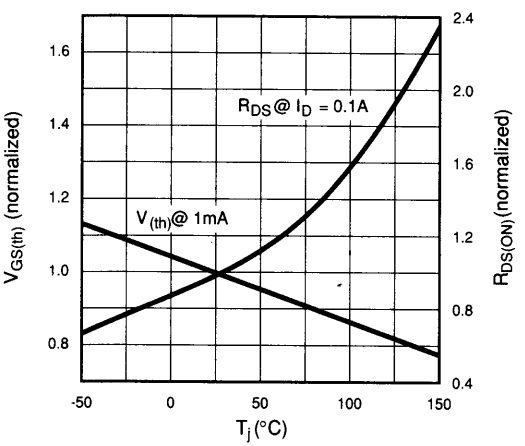
On-Resistance vs. Drain Current



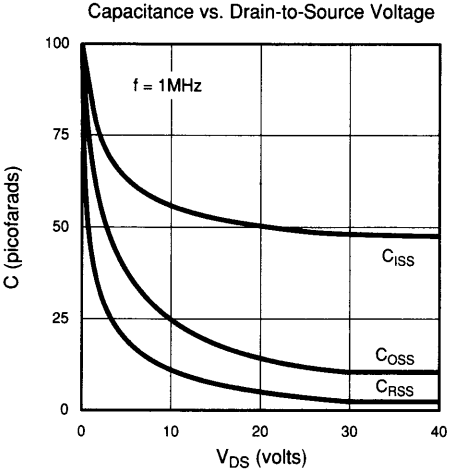
Transfer Characteristics



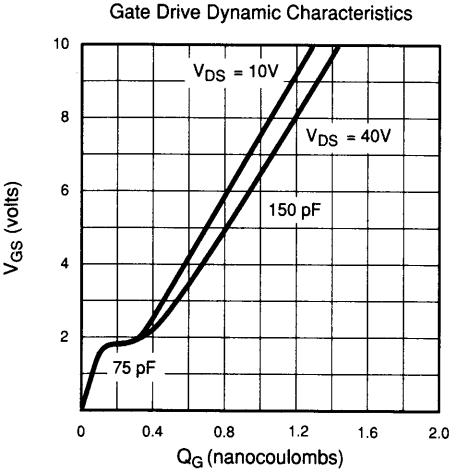
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package	
				TO-92	DICE†
350V	10Ω	1.0A	1.8V	TN0635N3	TN0635ND
400V	10Ω	1.0A	1.8V	TN0640N3	TN0640ND

† MIL visual screening available

Features

- ☐ Low threshold —1.8V max.
- ☐ High input impedance
- ☐ Low input capacitance — 85 pF typical
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Logic level interface – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line driver
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options (Note 1)

TO-92

Note 1: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-92	200mA	1.5A	1.0W	170	125	200mA	1.5A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

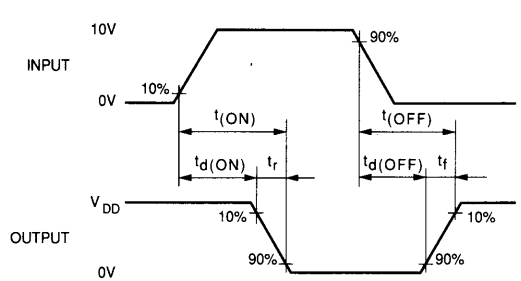
(Notes 1 and 2)

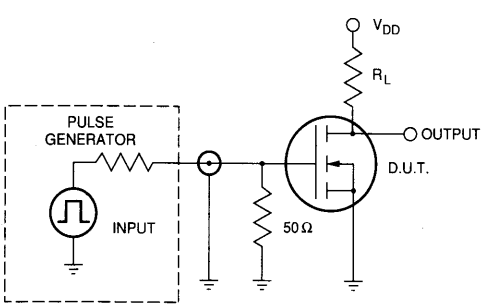
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN0640	400			V	V_{GS} = 0, I_D = 100µA
		TN0635	350				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.8	V	V_{GS} = V_{DS}, I_D= 1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-2.5	-4.0	mV/°C	V_{GS} = V_{DS}, I_D= 1mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				10		V_{GS} = 0, V_{DS} = Max Rating
					1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		0.3	1.5		mA	V_{GS} = 5V, V_{DS} = 25V
			1.0	1.8			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			8	10	Ω	V_{GS} = 4.5V, I_D = 150mA
				8	10		V_{GS} = 10V, I_D = 0.5A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				0.75	%/°C	V_{GS} = 10V, I_D = 500mA
G_{FS}	Forward Transconductance		125			m ℧	V_{DS} = 25V, I_D = 100mA
C_{ISS}	Input Capacitance			85	130	pF	V_{GS} = 0, V_{DS} = 25V f = 1 MHz
C_{OSS}	Common Source Output Capacitance			25	75		
C_{RSS}	Reverse Transfer Capacitance			10	20		
$t_{d(ON)}$	Turn-ON Delay Time				20	ns	V_{DD} = 25V, I_D =0.5A, R_S = 50Ω
t_r	Rise Time				15		
$t_{d(OFF)}$	Turn-OFF Delay Time				25		
t_f	Fall Time				20		
V_{SD}	Diode Forward Voltage Drop				1.8	V	V_{GS} = 0, I_{SD} = 200mA
t_{rr}	Reverse Recovery Time			300		ns	V_{GS} = 0, I_{SD} = 1.0A

Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300ms pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

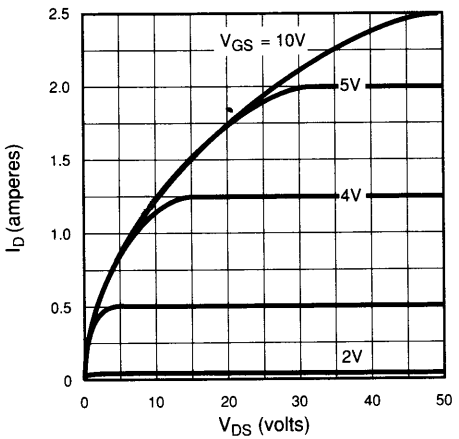
Switching Waveforms and Test Circuit



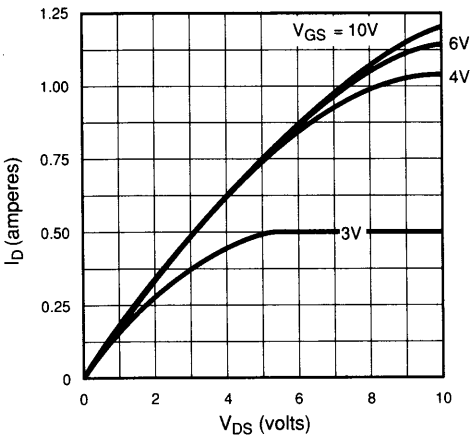


Typical Performance Curves

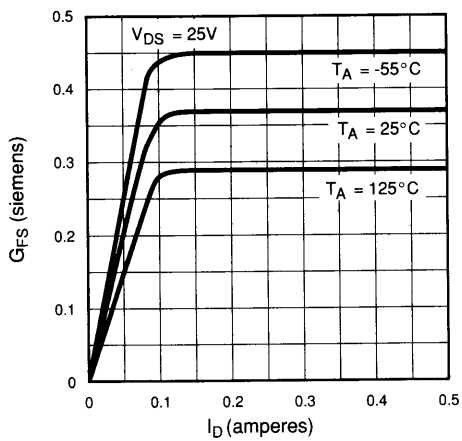
Output Characteristics



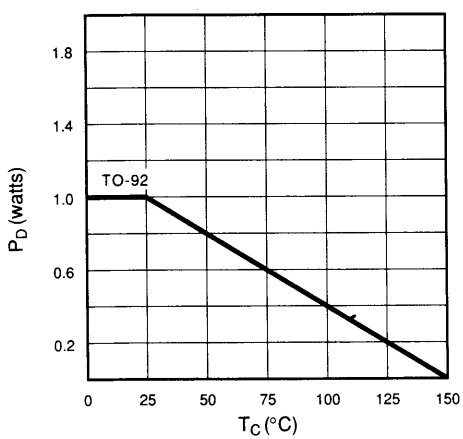
Saturation Characteristics



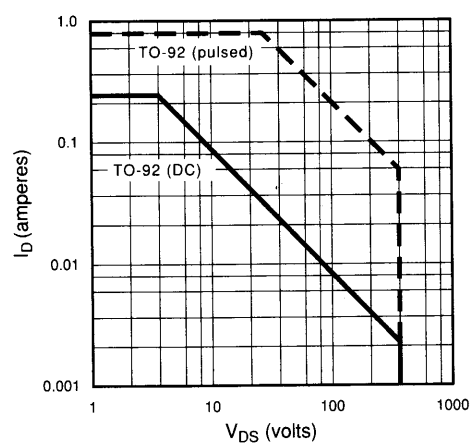
Transconductance vs. Drain Current



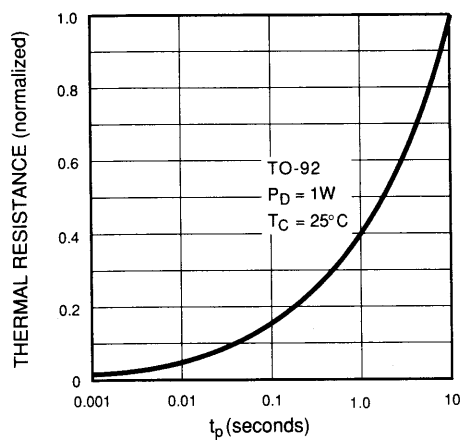
Power Dissipation vs. Case Temperature



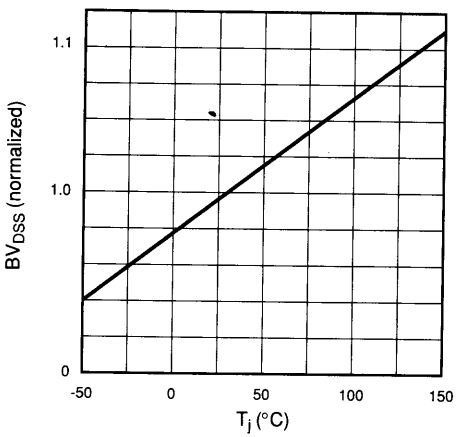
Maximum Rated Safe Operating Area



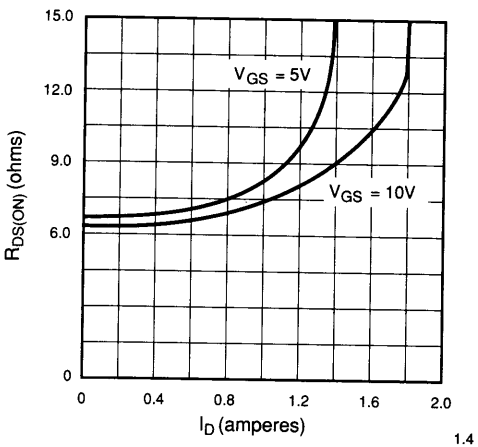
Thermal Response Characteristics



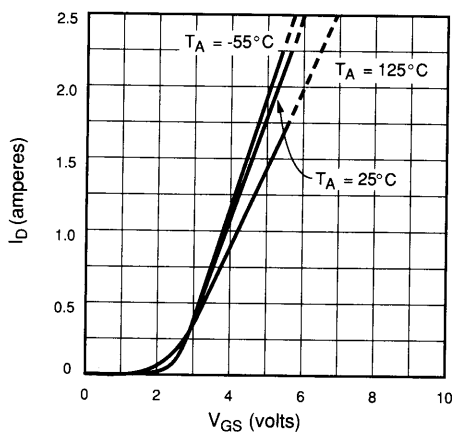
BV$_{DSS}$ Variation with Temperature



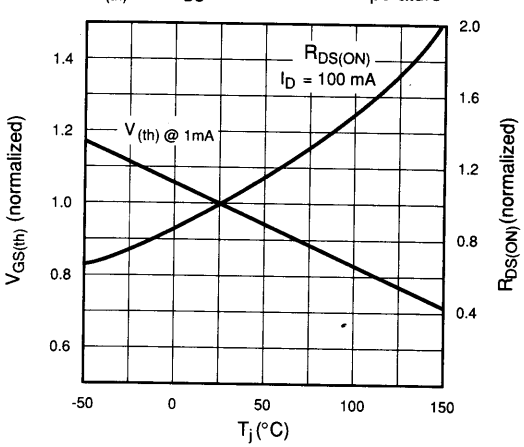
On-Resistance vs. I $_D$



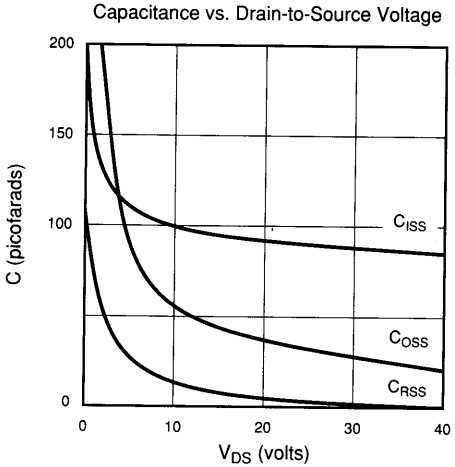
Transfer Characteristics



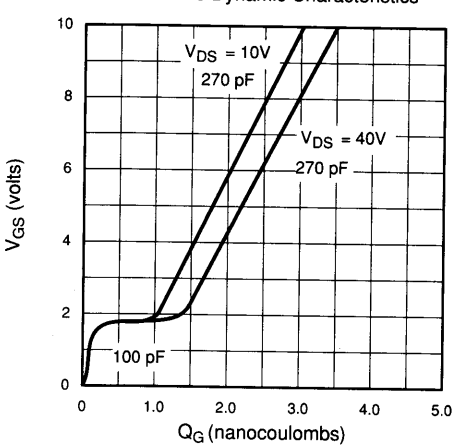
V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package	
				TO-92	DICE†
20V	1.3Ω	0.5A	1.0V	TN0702N3	TN0702ND

† MIL visual screening available

Features

- ☐ Low threshold — 1.0 max
- ☐ On resistance guaranteed at V_{GS} = 2, 3, and 5 volts
- ☐ High input impedance
- ☐ Low input capacitance —130 pF typical
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage

Applications

- ☐ Logic level interface
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line driver
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

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Package Options (Note 1)

TO-92

Note 1: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-92	0.6A	0.75A	1W	125	170	0.6A	0.75A

* I_D (continuous) is limited by max rated T_j.

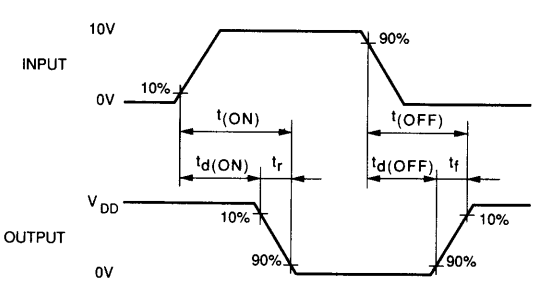
Electrical Characteristics (@ 25°C unless otherwise specified)

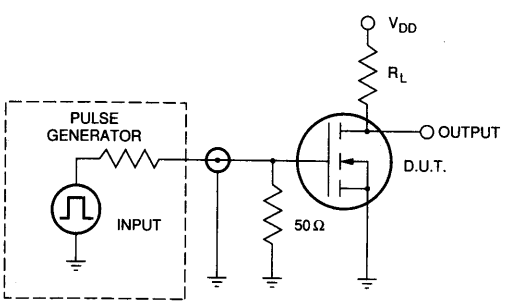
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	20			V	V_{GS} = 0, I_D = 1mA
$V_{GS(th)}$	Gate Threshold Voltage	0.5	0.8	1.0	V	V_{GS} = V_{DS}, I_D = 1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.0	mV/°C	V_{GS} = V_{DS}, I_D = 1.0mA
I_{GSS}	Gate Body Leakage			100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current			100	nA	V_{DS} = 20V, V_{GS} = 0V
				100	µA	V_{DS} = 0.8 Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	0.5	1.0		A	V_{GS} = V_{DS} = 5V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		4.0	5.0	Ω	V_{GS} = 2V, I_D = 50mA
			1.9	2.5		V_{GS} = 3V, I_D = 200mA
			1.0	1.3		V_{GS} = 5V, I_D =500mA
G_{FS}	Forward Transconductance	100			m℧	V_{DS} = 5V, I_D = 500mA
C_{ISS}	Input Capacitance		130	200	pF	V_{GS} = 0V, V_{DS} = 20V, f =1MHz
C_{OSS}	Common Source Output Capacitance		70	125		
C_{RSS}	Reverse Transfer Capacitance		30	60		
$t_{d(ON)}$	Turn-ON Delay Time			20	ns	V_{DD} = 20V, I_D = 0.5A, R_S = 50Ω
t_r	Rise Time			20		
$t_{d(OFF)}$	Turn-OFF Delay Time			30		
t_f	Fall Time			20		
V_{SD}	Diode Forward Voltage Drop			1.0	V	V_{GS} = 0V, I_{SD} = 0.5A

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwide stated. (Pulse test: 300 µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
				TO-243AA*	DICE†
20V	1.0Ω	1.6V	4.0A	—	TN2502ND
40V	1.0Ω	1.6V	4.0A	TN2504N8	TN2504ND

* Same as SOT-89.
† MIL visual screening available.

Features

- ☐ Low threshold — 1.6V max.
- ☐ High input impedance
- ☐ Low input capacitance — 125 pF max.
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Logic level interface – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line driver
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

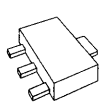
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options (Note 1)



TO-243AA
(SOT-89)

Note 1: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-243AA	0.6A	4.0A	0.55W†	227†	—	0.6A	4.0A

* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 board, 25mm x 19mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

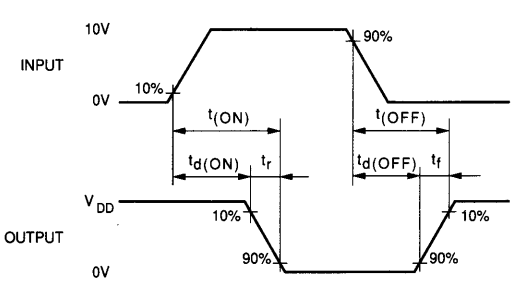
Electrical Characteristics (@ 25°C unless otherwise specified)

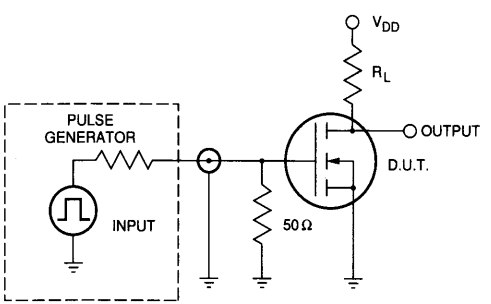
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN2504	40			V	V_{GS} = 0, I_D = 2mA
		TN2502	20				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.6	V	V_{GS} = V_{DS}, I_D= 1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.8	-4.5	mV/°C	V_{GS} = V_{DS}, I_D= 2.5mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	V_{GS} = 0, V_{DS} = Max Rating
					1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		1.0	2.1		A	V_{GS} = 5V, V_{DS} = 15V
			4.0	7.0			V_{GS} = 10V, V_{DS} = 15V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			0.8	1.5	Ω	V_{GS} = 5V, I_D = 750mA
				0.7	1.0		V_{GS} = 10V, I_D = 1.5A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				0.75	%/°C	V_{GS} = 10V, I_D = 2.0A
G_{FS}	Forward Transconductance		0.5	1.0		℧	V_{DS} = 15V, I_D = 2.0A
C_{ISS}	Input Capacitance				125	pF	V_{GS} = 0, V_{DS} = 15V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance				70		
C_{RSS}	Reverse Transfer Capacitance				25		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	V_{DD} = 15V, I_D = 500mA, R_S = 50Ω
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				25		
t_f	Fall Time				13		
V_{SD}	Diode Forward Voltage Drop			1.2	1.8	V	V_{GS} = 0, I_{SD} = 1.5A
t_{rr}	Reverse Recovery Time			300		ns	V_{GS} = 0, I_{SD} = 1A

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300ms pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





Preliminary

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
				TO-243AA*	DICE†
60V	1.5Ω	1.6V	3.0A	—	TN2506ND
100V	1.5Ω	1.6V	3.0A	TN2510N8	TN2510ND

* Same as SOT-89.
† MIL visual screening available.

Features

- ☐ Low threshold —1.6V max.
- ☐ High input impedance
- ☐ Low input capacitance — 125 pF max.
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Logic level interface – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line driver
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

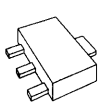
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options (Note 1)



TO-243AA
(SOT-89)

Note 1: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-243AA	0.42A	3.0A	0.55W†	227†	—	0.42A	3.0A

* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 board, 25mm x 19mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

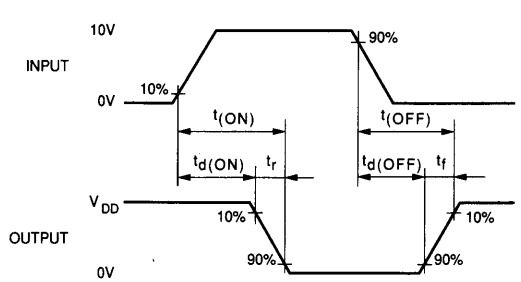
Electrical Characteristics (@ 25°C unless otherwise specified)

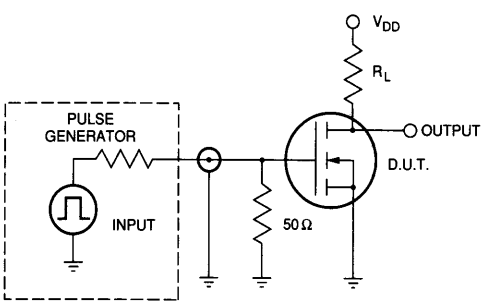
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN2510	100			V	V_{GS} = 0, I_D = 2mA
		TN2506	60				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.6	V	V_{GS} = V_{DS}, I_D= 1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				-4.5	mV/°C	V_{GS} = V_{DS}, I_D= 1.0mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	V_{GS} = 0, V_{DS} = Max Rating
					1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		1.2	2.0		A	V_{GS} = 5V, V_{DS} = 25V
			3.0	6.0			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			1.5	2.0	Ω	V_{GS} = 5V, I_D = 750mA
				1.0	1.5		V_{GS} = 10V, I_D = 750mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				0.75	%/°C	V_{GS} = 10V, I_D = 0.5A
G_{FS}	Forward Transconductance		0.4	0.6		℧	V_{DS} = 25V, I_D = 1.0A
C_{ISS}	Input Capacitance				125	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance				70		
C_{RSS}	Reverse Transfer Capacitance				25		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	V_{DD} = 25V, I_D = 1.5A, R_S = 50Ω
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				10		
V_{SD}	Diode Forward Voltage Drop				1.8	V	V_{GS} = 0, I_{SD} = 1.5A
t_{rr}	Reverse Recovery Time			300		ns	V_{GS} = 0, I_{SD} = 1.5A

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300ms pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
				TO-243AA*	DICE
200V	6Ω	2.0V	1.0A	—	TN2520ND
240V	6Ω	2.0V	1.0A	TN2524N8	TN2524ND

* Same as SOT-89.

Features

- ☐ Low threshold — 2.0V max.
- ☐ High input impedance
- ☐ Low input capacitance — 125 pF max.
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Logic level interface – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line driver
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

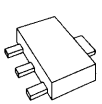
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options (Note 1)



TO-243AA
(SOT-89)

Note 1: See package outline section for decrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-243AA	0.2A	1.8A	0.55W†	227†	—	0.2A	1.8A

* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 board, 25mm x 19mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

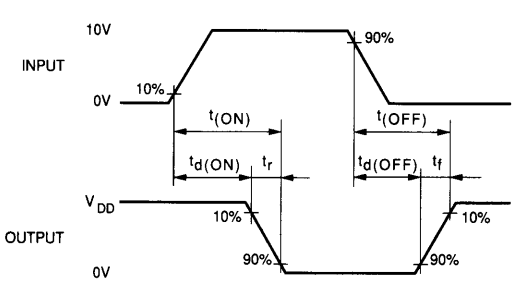
Electrical Characteristics (@ 25°C unless otherwise specified)

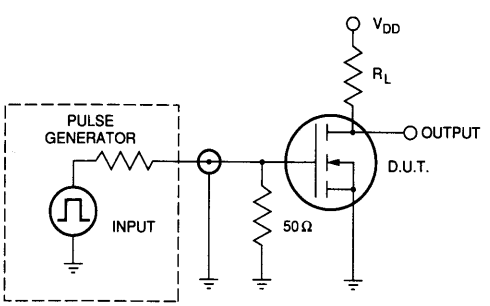
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN2524	240			V	V_{GS} = 0, I_D = 2mA
		TN2520	200				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		2.0	V	V_{GS} = V_{DS}, I_D= 1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				-5.0	mV/°C	V_{GS} = V_{DS}, I_D= 1mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	V_{GS} = 0, V_{DS} = Max Rating
					1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		0.5			A	V_{GS} = 4.5V, V_{DS} = 25V
			1.0				V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			4	6	Ω	V_{GS} = 4.5V, I_D = 250mA
				4	6		V_{GS} = 10V, I_D = 0.5A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				1.4	%/°C	V_{GS} = 10V, I_D = 0.5A
G_{FS}	Forward Transconductance		300			m℧	V_{DS} = 25V, I_D = 0.5A
C_{ISS}	Input Capacitance				125	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance				70		
C_{RSS}	Reverse Transfer Capacitance				25		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	V_{DD} = 25V, I_D = 1.0A, R_S = 50Ω
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				20		
V_{SD}	Diode Forward Voltage Drop				1.8	V	V_{GS} = 0, I_{SD} = 1.0A
t_{rr}	Reverse Recovery Time			300		ns	V_{GS} = 0, I_{SD} = 1.0A

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300ms pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
				TO-243AA*	DICE†
350V	12Ω	1.8V	1.0A	—	TN2535ND
400V	12Ω	1.8V	1.0A	TN2540N8	TN2540ND

* Same as SOT-89.
† MIL visual screening available.

Features

- ☐ Low threshold — 1.8V max.
- ☐ High input impedance
- ☐ Low input capacitance — 125 pF max.
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Logic level interface – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line driver
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

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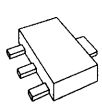
Package Options (Note 1)



TO-243AA
(SOT-89)

Note 1: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-243AA	165mA	1.0A	0.55W†	227†	—	165mA	1.0A

* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 board, 25mm x 19mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

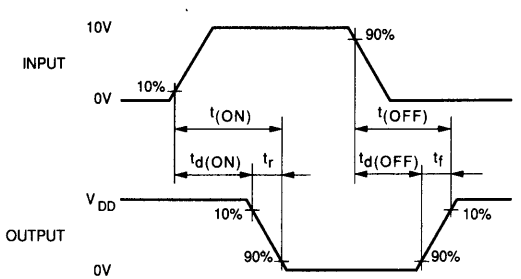
Electrical Characteristics (@ 25°C unless otherwise specified)

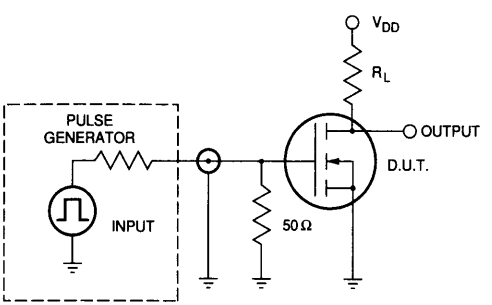
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TN2540	400			V	V_{GS} = 0, I_D = 100µA
		TN2535	350				
$V_{GS(th)}$	Gate Threshold Voltage		0.6		1.8	V	V_{GS} = V_{DS}, I_D= 1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-2.5	-4.0	mV/°C	V_{GS} = V_{DS}, I_D= 1mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				10	µA	V_{GS} = 0, V_{DS} = Max Rating
					1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		0.3	1.5		A	V_{GS} = 4.5V, V_{DS} = 25V
			1.0	1.8			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			8	12	Ω	V_{GS} = 4.5V, I_D = 150mA
				8	12		V_{GS} = 10V, I_D = 0.5A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				0.75	%/°C	V_{GS} = 10V, I_D = 500mA
G_{FS}	Forward Transconductance		125			m℧	V_{DS} = 25V, I_D = 100mA
C_{ISS}	Input Capacitance				125	pF	V_{GS} = 0, V_{DS} = 25V f = 1 MHz
C_{OSS}	Common Source Output Capacitance				70		
C_{RSS}	Reverse Transfer Capacitance				25		
$t_{d(ON)}$	Turn-ON Delay Time				20	ns	V_{DD} = 25V, I_D = 500mA, R_S = 50Ω
t_r	Rise Time				15		
$t_{d(OFF)}$	Turn-OFF Delay Time				25		
t_f	Fall Time				20		
V_{SD}	Diode Forward Voltage Drop				1.8	V	V_{GS} = 0, I_{SD} = 200mA
t_{rr}	Reverse Recovery Time			300		ns	V_{GS} = 0, I_{SD} = 1A

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300ms pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

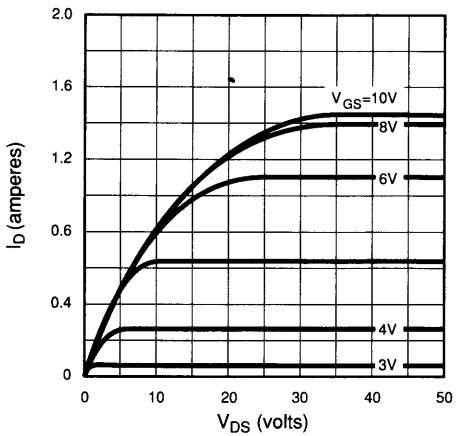
Switching Waveforms and Test Circuit



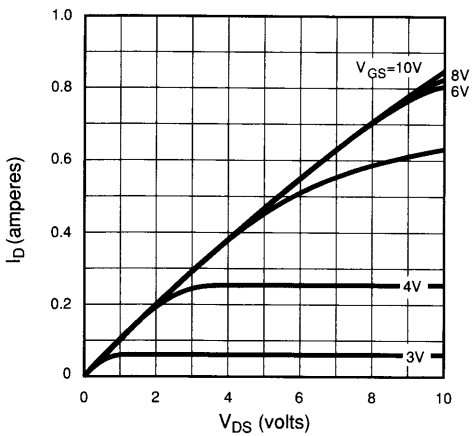


Typical Performance Curves

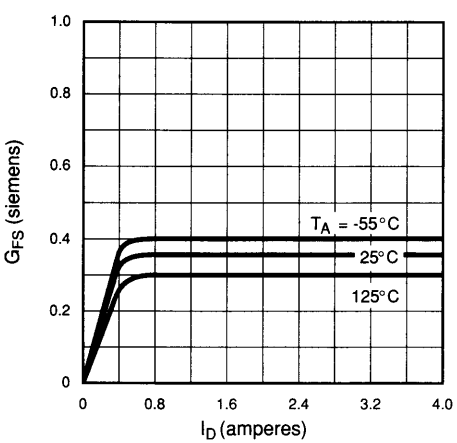
Output Characteristics



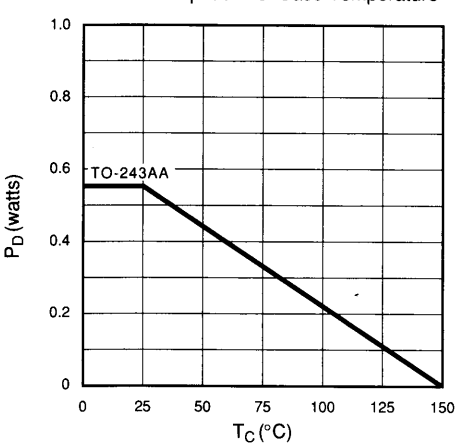
Saturation Characteristics



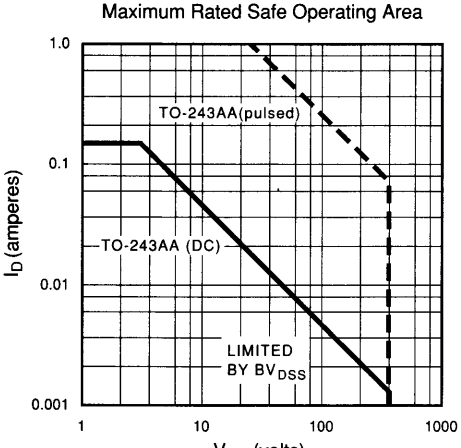
Transconductance vs. Drain Current



Power Dissipation vs. Case Temperature

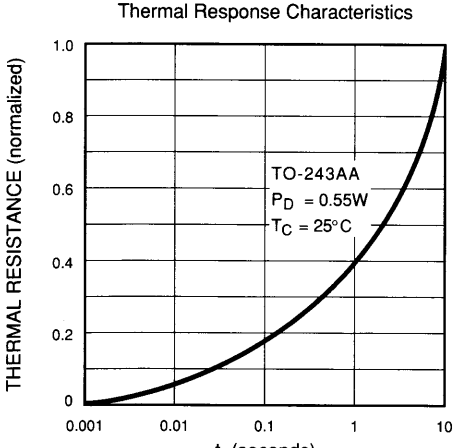


Maximum Rated Safe Operating Area

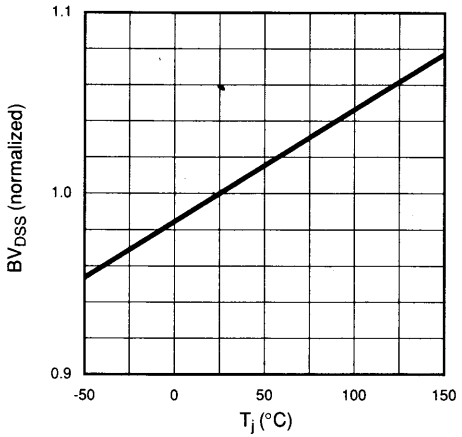


Pulsed Condition: 300 µs; 20% Duty Cycle

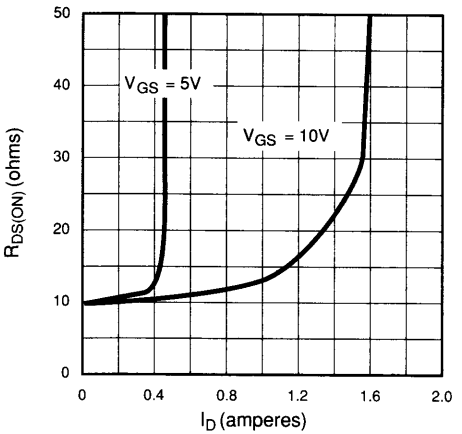
Thermal Response Characteristics



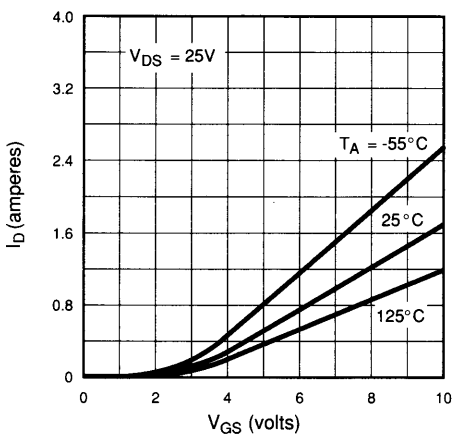
BV$_{DSS}$ Variation with Temperature



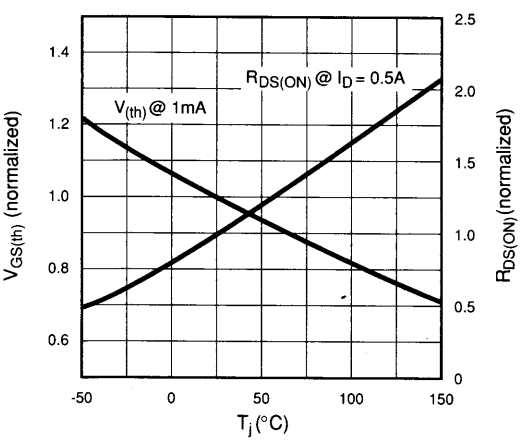
On-Resistance vs. Drain Current



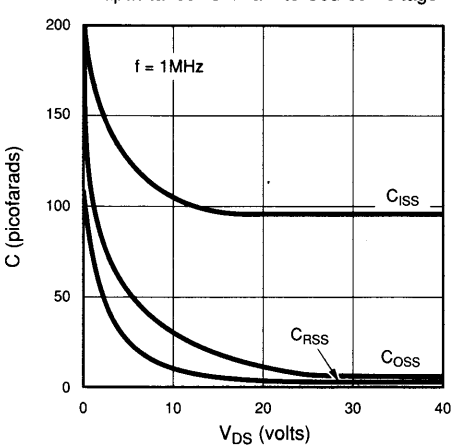
Transfer Characteristics



V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics