Siliconix incorporated

TN2010L, TN2410L
N-Channel Enhancement-Mode MOS Transistors

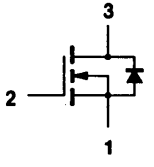
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
TN2010L	200	10	0.18
TN2410L	240	10	0.18

Performance Curves: VNDB24

TO-92 (TO-226AA) BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS TN2010L	LIMITS TN2410L	UNITS
Drain-Source Voltage		V_{DS}	200	240	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current	T_A = 25°C	I_D	±0.18	±0.18	A
	T_A = 100°C		±0.11	±0.11	
Pulsed Drain Current[1]		I_{DM}	±1	±1	
Maximum Power Dissipation	T_A = 25°C	P_D	0.8	0.8	W
	T_A = 100°C		0.32	0.32	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	156	K/W

[1]Pulse width limited by maximum junction temperature.

6

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SPECIFICATIONS[a]				LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 100 µA	TN2410L	260	240		V
			TN2010L	240	200		
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA		1.4	0.5	1.8	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V		±1		±10	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x rated $V_{(BR)DSS}$, V_{GS} = 0 V		0.01		1	µA
			T_J = 125°C	1.0		100	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V		0.8	0.25		A
Drain-Source On-Resitance[c]	$r_{DS(ON)}$	V_{GS} = 3.5 V, I_D = 50 mA		6		15	Ω
		V_{GS} = 4.5 V, I_D = 200 mA		5		10	
			T_J = 125°C	10		20	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 0.2 A		500	100		mS
DYNAMIC							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		110		135	pF
Output Capacitance	C_{oss}			30		50	
Reverse Transfer Capacitance	C_{rss}			5		20	
SWITCHING							
Turn-On Time	t_{ON}	V_{DD} = 60 V, R_L = 150 Ω, I_D = 0. 4 A V_{GEN} = 10 V, R_G = 25 Ω		15		35	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)		30		60	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

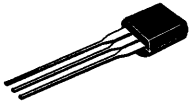
Siliconix incorporated

TN2460 SERIES
N-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

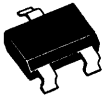
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (mA)	PACKAGE
TN2460L	240	60	76	TO-92
TN2460T	240	60	51	SOT-23

TO-92 (TO-226AA)

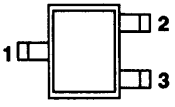


BOTTOM VIEW

SOT-23

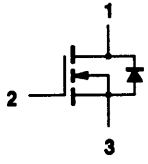


BOTTOM VIEW



Performance Curves: VNDN24

PRODUCT MARKING	
TN2460T	TO3



1 DRAIN
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS TN2460L	LIMITS TN2460T	UNITS
Drain-Source Voltage		V_{DS}	240	240	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current[1]	T_A = 25°C	I_D	±76	±51	mA
	T_A = 100°C		±48	±32	
Pulsed Drain Current[1]		I_{DM}	±0.8	±0.40	
Power Dissipation	T_A = 25°C	P_D	0.80	0.36	W
	T_A = 100°C		0.32	0.14	
Operating Junction Temperature		T_J	-55 to 150		°C
Storage Temperature		T_{stg}	-55 to 150		
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS TN2460L	LIMITS TN2460T	UNITS
Junction-to-Ambient	R_{thJA}	156	350	K/W

[1]Pulse width limited by maximum junction temperature

6

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SPECIFICATIONS[a]			LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D = 10 µA, V_{GS} = 0 V	260	240		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1.40	0.5	1.8	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±10	nA
		T_J = 125°C	±5			
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 120 V, V_{GS} = 0 V			0.1	µA
		T_J = 125°C			5.0	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V	140	20		mA
		V_{DS} = 10 V, V_{GS} = 10 V	170	75		
Drain-Source On-Resistance[c]	$r_{DS(ON)}$	V_{GS} = 4.5 V, I_D = 20 mA	55		60	Ω
		T_J = 125°C	110		120	
		V_{GS} = 10 V, I_D = 50 mA			60	
Forward Transconductance[c]	g_{FS}	V_{DS} = 10 V, I_D = 50 mA		30		mS
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	15		30	pF
Output Capacitance	C_{oss}		4		15	
Reverse Transfer Capacitance	C_{rss}		1		10	
SWITCHING						
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 500 Ω, I_D = 50 mA V_{GEN} = 10 V, R_G = 25 Ω	10		20	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)	20		35	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 80 µsec, Duty Cycle ≤ 1%.

Siliconix incorporated

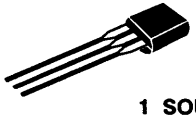
TN3512L, TN4012L
N-Channel Enhancement-Mode MOS Transistors

PRODUCT SUMMARY

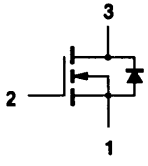
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
TN3512L	350	12	0.16
TN4012L	400	12	0.16

Performance Curves: VNDV40

TO-92 (TO-226AA) BOTTOM VIEW



1 SOURCE
2 GATE
3 DRAIN



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS TN3512L	LIMITS TN4012L	UNITS
Drain-Source Voltage		V_{DS}	350	400	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current	T_A = 25°C	I_D	±0.16	±0.16	A
	T_A = 100°C		±0.10	±0.10	
Pulsed Drain Current[1]		I_{DM}	±0.65	±0.65	
Maximum Power Dissipation	T_A = 25°C	P_D	0.80	0.80	W
	T_A = 100°C		0.32	0.32	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	156	K/W

[1]Pulse width limited by maximum junction temperature.

6

Siliconix incorporated

SPECIFICATIONS[a]				LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 µA	TN4012L	420	400		V
			TN3512L	400	350		
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA		1.3	0.6	1.8	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V		±1		±10	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x rated $V_{(BR)DSS}$, V_{GS} = 0 V				1	µA
			T_J = 125°C			100	
On-State Drain Current [c]	$I_{D(ON)}$	V_{DS} = 10 V, V_{GS} = 4.5 V		300	150		mA
Drain-Source On-Resitance[c]	$r_{DS(ON)}$	V_{GS} = 3.5 V, I_D = 50 mA		10		15	Ω
		V_{GS} = 4.5 V, I_D = 150 mA		9		12	
			T_J = 125°C	17		30	
Forward Transconductance[c]	g_{FS}	V_{DS} = 15 V, I_D = 100 mA		350	125		mS
DYNAMIC							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		90		110	pF
Output Capacitance	C_{oss}			20		30	
Reverse Transfer Capacitance	C_{rss}			5		10	
SWITCHING							
Turn-On Time	t_{ON}	V_{DD} = 25 V, R_L = 250 Ω, I_D = 0.1 A, V_{GEN} = 10 V, R_G = 25 Ω		5.5		15	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)		40		60	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.