P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	$V_{GS(th)}$ (max)	Order Number / Package	
				TO-92	DICE†
-20V	3.0Ω	-0.35A	-1.3V	TP0702N3	TP0702ND

† MIL visual screening available

Features

- ☐ Low threshold —1.0V max
- ☐ On resistance guaranteed at V_{GS} = 2, 3, and 5 volts
- ☐ High input impedance
- ☐ Low input capacitance —130 pF typical
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage

Applications

- ☐ Logic level interface
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line driver
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options (Note 1)

TO-92

Note 1: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-92	-0.35A	-0.40A	1W	125	170	-.035A	0.75A

* I_D (continuous) is limited by max rated T_j.

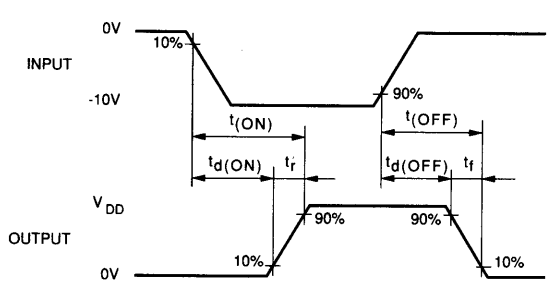
Electrical Characteristics (@ 25°C unless otherwise specified)

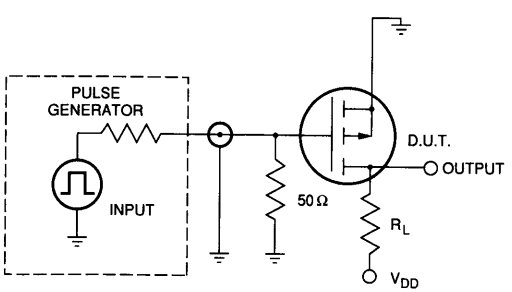
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-20			V	V_{GS} = 0, I_D = -1mA
$V_{GS(th)}$	Gate Threshold Voltage	-0.7		-1.3	V	V_{GS} = V_{DS}, I_D = -1.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.5	mV/°C	V_{GS} = V_{DS}, I_D = -1.0mA
I_{GSS}	Gate Body Leakage			-100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current			-100	nA	V_{DS} = 20V, V_{GS} = 0V
				-100	µA	V_{DS} = 0.8 Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	-0.35			A	V_{GS} = V_{DS} = 5V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			10.0	Ω	V_{GS} = 2V, I_D = -30mA
				5.0		V_{GS} = 3V, I_D = -120mA
				3.0		V_{GS} = 5V, I_D = -250mA
G_{FS}	Forward Transconductance	80			m℧	V_{DS} = 5V, I_D = -250mA
C_{ISS}	Input Capacitance		130	200	pF	V_{GS} = 0V, V_{DS} = -20V, f =1MHz
C_{OSS}	Common Source Output Capacitance		70	125		
C_{RSS}	Reverse Transfer Capacitance		30	60		
$t_{d(ON)}$	Turn-ON Delay Time			20	ns	V_{DD} = 20V, I_D =-250mA, R_S = 50Ω
t_r	Rise Time			20		
$t_{d(OFF)}$	Turn-OFF Delay Time			30		
t_f	Fall Time			20		
V_{SD}	Diode Forward Voltage Drop			-1.0	V	V_{GS} = 0V, I_{SD} = -250mA

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwide stated. (Pulse test: 300 µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
				TO-243AA*	DICE†
-20V	2.0Ω	-2.4V	-2.0A	TP2502N8	TP2502ND

* Same as SOT-89.
† MIL visual screening available.

Features

- ☐ Low threshold — -2.4V max.
- ☐ High input impedance
- ☐ Low input capacitance — 125 pF max.
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Logic level interface – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line driver
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

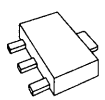
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options (Note 1)



TO-243AA
(SOT-89)

Note 1: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-243AA	-0.37A	-2.0A	0.55W†	227†	—	-0.37A	-2.0A

* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 board, 25mm x 19mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

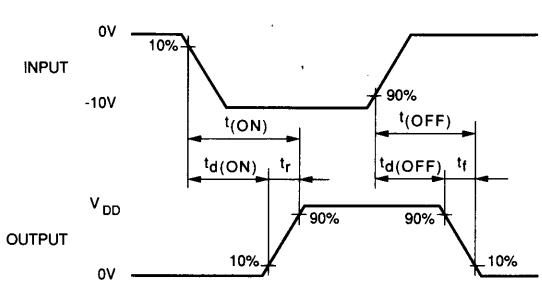
Electrical Characteristics (@ 25°C unless otherwise specified)

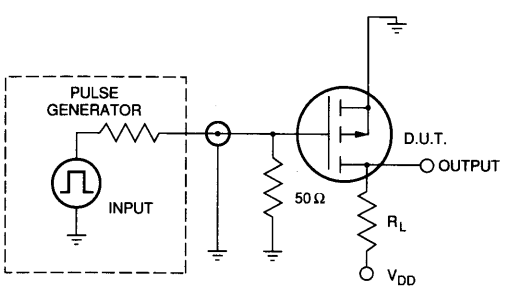
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TP2504	-40			V	V_{GS} = 0, I_D = -2mA
		TP2502	-20				
$V_{GS(th)}$	Gate Threshold Voltage		-1.0		-2.4	V	V_{GS} = V_{DS}, I_D = -1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			3.0	4.5	mV/°C	V_{GS} = V_{DS}, I_D = -1mA
I_{GSS}	Gate Body Leakage				-100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	V_{GS} = 0, V_{DS} = Max Rating
					-1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		-0.4	-0.7		A	V_{GS} = -5V, V_{DS} = -15V
			-2.0	-3.3			V_{GS} = -10V, V_{DS} = -15V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			2.0	3.5	Ω	V_{GS} = -5V, I_D = -250mA
				1.5	2.0		V_{GS} = -10V, I_D = -1A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.75	1.2	%/°C	V_{GS} = -10V, I_D = -1A
G_{FS}	Forward Transconductance		0.4	0.65		℧	V_{DS} = -15V, I_D = -1A
C_{ISS}	Input Capacitance				125	pF	V_{GS} = 0, V_{DS} = -15V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance				70		
C_{RSS}	Reverse Transfer Capacitance				25		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	V_{DD} = -15V, I_D = -1.0A, R_S = 50Ω
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				15		
t_f	Fall Time				10		
V_{SD}	Diode Forward Voltage Drop			1.3	2.0	V	V_{GS} = 0, I_{SD} = -1.5A
t_{rr}	Reverse Recovery Time			300		ns	V_{GS} = 0, I_{SD} = -1.5A

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300ms pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
				TO-243AA*	DICE†
-60V	3.5Ω	-2.4V	-1.5A	—	TP2506ND
-100V	3.5Ω	-2.4V	-1.5A	TP2510N8	TP2510ND

* Same as SOT-89.
† MIL visual screening available.

Features

- ☐ Low threshold — -2.4V max.
- ☐ High input impedance
- ☐ Low input capacitance — 125 pF max
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Logic level interface – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line driver
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

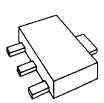
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options (Note 1)



TO-243AA
(SOT-89)

Note 1: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-243AA	-0.28A	-1.5A	0.55W†	227†	—	-0.28A	-1.5A

* I_D (continuous) is limited by max rated T_j.

† Mounted on FR5 board, 25mm x 19mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

Electrical Characteristics (@ 25°C unless otherwise specified)

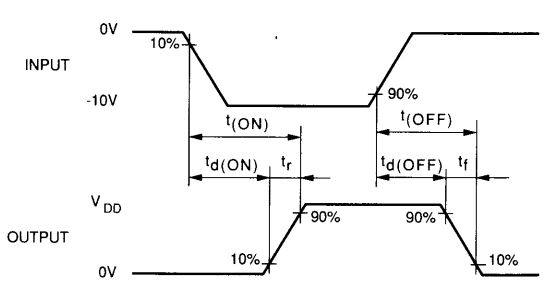
(Notes 1 and 2)

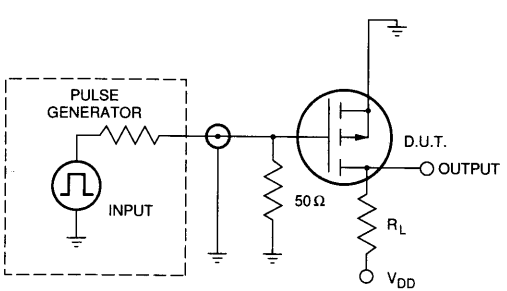
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TP2510	-100			V	V_{GS} = 0, I_D = -2mA
		TP2506	-60				
$V_{GS(th)}$	Gate Threshold Voltage		-1.0		-2.4	V	V_{GS} = V_{DS}, I_D= -1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				5.0	mV/°C	V_{GS} = V_{DS}, I_D= -1mA
I_{GSS}	Gate Body Leakage				-100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	V_{GS} = 0, V_{DS} = Max Rating
					-1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		-0.4	-0.6		A	V_{GS} = -5V, V_{DS} = -25V
			-1.5	-2.5			V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			5	7	Ω	V_{GS} = -5V, I_D = -250mA
				3	3.5		V_{GS} = -10V, I_D = -0.75A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				1.7	%/°C	V_{GS} = -10V, I_D = -0.75A
G_{FS}	Forward Transconductance		300			m℧	V_{DS} = -25V, I_D = -0.75A
C_{ISS}	Input Capacitance				125	pF	V_{GS} = 0, V_{DS} = -25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance				70		
C_{RSS}	Reverse Transfer Capacitance				25		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	V_{DD} = -25V, I_D = -1.0A, R_S = 50Ω
t_r	Rise Time				15		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				15		
V_{SD}	Diode Forward Voltage Drop				-1.8	V	V_{GS} = 0, I_{SD} = -1.0A
t_{rr}	Reverse Recovery Time			300		ns	V_{GS} = 0, I_{SD} = -1.0A

Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300ms pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
				TO-243AA*	DICE†
-160V	12Ω	-2.4V	-0.75A	—	TP2516ND
-200V	12Ω	-2.4V	-0.75A	TP2520N8	TP2520ND

* Same as SOT-89.
† MIL visual screening available.

Features

- ☐ Low threshold — -2.4V max.
- ☐ High input impedance
- ☐ Low input capacitance — 125 pF max.
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

Applications

- ☐ Logic level interface – ideal for TTL and CMOS
- ☐ Solid state relays
- ☐ Battery operated systems
- ☐ Photo voltaic drive
- ☐ Analog switches
- ☐ General purpose line driver
- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

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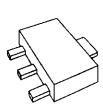
Package Options (Note 1)



TO-243AA
(SOT-89)

Note 1: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation / @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-243AA	-0.15A	-0.75A	0.55W†	227†	—	-0.15A	-0.75A

* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 board, 25mm x 19mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

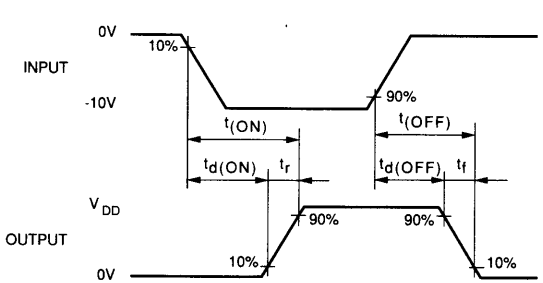
Electrical Characteristics (@ 25°C unless otherwise specified)

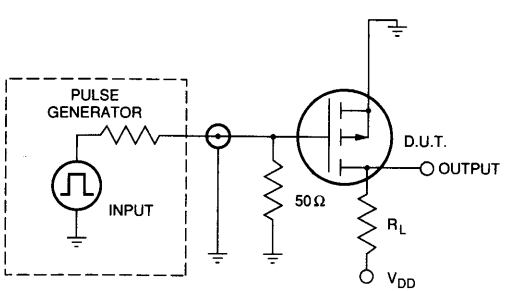
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TP2520	-200			V	V_{GS} = 0, I_D = -2mA
		TP2516	-160				
$V_{GS(th)}$	Gate Threshold Voltage		-1.0		-2.4	V	V_{GS} = V_{DS}, I_D= -1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				4.5	mV/°C	V_{GS} = V_{DS}, I_D= -1mA
I_{GSS}	Gate Body Leakage				-100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	V_{GS} = 0, V_{DS} = Max Rating
					-1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		-0.25			A	V_{GS} = -4.5V, V_{DS} = -25V
			-0.75				V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			12	15	Ω	V_{GS} = -4.5V, I_D = -100mA
				9	12		V_{GS} = -10V, I_D = -200mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				1.7	%/°C	V_{GS} = -10V, I_D = -200mA
G_{FS}	Forward Transconductance		100			m℧	V_{DS} = -25V, I_D = -200mA
C_{ISS}	Input Capacitance				125	pF	V_{GS} = 0, V_{DS} = -25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance				85		
C_{RSS}	Reverse Transfer Capacitance				35		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	V_{DD} = -25V, I_D = -1.0A, R_S = 50Ω
t_r	Rise Time				15		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				15		
V_{SD}	Diode Forward Voltage Drop				-1.8	V	V_{GS} = 0, I_{SD} = -0.5A
t_{rr}	Reverse Recovery Time			300		ns	V_{GS} = 0, I_{SD} = -0.5A

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300ms pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
				TO-92	TO-243AA*	DICE†
-350V	25Ω	-2.4V	-0.4A	TP2535N3	—	TP2535ND
-400V	25Ω	-2.4V	-0.4A	TP2540N3	TP2540N8	TP2540ND

* Same as SOT-89.
† MIL visual screening available.

Features

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- ☐ High input impedance
- ☐ Low input capacitance — 125 pF typical
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- ☐ Logic level interface – ideal for TTL and CMOS
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- ☐ Telecom switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

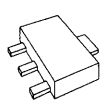
* Distance of 1.6 mm from case for 10 seconds.

Low Threshold DMOS Technology

These low threshold enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options (Note 1)



TO-243AA
(SOT-89)

TO-92

Note 1: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-92	-0.3A	-0.6A	1W	125	170	-03A	-0.6A
TO-243AA	-0.1A	-0.4A	0.55W†	227†	—	-0.1A	-0.4A

* I_D (continuous) is limited by max rated T_j.
† Mounted on FR5 board, 25mm x 19mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

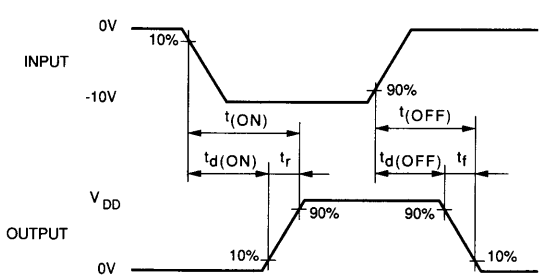
Electrical Characteristics (@ 25°C unless otherwise specified)

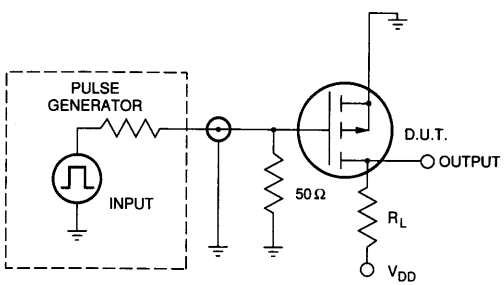
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	TP2540	-400			V	V_{GS} = 0, I_D = -2mA
		TP2535	-350				
$V_{GS(th)}$	Gate Threshold Voltage		-1.0		-2.4	V	V_{GS} = V_{DS}, I_D= -1mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature				4.8	mV/°C	V_{GS} = V_{DS}, I_D= -1mA
I_{GSS}	Gate Body Leakage				-100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-10	µA	V_{GS} = 0, V_{DS} = Max Rating
					-1	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		-200	-300		mA	V_{GS} = -4.5V, V_{DS} = -25V
			-400	-550			V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			20	30	Ω	V_{GS} = -4.5V, I_D = -100mA
				19	25		V_{GS} = -10V, I_D = -100mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature				0.75	%/°C	V_{GS} = -10V, I_D = -100mA
G_{FS}	Forward Transconductance		100			m℧	V_{DS} = -25V, I_D = -100mA
C_{ISS}	Input Capacitance				125	pF	V_{GS} = 0, V_{DS} = -25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance				70		
C_{RSS}	Reverse Transfer Capacitance				25		
$t_{d(ON)}$	Turn-ON Delay Time				10	ns	V_{DD} = -25V, I_D = -100mA, R_S = 50Ω
t_r	Rise Time				10		
$t_{d(OFF)}$	Turn-OFF Delay Time				20		
t_f	Fall Time				10		
V_{SD}	Diode Forward Voltage Drop				-1.8	V	V_{GS} = 0, I_{SD} = -100mA
t_{rr}	Reverse Recovery Time			300		ns	V_{GS} = 0, I_{SD} = -100mA

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300ms pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

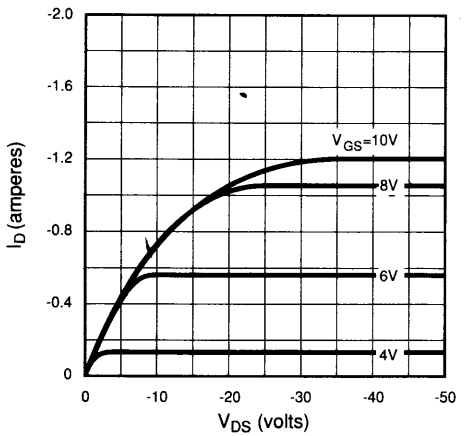
Switching Waveforms and Test Circuit



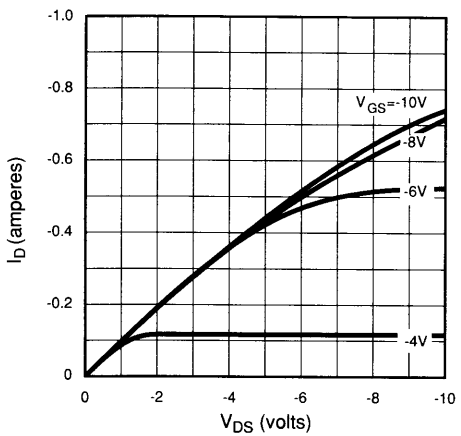


Typical Performance Curves

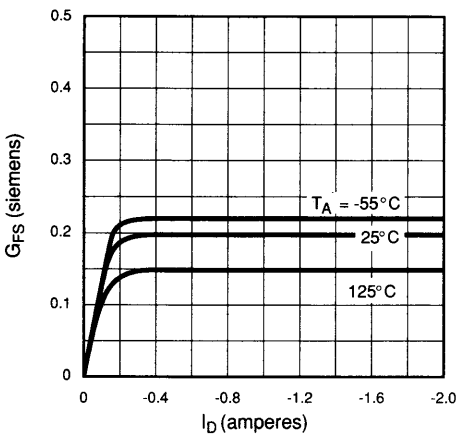
Output Characteristics



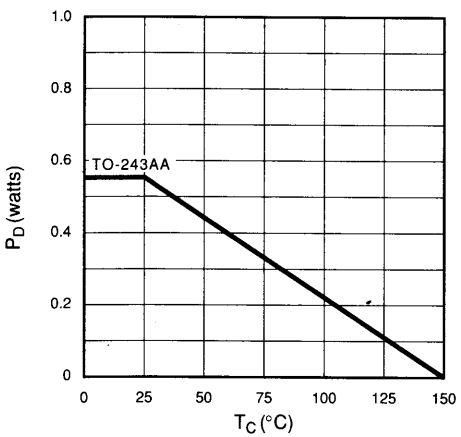
Saturation Characteristics



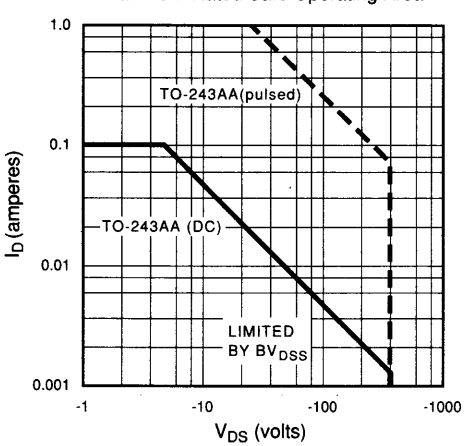
Transconductance vs. Drain Current



Power Dissipation vs. Case Temperature

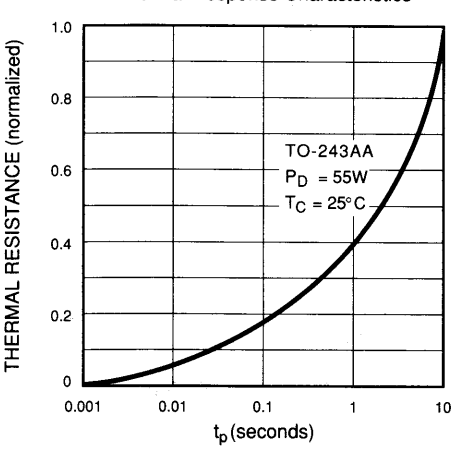


Maximum Rated Safe Operating Area

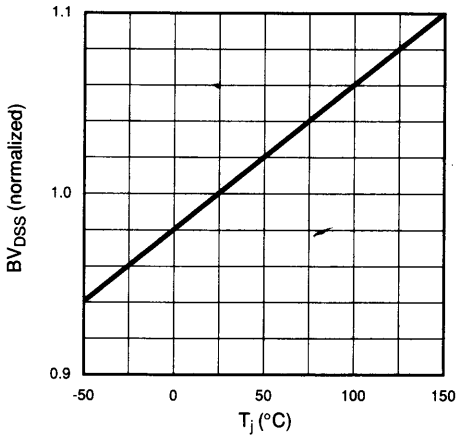


Pulsed Condition: 300 µs; 20% Duty Cycle

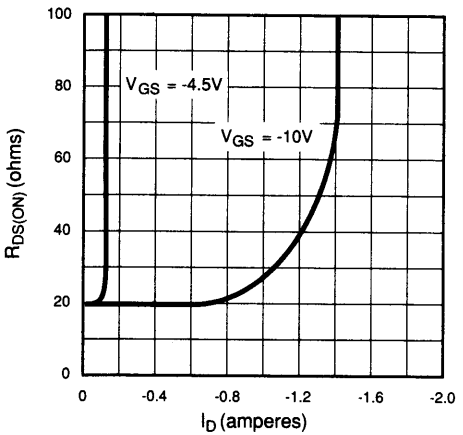
Thermal Response Characteristics



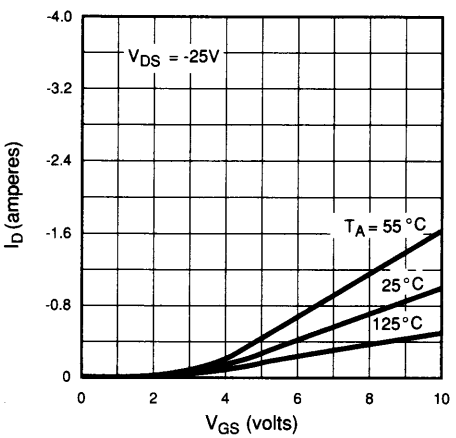
BV$_{DSS}$ Variation with Temperature



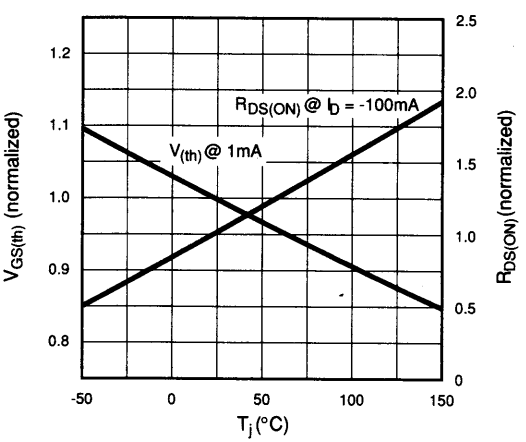
On-Resistance vs. Drain Current



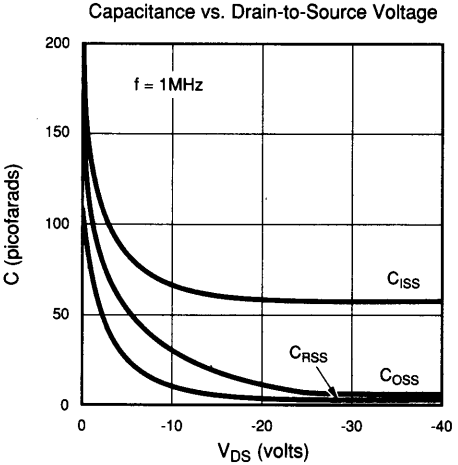
Transfer Characteristics



V$_{(th)}$ and R$_{DS}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics