TP1220L, TP2020L
P-Channel Enhancement-Mode MOS Transistors

Siliconix incorporated

PRODUCT SUMMARY

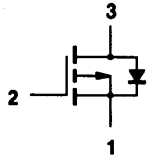
PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
TP1220L	-120	20	-0.12
TP2020L	-200	20	-0.12

Performance Curves: VPDQ20

TO-92 (TO-226AA)

BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS TP1220L	LIMITS TP2020L	UNITS
Drain-Source Voltage		V_{DS}	-120	-200	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current	T_A = 25°C	I_D	-0.12	-0.12	A
	T_A = 100°C		-0.08	-0.08	
Pulsed Drain Current[1]		I_{DM}	-0.48	-0.48	
Maximum Power Dissipation	T_A = 25°C	P_D	0.80	0.80	W
	T_A = 100°C		0.32	0.32	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	156	K/W

[1]Pulse width limited by maximum junction temperature.

SPECIFICATIONS[a]				LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V	TP1220L	-200	-120		V
		I_D = -10 µA	TP2020L	-220	-200		
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -1 mA		-1.9	-1	-2.4	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±10	nA
			T_J = 125°C			±50	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V				-1	µA
			T_J = 125°C			-100	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = -10 V, V_{GS} = -4.5 V		-250	-50		mA
Drain-Source On-Resitance[c]	$r_{DS(ON)}$	V_{GS} = -4.5 V, I_D = -50 mA		15		20	Ω
			T_J = 125°C	30		40	
		V_{GS} = -10 V, I_D = -100 mA		15		20	
Forward Transconductance[c]	g_{FS}	V_{DS} = -10 V, I_D = -100 mA		100	60		mS
DYNAMIC							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = -25 V, f = 1 MHz		30		60	pF
Output Capacitance	C_{oss}			10		20	
Reverse Transfer Capacitance	C_{rss}			2		10	
SWITCHING							
Turn-On Time	t_{ON}	V_{DD} = -25 V, R_L = 250 Ω, I_D = -0.1 A V_{GEN} = -10 V, R_G = 25 Ω		15		25	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)		35		55	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.

6

TP2010L, TP2410L
P-Channel Enhancement-Mode MOS Transistors

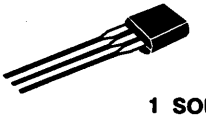
Siliconix incorporated

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
TP2010L	-200	10	-0.18
TP2410L	-240	10	-0.18

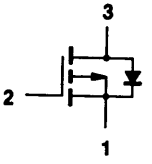
Performance Curves: VPDV24

TO-92 (TO-226AA)



BOTTOM VIEW

1 SOURCE
2 GATE
3 DRAIN



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS TP2010L	LIMITS TP2410L	UNITS
Drain-Source Voltage		V_{DS}	-200	-240	V
Gate-Source Voltage		V_{GS}	±20	±20	
Continuous Drain Current	T_A = 25°C	I_D	-0.18	-0.18	A
	T_A = 100°C		-0.11	-0.11	
Pulsed Drain Current[1]		I_{DM}	-0.72	-0.72	
Maximum Power Dissipation	T_A = 25°C	P_D	0.80	0.80	W
	T_A = 100°C		0.32	0.32	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	LIMITS	UNITS
Junction-to-Ambient	R_{thJA}	156	K/W

[1]Pulse width limited by maximum junction temperature.

SPECIFICATIONS[a]				LIMITS			
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = −10 µA	TP2010L	−220	−200		V
			TP2410L	−255	−240		
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −1 mA		−1.9	−1	−2.4	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±10	nA
			T_J = 125°C			±50	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V				−1	µA
			T_J = 125°C			−100	
On-State Drain Current[c]	$I_{D(ON)}$	V_{DS} = −10 V, V_{GS} = −4.5 V		−300	−100		mA
Drain-Source On-Resitance[c]	$r_{DS(ON)}$	V_{GS} = −4.5 V, I_D = −100 mA		8.5		10	Ω
			T_J = 125°C	15.5		20	
Forward Transconductance[c]	g_{FS}	V_{DS} = −10 V, I_D = −100 mA		175	125		mS
DYNAMIC							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = −25 V, f = 1 MHz		90		110	pF
Output Capacitance	C_{oss}			30		50	
Reverse Transfer Capacitance	C_{rss}			10		15	
SWITCHING							
Turn-On Time	t_{ON}	V_{DD} = −25 V, R_L = 250 Ω, I_D = −100 mA, V_{GEN} = −10 V, R_G = 25 Ω		25		45	ns
Turn-Off Time	t_{OFF}	(Switching time is essentially independent of operating temperature)		90		130	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.