

RF MOSFET Power Transistor, 100W, 28V

100 - 500 MHz

UF28100H

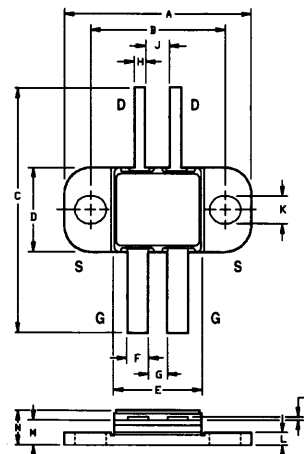
V2.00

Features

- N-Channel Enhancement Mode Device
- DMOS Structure
- Lower Capacitances for Broadband Operation
- High Saturated Output Power
- Lower Noise Figure Than Competitive Devices

Absolute Maximum Ratings at 25°C

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	65	V
Gate-Source Voltage	V_{GS}	20	V
Drain-Source Current	I_{DS}	12*	A
Power Dissipation	P_D	250	W
Junction Temperature	T_J	200	°C
Storage Temperature	T_{STG}	-55 to +150	°C
Thermal Resistance	θ_{JC}	0.7	°C/W



LETTER DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.73	22.99	.903	.905
B	16.26	16.41	.640	.650
C	25.00	25.03	1.000	1.010
D	10.00	10.05	.394	.400
E	10.04	10.06	.400	.401
F	2.41	2.67	.095	.105
G	2.00	2.54	.080	.100
H	1.54	1.60	.061	.063
J	2.79	3.30	.110	.130
K	3.18	3.30	.125	.130
L	1.40	1.65	.055	.065
M	2.87	3.30	.113	.130
N	3.66	4.87	.144	.192
P	.30	.35	.012	.014

Electrical Characteristics at 25°C

Parameter	Symbol	Min	Max	Units	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	65	-	V	$V_{GS}=0.0\text{ V}$, $I_{DS}=15.0\text{ mA}^*$
Drain-Source Leakage Current	I_{DSS}	-	3.0	mA	$V_{DS}=28.0\text{ V}$, $V_{GS}=0.0\text{ V}^*$
Gate-Source Leakage Current	I_{GSS}	-	3.0	μA	$V_{GS}=20\text{ V}$, $V_{DS}=0.0\text{ V}^*$
Gate Threshold Voltage	$V_{GS(TH)}$	2.0	6.0	V	$V_{DS}=10.0\text{ V}$, $I_{DS}=300.0\text{ mA}^*$
Forward Transconductance	G_m	1.5	-	S	$V_{DS}=10.0\text{ V}$, $I_{DS}=3000.0\text{ mA}$, $\Delta V_{GS}=1.0\text{ V}$, 80 μs Pulse*
Input Capacitance	C_{ISS}	-	135	pF	$V_{DS}=28.0\text{ V}$, $F=1.0\text{ MHz}^*$
Output Capacitance	C_{OSS}	-	90	pF	$V_{DS}=28.0\text{ V}$, $F=1.0\text{ MHz}^*$
Reverse Capacitance	C_{RSS}	-	24	pF	$V_{DS}=28.0\text{ V}$, $F=1.0\text{ MHz}^*$
Power Gain	G_p	10	-	dB	$V_{DD}=28.0\text{ V}$, $I_{DQ}=600.0\text{ mA}$, $P_{OUT}=100.0\text{ W}$, $F=500\text{ MHz}$
Drain Efficiency	η_D	50	-	%	$V_{DD}=28.0\text{ V}$, $I_{DQ}=600.0\text{ mA}$, $P_{OUT}=100.0\text{ W}$, $F=500\text{ MHz}$
Return Loss	R_L	10	-	dB	$V_{DD}=28.0\text{ V}$, $I_{DQ}=600.0\text{ mA}$, $P_{OUT}=100.0\text{ W}$, $F=500\text{ MHz}$
Load Mismatch Tolerance	VSWR-T	-	30:1	-	$V_{DD}=28.0\text{ V}$, $I_{DQ}=600.0\text{ mA}$, $P_{OUT}=100.0\text{ W}$, $F=500\text{ MHz}$

* Per Side

Specifications Subject to Change Without Notice.

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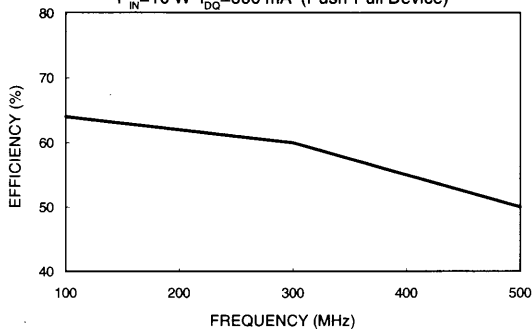
North America: Tel. (800) 366-2266
Fax (800) 618-8883

Asia/Pacific: Tel. +81 (03) 3226-1671
Fax +81 (03) 3226-1451

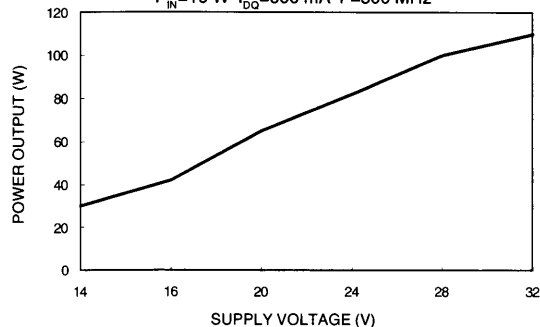
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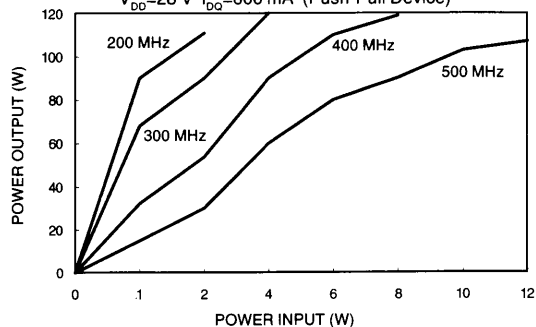
Typical Broadband Performance Curves

EFFICIENCY vs² FREQUENCY $P_{IN}=10\text{ W}$ $I_{DQ}=600\text{ mA}$ (Push-Pull Device)

POWER OUTPUT vs SUPPLY VOLTAGE

 $P_{IN}=10\text{ W}$ $I_{DQ}=600\text{ mA}$ $F=500\text{ MHz}$ 

POWER OUTPUT vs POWER INPUT

 $V_{DQ}=28\text{ V}$ $I_{DQ}=600\text{ mA}$ (Push-Pull Device)

Specifications Subject to Change Without Notice.

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Fax (800) 618-8883

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Fax +81 (03) 3226-1451

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Typical Device Impedance

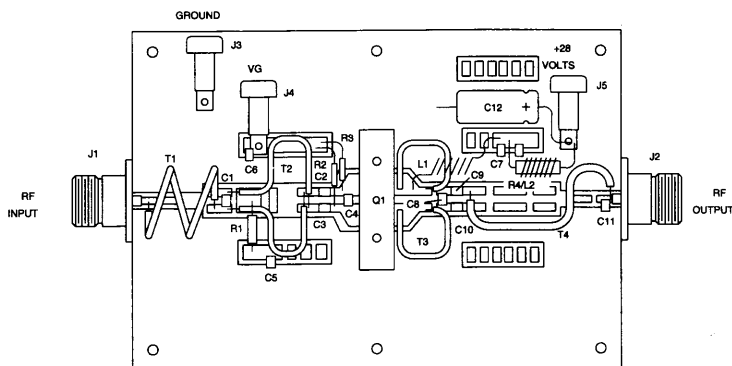
Frequency (MHz)	Z_{IN} (OHMS)	Z_{LOAD} (OHMS)
100	$4.5 - j 6.0$	$14.5 + j 0.5$
300	$2.25 - j 1.75$	$7.5 + j 1.0$
500	$1.5 + j 5.5$	$3.5 - j 3.5$

$$V_{DD}=28 \text{ V}, I_{DQ}=600 \text{ mA}, P_{OUT}=100.0 \text{ Watts}$$

Z_{IN} is the series equivalent input impedance of the device from gate to gate.

Z_{LOAD} is the optimum series equivalent load impedance as measured from drain to drain.

RF Test Fixture



PARTS LIST

C1,C8	CHIP CAPACITOR, 2.0pF ATC B
C2,C3	CHIP CAPACITOR, 5000pF
C4	CHIP CAPACITOR, 37pF ATC B
C5	CHIP CAPACITOR, 260pF ATC B
C6,C7	CHIP CAPACITOR, .015uF
C9,C10	CHIP CAPACITOR, 560pF ATC B
C11	CHIP CAPACITOR, 0.6pF ATC B
C12	ELECTROLYTIC CAPACITOR, 50uF 50 VOLTS
R1,R4	RESISTOR, 27 OHM .25 WATT
R2,R3	RESISTOR, 22K OHM .25 WATT
L1	INDUCTOR, 5 TURNS OF NO. 18 AWG ON .10"
L2	INDUCTOR, 10 TURNS OF NO. 22 AWG ON R4
T1	1:1 BALUN TRANSFORMER, 50 OHM SEMI-RIGID COAX .085" X 3" LONG
T2	4:1 BALUN TRANSFORMER, 25 OHM SEMI-RIGID COAX .070" X 2.5" LONG
T3	1:9 BALUN TRANSFORMER, 10 OHM SEMI-RIGID COAX .070" X 2.5" LONG
T4	1:1 BALUN TRANSFORMER, 50 OHM SEMI-RIGID COAX .085" X 4" LONG
Q1	UF28100H
BOARD	ROGERS 5870, .031" THICK
J1,J2	CONNECTOR, TYPE 'N'
J3,J4,J5	BANANA JACK
HEATSINK	FINNED ALUMINUM, D/N 73050182-03

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RF MOSFET Power Transistor, 100W, 28V

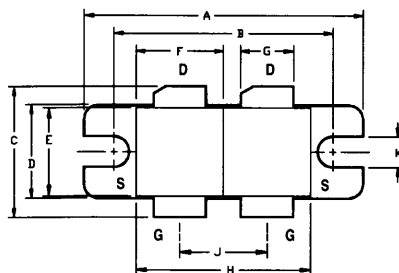
100 - 500 MHz

UF28100M

V2.00

Features

- N-Channel Enhancement Mode Device
- DMOS Structure
- Lower Capacitances for Broadband Operation
- High Saturated Output Power
- Lower Noise Figure Than Competitive Devices



Absolute Maximum Ratings at 25°C

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	65	V
Gate-Source Voltage	V_{GS}	20	V
Drain-Source Current	I_{DS}	12*	A
Power Dissipation	P_D	250	W
Junction Temperature	T_J	200	°C
Storage Temperature	T_{STG}	-55 to +150	°C
Thermal Resistance	θ_{JC}	0.7	°C/W

LETTER DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	30.35	30.61	1.195	1.205
B	23.65	23.90	.931	.941
C	13.72	14.22	.540	.560
D	9.63	9.88	.379	.389
E	9.44	9.65	.370	.380
F	9.44	9.65	.370	.380
G	5.59	5.84	.220	.230
H	18.80	19.30	.740	.760
J	9.44	9.65	.370	.380
K	3.12	3.38	.123	.133
L	1.47	1.57	.058	.062
M	2.39	2.74	.094	.108
N	5.03	5.69	.198	.224
P	.05	.13	.002	.005

Electrical Characteristics at 25°C

Parameter	Symbol	Min	Max	Units	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	65	-	V	$V_{GS}=0.0\text{ V}$, $I_{DS}=15.0\text{ mA}^*$
Drain-Source Leakage Current	I_{DSS}	-	3.0	mA	$V_{DS}=28.0\text{ V}$, $V_{GS}=0.0\text{ V}^*$
Gate-Source Leakage Current	I_{GSS}	-	3.0	μA	$V_{GS}=20\text{ V}$, $V_{DS}=0.0\text{ V}^*$
Gate Threshold Voltage	$V_{GS(TH)}$	2.0	6.0	V	$V_{DS}=10.0\text{ V}$, $I_{DS}=300.0\text{ mA}^*$
Forward Transconductance	G_m	1.5	-	S	$V_{DS}=10.0\text{ V}$, $I_{DS}=3000.0\text{ mA}$, $\Delta V_{GS}=1.0\text{ V}$, 80 μs Pulse*
Input Capacitance	C_{ISS}	-	135	pF	$V_{DS}=28.0\text{ V}$, $F=1.0\text{ MHz}^*$
Output Capacitance	C_{OSS}	-	90	pF	$V_{DS}=28.0\text{ V}$, $F=1.0\text{ MHz}^*$
Reverse Capacitance	C_{RSS}	-	24	pF	$V_{DS}=28.0\text{ V}$, $F=1.0\text{ MHz}^*$
Power Gain	G_p	10	-	dB	$V_{DS}=28.0\text{ V}$, $I_{DQ}=600.0\text{ mA}$, $P_{OUT}=100.0\text{ W}$, $F=500\text{ MHz}$
Drain Efficiency	η_D	50	-	%	$V_{DS}=28.0\text{ V}$, $I_{DQ}=600.0\text{ mA}$, $P_{OUT}=100.0\text{ W}$, $F=500\text{ MHz}$
Return Loss	R_L	10	-	dB	$V_{DS}=28.0\text{ V}$, $I_{DQ}=600.0\text{ mA}$, $P_{OUT}=100.0\text{ W}$, $F=500\text{ MHz}$
Load Mismatch Tolerance	VSWR-T	-	30:1	-	$V_{DS}=28.0\text{ V}$, $I_{DQ}=600.0\text{ mA}$, $P_{OUT}=100.0\text{ W}$, $F=500\text{ MHz}$

* Per Side

Specifications Subject to Change Without Notice.

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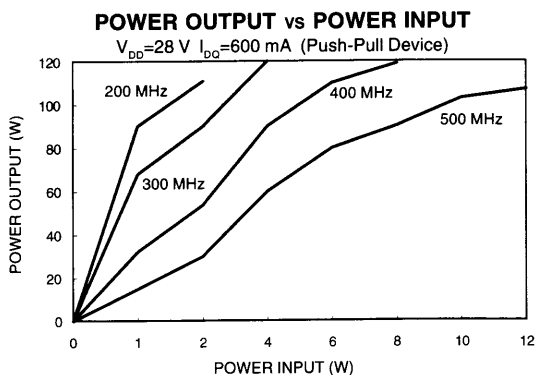
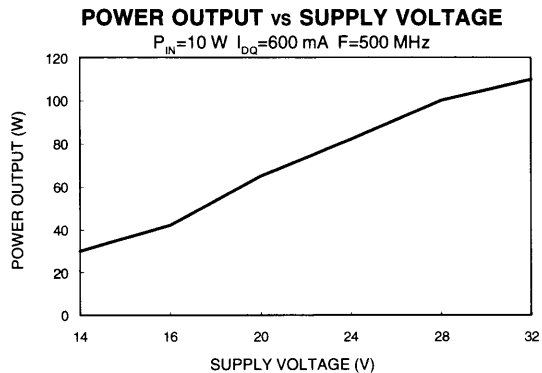
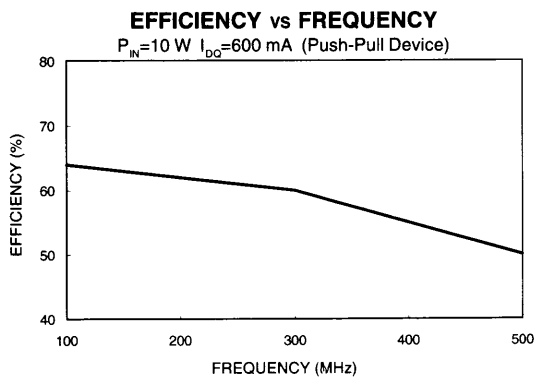
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Typical Broadband Performance Curves



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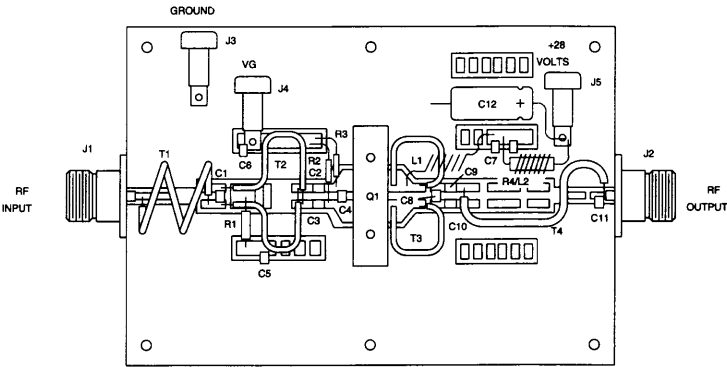
Typical Device Impedance

Frequency (MHz)	Z_{IN} (OHMS)	Z_{LOAD} (OHMS)
100	4.5 - j 6.0	14.5 + j 0.5
300	2.25 - j 1.75	7.5 + j 1.0
500	1.5 + j 5.5	3.5 - j 3.5

$V_{DD}=28\text{ V}$, $I_{DQ}=600\text{ mA}$, $P_{OUT}=100.0\text{ Watts}$

Z_{IN} is the series equivalent input impedance of the device from gate to gate.
 Z_{LOAD} is the optimum series equivalent load impedance as measured from drain to drain.

RF Test Fixture



PARTS LIST

C1,C8	CHIP CAPACITOR, 2.0pF ATC B
C2,C3	CHIP CAPACITOR, 5000pF
C4	CHIP CAPACITOR, 37pF ATC B
C5	CHIP CAPACITOR, 280pF ATC B
C6,C7	CHIP CAPACITOR, .015uF
C9,C10	CHIP CAPACITOR, 560pF ATC B
C11	CHIP CAPACITOR, 0.6pF ATC B
C12	ELECTROLYTIC CAPACITOR, 50uF 50 VOLTS
R1,R4	RESISTOR, 27 OHM .25 WATT
R2,R3	RESISTOR, 22K OHM .25 WATT
L1	INDUCTOR, 5 TURNS OF NO. 18 AWG ON .10"
L2	INDUCTOR, 10 TURNS OF NO. 22 AWG ON R4
T1	1:1 BALUN TRANSFORMER, 50 OHM SEMI-RIGID COAX .085" X 3" LONG
T2	4:1 BALUN TRANSFORMER, 25 OHM SEMI-RIGID COAX .070" X 2.5" LONG
T3	1:9 BALUN TRANSFORMER, 10 OHM SEMI-RIGID COAX .070" X 2.5" LONG
T4	1:1 BALUN TRANSFORMER, 50 OHM SEMI-RIGID COAX .085" X 4" LONG
Q1	UF28100M
BOARD	ROGERS 5870, .031" THICK
J1,J2	CONNECTOR, TYPE 'N'
J3,J4,J5	BANANA JACK
HEATSINK	FINNED ALUMINUM, D/N 73050182-03

RF MOSFET Power Transistor, 100W, 28V

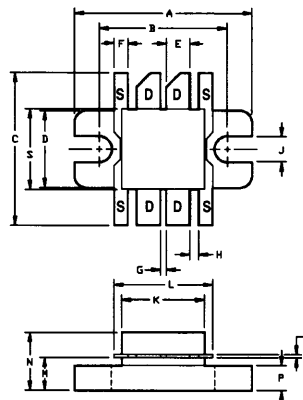
100 - 500 MHz

UF28100V

V2.00

Features

- N-Channel Enhancement Mode Device
- DMOS Structure
- Lower Capacitances for Broadband Operation
- High Saturated Output Power
- Lower Noise Figure Than Competitive Devices



LETTER DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.73	22.99	.895	.905
B	16.38	16.54	.645	.653
C	19.03	19.36	.750	.770
D	.382	.389	.382	.389
E	2.92	3.18	.115	.125
F	1.65	1.91	.065	.075
G	.64	.89	.025	.035
H	1.02	1.27	.040	.050
J	3.18	3.30	.125	.130
K	10.67	10.87	.420	.429
L	12.43	12.93	.490	.510
N	4.06	4.57	.160	.180
M	6.71	7.52	.264	.296
P	3.03	3.30	.120	.130
R	.10	.25	.004	.010
S	10.06	10.26	.396	.404

Absolute Maximum Ratings at 25°C

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	65	V
Gate-Source Voltage	V_{GS}	20	V
Drain-Source Current	I_{DS}	12*	A
Power Dissipation	P_D	250	W
Junction Temperature	T_J	200	°C
Storage Temperature	T_{STG}	-55 to +150	°C
Thermal Resistance	θ_{JC}	0.7	°C/W

Electrical Characteristics at 25°C

Parameter	Symbol	Min	Max	Units	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	65	-	V	$V_{GS}=0.0\text{ V}$, $I_{DS}=15.0\text{ mA}^*$
Drain-Source Leakage Current	I_{DSS}	-	3.0	mA	$V_{DS}=28.0\text{ V}$, $V_{GS}=0.0\text{ V}^*$
Gate-Source Leakage Current	I_{GSS}	-	3.0	μA	$V_{GS}=20\text{ V}$, $V_{DS}=0.0\text{ V}^*$
Gate Threshold Voltage	$V_{GS(TH)}$	2.0	6.0	V	$V_{DS}=10.0\text{ V}$, $I_{DS}=300.0\text{ mA}^*$
Forward Transconductance	G_M	1.5	-	S	$V_{DS}=10.0\text{ V}$, $I_{DS}=3000.0\text{ mA}$, $\Delta V_{GS}=1.0\text{ V}$, 80 μs Pulse*
Input Capacitance	C_{ISS}	-	135	pF	$V_{DS}=28.0\text{ V}$, $F=1.0\text{ MHz}^*$
Output Capacitance	C_{OSS}	-	90	pF	$V_{DS}=28.0\text{ V}$, $F=1.0\text{ MHz}^*$
Reverse Capacitance	C_{RSS}	-	24	pF	$V_{DS}=28.0\text{ V}$, $F=1.0\text{ MHz}^*$
Power Gain	G_p	10	-	dB	$V_{DD}=28.0\text{ V}$, $I_{DG}=600.0\text{ mA}$, $P_{OUT}=100.0\text{ W}$, $F=500\text{ MHz}$
Drain Efficiency	η_D	50	-	%	$V_{DD}=28.0\text{ V}$, $I_{DG}=600.0\text{ mA}$, $P_{OUT}=100.0\text{ W}$, $F=500\text{ MHz}$
Load Mismatch Tolerance	VSWR-T	-	30:1	-	$V_{DD}=28.0\text{ V}$, $I_{DG}=600.0\text{ mA}$, $P_{OUT}=100.0\text{ W}$, $F=500\text{ MHz}$

* Per Side

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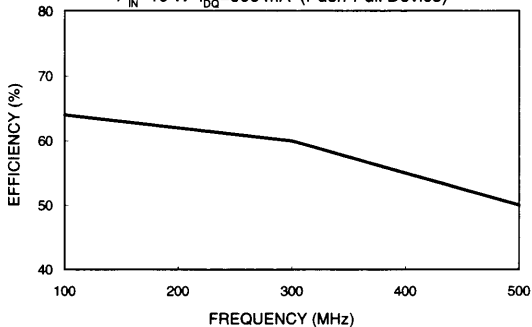
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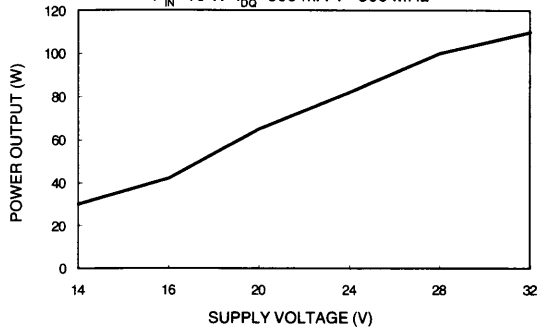
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Typical Broadband Performance Curves

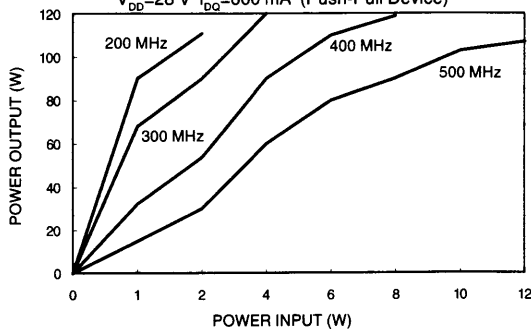
EFFICIENCY vs FREQUENCY

 $P_{IN}=10\text{ W}$ $I_{DQ}=600\text{ mA}$ (Push-Pull Device)

POWER OUTPUT vs SUPPLY VOLTAGE

 $P_{IN}=10\text{ W}$ $I_{DQ}=600\text{ mA}$ $F=500\text{ MHz}$ 

POWER OUTPUT vs POWER INPUT

 $V_{DD}=28\text{ V}$ $I_{DQ}=600\text{ mA}$ (Push-Pull Device)

Specifications Subject to Change Without Notice.

Typical Device Impedance

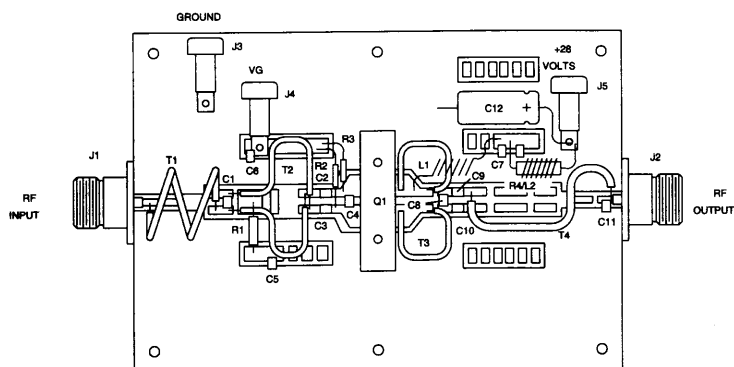
Frequency (MHz)	Z_{IN} (OHMS)	Z_{LOAD} (OHMS)
100	$4.5 - j 6.0$	$14.5 + j 0.5$
300	$2.25 - j 1.75$	$7.5 + j 1.0$
500	$1.5 + j 5.5$	$3.5 - j 3.5$

$$V_{DD}=28 \text{ V}, I_{DQ}=600 \text{ mA}, P_{OUT}=100.0 \text{ Watts}$$

Z_{IN} is the series equivalent input impedance of the device from gate to gate.

Z_{LOAD} is the optimum series equivalent load impedance as measured from drain to drain.

RF Test Fixture



PARTS LIST

C1,C8	CHIP CAPACITOR, 2.0pF ATC B
C2,C3	CHIP CAPACITOR, 5000pF
C4	CHIP CAPACITOR, 37pF ATC B
C5	CHIP CAPACITOR, 260pF ATC B
C6,C7	CHIP CAPACITOR, .015uF
C9,C10	CHIP CAPACITOR, 560pF ATC B
C11	CHIP CAPACITOR, 0.8pF ATC B
C12	ELECTROLYTIC CAPACITOR, 50uF 50 VOLTS
R1,R4	RESISTOR, 27 OHM .25 WATT
R2,R3	RESISTOR, 22K OHM .25 WATT
L1	INDUCTOR, 5 TURNS OF NO. 18 AWG ON .10"
L2	INDUCTOR, 10 TURNS OF NO. 22 AWG ON R4
T1	1:1 BALUN TRANSFORMER, 50 OHM SEMI-RIGID COAX ".085" X 3" LONG
T2	4:1 BALUN TRANSFORMER, 25 OHM SEMI-RIGID COAX ".070" X 2.5" LONG
T3	1:9 BALUN TRANSFORMER, 10 OHM SEMI-RIGID COAX ".070" X 2.5" LONG
T4	1:1 BALUN TRANSFORMER, 50 OHM SEMI-RIGID COAX ".085" X 4" LONG
Q1	UF28100V
BOARD	ROGERS 5870, .031" THICK
J1,J2	CONNECTOR, TYPE 'N'
J3,J4,J5	BANANA JACK
HEATSINK	FINNED ALUMINUM, D/N 73050182-03

Specifications Subject to Change Without Notice.

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Fax (800) 618-8883

Asia/Pacific: Tel. +81 (03) 3226-1671
Fax +81 (03) 3226-1451

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RF MOSFET Power Transistor, 150W, 28V 100 - 500 MHz

UF28150J

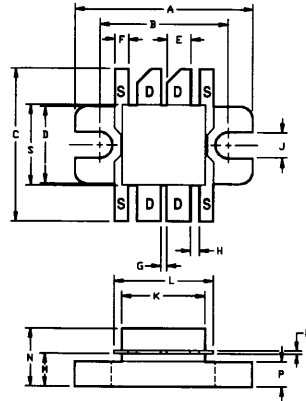
V2.00

Features

- N-Channel Enhancement Mode Device
- DMOS Structure
- Lower Capacitances for Broadband Operation
- Common Source Configuration
- Lower Noise Floor

Absolute Maximum Ratings at 25°C

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	65	V
Gate-Source Voltage	V_{GS}	20	V
Drain-Source Current	I_{DS}	16*	A
Power Dissipation	P_D	389	W
Junction Temperature	T_J	200	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Thermal Resistance	θ_{JC}	0.45	°C/W



LETTER DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.73	22.99	.895	.905
B	16.38	16.64	.645	.655
C	19.85	19.56	.780	.770
D	.382	.389	.015	.016
E	2.92	3.18	.115	.125
F	1.65	1.91	.065	.075
G	.64	.89	.025	.035
H	1.82	1.27	.070	.050
J	3.12	3.38	.123	.133
K	15.67	15.87	.620	.625
L	12.43	12.93	.490	.510
M	4.86	4.57	.190	.180
N	6.71	7.52	.264	.296
P	3.85	3.30	.150	.130
Q	.10	.15	.004	.006
R	10.66	10.25	.420	.404

Electrical Characteristics at 25°C

Parameter	Symbol	Min	Max	Units	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	65	-	V	$V_{GS}=0.0\text{ V}, I_{DS}=25.0\text{ mA}^*$
Drain-Source Leakage Current	I_{DSS}	-	4.0	mA	$V_{DS}=28.0\text{ V}, V_{GS}=0.0\text{ V}^*$
Gate-Source Leakage Current	I_{GSS}	-	4.0	μA	$V_{GS}=20\text{ V}, V_{DS}=0.0\text{ V}^*$
Gate Threshold Voltage	$V_{GS(TH)}$	2.0	6.0	V	$V_{DS}=10.0\text{ V}, I_{DS}=400.0\text{ mA}^*$
Forward Transconductance	G_M	2.0	-	S	$V_{DS}=10.0\text{ V}, I_{DS}=4000.0\text{ mA}, \Delta V_{GS}=1.0\text{ V}, 80\text{ }\mu\text{s Pulse}^*$
Input Capacitance	C_{ISS}	-	180	pF	$V_{DS}=28.0\text{ V}, F=1.0\text{ MHz}^*$
Output Capacitance	C_{OSS}	-	120	pF	$V_{DS}=28.0\text{ V}, F=1.0\text{ MHz}^*$
Reverse Capacitance	C_{RSS}	-	32	pF	$V_{DS}=28.0\text{ V}, F=1.0\text{ MHz}^*$
Power Gain	G_P	8	-	dB	$V_{DD}=28.0\text{ V}, I_{DQ}=400.0\text{ mA}, P_{OUT}=150.0\text{ W}, F=500\text{ MHz}$
Drain Efficiency	η_D	55	-	%	$V_{DD}=28.0\text{ V}, I_{DQ}=400.0\text{ mA}, P_{OUT}=150.0\text{ W}, F=500\text{ MHz}$
Load Mismatch Tolerance	VSWR-T	-	10:1	-	$V_{DD}=28.0\text{ V}, I_{DQ}=400.0\text{ mA}, P_{OUT}=150.0\text{ W}, F=500\text{ MHz}$

* Per Side

Specifications Subject to Change Without Notice.

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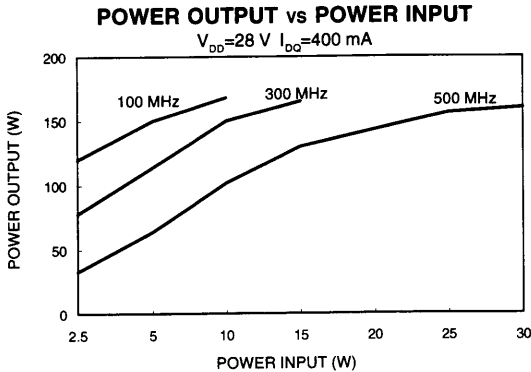
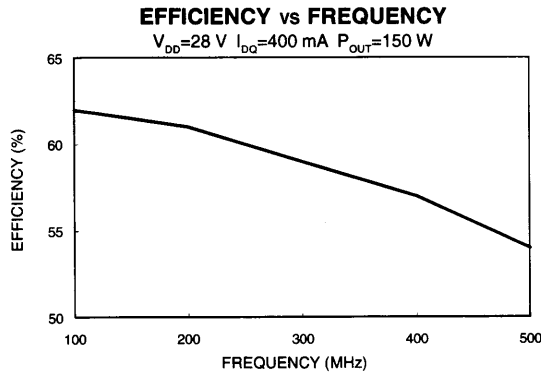
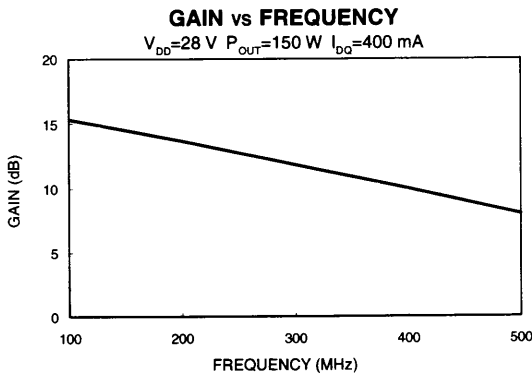
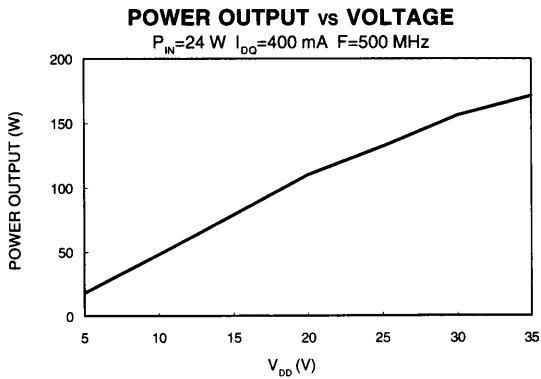
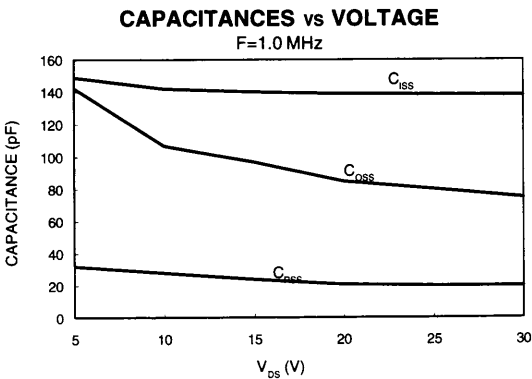
M/A-COM, Inc.

North America: Tel. (800) 366-2266
Fax (800) 618-8883

■ Asia/Pacific: Tel. +81 (03) 3226-1671
Fax +81 (03) 3226-1451

■ Europe: Tel. +44 (1344) 869 595
Fax +44 (1344) 300 020

Typical Broadband Performance Curves



Typical Device Impedance

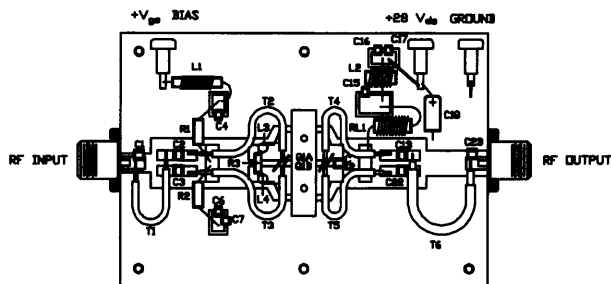
Frequency (MHz)	Z_{IN} (OHMS)	Z_{LOAD} (OHMS)
100	$3.7 - j 5.9$	$3.0 - j 0.7$
300	$2.7 - j 5.8$	$2.6 - j 0.55$
500	$2.5 + j 2.9$	$2.5 - j 0.5$

$$V_{DD}=28\text{ V}, I_{DQ}=400\text{ mA}, P_{OUT}=150.0\text{ Watts}$$

Z_{IN} is the series equivalent input impedance of the device from gate to gate.

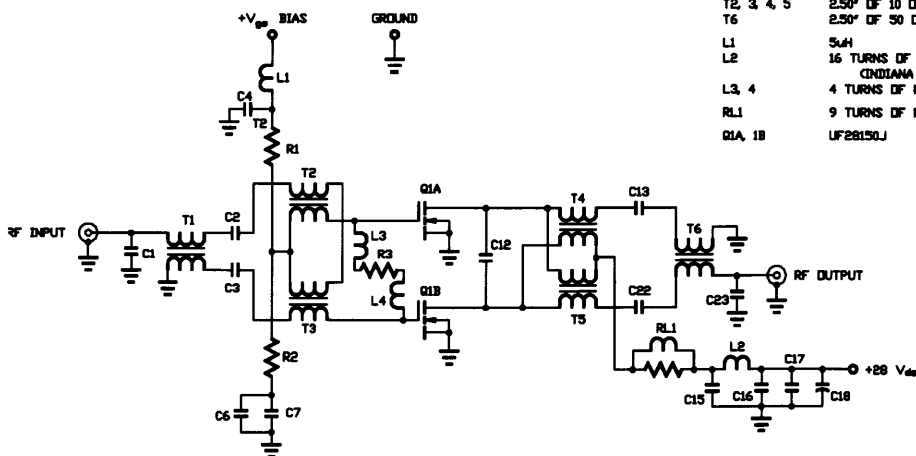
Z_{LOAD} is the optimum series equivalent load impedance as measured from drain to drain.

RF Test Fixture



PARTS LIST

C23	10pF
C1	91pF
C12	11pF
C2, 3, 13, 22	270pF
C7, 16	680pF
C4, 6, 15, 17	.015uF
C18	50uF 50 V.
R1	11K OHM .25 W. 10%
R2	47 OHM .50 W. 10%
R3	12 OHM .25 W. 10%
T1	2.50' OF 50 OHM (.063" O.D) SEMI-RIGID CABLE
T2, 3, 4, 5	2.50' OF 10 OHM (.070" O.D) SEMI-RIGID CABLE
T6	2.50' OF 50 OHM (.141" O.D) SEMI-RIGID CABLE
L1	5uH
L2	16 TURNS OF NO. 18 AVG ON TOROID CORE (INDIANA GENERAL F6278-Q1)
L3, 4	4 TURNS OF NO. 18 AVG ON .125" DIAMETER
RL1	9 TURNS OF NO. 18 AVG ON 15 OHM 2 W. 10% RESISTOR
Q1A, 1B	UF28150J



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