monolithic dual n-channel JFETs *designed for . . .*

- **Low Noise FET Input Amplifiers**
- **Low and Medium Frequency Amplifiers**
- **Impedance Converters**
- **Precision Instrumentation Amplifiers**
- **Comparators**

Siliconix

Performance Curves NNR
See Section 4

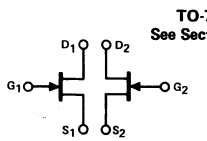
BENEFITS

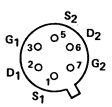
- **Minimum System Error and Calibration**
  5 mV Offset Maximum (U401)
  95 dB Minimum CMRR (U401-04)
- **Low Drift with Temperature**
  10 μV/°C Maximum (U401, 02)
- **Operates from Low Power Supply Voltages**
  $V_{GS(off)} < 2.5$ V
- **Simplifies Amplifier Design**
  Output Conductance < 2 μmho
- **Low Noise**
  $\overline{e}_n = 6\ nV/\sqrt{Hz}$ at 10 Hz Typical

ABSOLUTE MAXIMUM RATINGS (25°C)

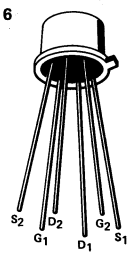
Gate-Drain or Gate-Source Voltage	50 V
Forward Gate Current	10 mA
Device Dissipation (each side)	
@ T_A = 85°C derate 2.6 mW/°C	300 mW
Total Device Dissipation	
@ T_A = 85°C (derate 5 mW/°C)	500 mW
Storage Temperature Range	−65 to 200°C

TO-71
See Section 6





Bottom View



ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

		Characteristic	U401 Min	U401 Max	U402 Min	U402 Max	U403 Min	U403 Max	U404 Min	U404 Max	U405 Min	U405 Max	U406 Min	U406 Max	Unit	Test Conditions	
1		BV_{GSS} Gate-Source Breakdown Voltage	−50		−50		−50		−50		−50		−50		V	V_{DS} = 0, I_G = −1 μA	
2		I_{GSS} Gate Reverse Current (Note 1)		−25		−25		−25		−25		−25		−25	pA	V_{DS} = 0, V_{GS} = −30 V	
3	STATIC	$V_{GS(off)}$ Gate-Source Cutoff Voltage	−.5	−2.5	−.5	−2.5	−.5	−2.5	−.5	−2.5	−.5	−2.5	−.5	−2.5	V	V_{DS} = 15 V, I_D = 1 nA	
4	STATIC	$V_{GS(on)}$ Gate-Source Voltage (on)		−2.3		−2.3		−2.3		−2.3		−2.3		−2.3	V	V_{DG} = 15 V, I_D = 200 μA	
5	STATIC	I_{DSS} Saturation Drain Current (Note 2)	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	mA	V_{DS} = 10 V, V_{GS} = 0	
6	STATIC	I_G Gate Current (Note 1)		−15		−15		−15		−15		−15		−15	pA	V_{DG} = 15 V, I_D = 200 μA	
7	STATIC	I_G Gate Current (Note 1)		−10		−10		−10		−10		−10		−10	nA	I_D = 200 μA	T_A = 125°C
8	STATIC	BV_{G1-G2} Gate-Gate Breakdown Voltage	±50		±50		±50		±50		±50		±50		V	V_{DS} = 0, V_{GS} = 0, I_G = ±1 μA	
9	DYNAMIC	g_{fs} Common-Source Forward Transconductance (Note 2)	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
10	DYNAMIC	g_{os} Common-Source Output Conductance		20		20		20		20		20		20	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
11	DYNAMIC	g_{fs} Common-Source Forward Transconductance	1000	2000	1000	2000	1000	2000	1000	2000	1000	2000	1000	2000	μmho	V_{DG} = 15 V, I_D = 200 μA	f = 1 kHz
12	DYNAMIC	g_{os} Common-Source Output Conductance		2.0		2.0		2.0		2.0		2.0		2.0	μmho	V_{DG} = 15 V, I_D = 200 μA	f = 1 kHz
13	DYNAMIC	C_{iss} Common-Source Input Capacitance		8.0		8.0		8.0		8.0		8.0		8.0	pF	V_{DG} = 15 V, I_D = 200 μA	f = 1 MHz
14	DYNAMIC	C_{rss} Common-Source Reverse Transfer Capacitance		3.0		3.0		3.0		3.0		3.0		3.0	pF	V_{DG} = 15 V, I_D = 200 μA	f = 1 MHz
15	DYNAMIC	$\overline{e}_N$ Equivalent Short-Circuit Input Noise Voltage		20		20		20		20		20		20	nV/√Hz	V_{DS} = 15 V, V_{GS} = 0	f = 10 Hz
16	MATCHING	CMRR Common-Mode Rejection Ratio (Note 3)	95		95		95		95		90				dB	V_{DG} = 10 to 20 V, I_D = 200 μA	
17	MATCHING	$\lvert V_{GS1} - V_{GS2}\rvert$ Differential Gate-Source Voltage		5		10		10		15		20		40	mV	V_{DG} = 10 V, I_D = 200 μA	
18	MATCHING	$\frac{\Delta\lvert V_{GS1} - V_{GS2}\rvert}{\Delta T}$ Gate-Source Voltage Differential Drift (Note 4).		10		10		25		25		40		80	μV/°C	V_{DG} = 10 V, I_D = 200 μA	T_A = −55°C, T_B = +25°C, T_C = +125°C

NOTES:
1. Approximately doubles for every 10°C increase in T_A. 2. Pulse test duration = 300 μs; duty cycle ≤ 3%. 3. $CMRR = 20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1}-V_{GS2}\rvert}\right]$, ΔV_{DD} = 10 V.
4. Measured at end points, T_A, T_B and T_C.

NNR

monolithic dual n-channel JFETs *designed for . . .*

Siliconix

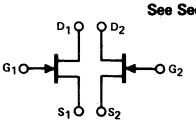
- **FET Input Amplifiers**
- **Low and Medium Frequency Amplifiers**
- **Impedance Converters**
- **Precision Instrumentation Amplifiers**
- **Comparators**

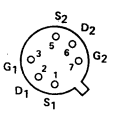
Performance Curves NQP
See Section 4

BENEFITS

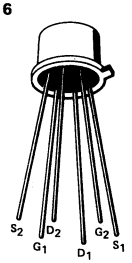
- Low Cost
- Minimum System Error and Calibration
  10 mV Offset Maximum (U410)
  70 dB Minimum CMRR (U410)
- Low Drift with Temperature
  10 μV/°C Maximum (U410)
- Simplifies Amplifier Design
  Low Output Conductance

TO-71
See Section 6





Bottom View



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-To-Gate Voltage	±40 V
Gate-Drain or Gate-Source Voltage	−40 V
Gate Current	50 mA
Total Package Dissipation (25°C Free-Air)	375 mW
Power Derating	3.0 mW/°C
Storage Temperature Range	−65 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U410			U411			U412			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-200			-200			-200	pA	V_{DS} = 0, V_{GS} = -30 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5		-3.5	-0.5		-3.5	-0.5		-3.5	V	V_{DS} = 20 V, I_D = 1 nA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-40			-40			-40			V	V_{DS} = 0 V, I_G = -1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	0.5		5.0	0.5		5.0	0.5		5.0	mA	V_{DS} = 20 V, V_{GS} = 0 V	
5	STATIC	I_G	Gate Current (Note 1)			-200			-200			-200	pA	V_{DG} = 20 V, I_D = 200 μA	
6	STATIC	V_{GS}	Gate-Source Voltage	-0.2		-3.0	-0.2		-3.0	-0.2		-3.0	V		
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1,000		4,000	1,000		4,000	1,000		4,000	μmho	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 kHz
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	600		1,200	600		1,200	600		1,200	μmho	V_{DG} = 20 V, I_D = 200 μA	f = 1 kHz
9	DYNAMIC	g_{os}	Common-Source Output Conductance			20			20			20	μmho	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 kHz
10	DYNAMIC	g_{os}	Common-Source Output Conductance			5			5			5	μmho	V_{DG} = 20 V, I_D = 200 μA	f = 1 kHz
11	DYNAMIC	C_{iss}	Common-Source Input Capacitance		4.5			4.5			4.5		pF	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 MHz
12	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			1.2			1.2		pF		
13	DYNAMIC	$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage			50			50			50	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 20 V, I_D = 200 μA	f = 100 Hz
14	MATCHING	$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage			10			20			40	mV	V_{DG} = 20 V, I_D = 200 μA	
15	MATCHING	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Drift (Note 3)			10			25			80	μV/°C	V_{DG} = 20 V, I_D = 200 μA T_A = 25°C to T_B = 85°C	
16	MATCHING	CMRR	Common-Mode Rejection Ratio (Note 4)		80			80			70		dB	V_{DD} = 10 V to V_{DD} = 20 V I_D = 200 μA	

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μsec; duty cycle ≤ 3%.
3. Measured at end points, T_A and T_B.
4. $CMRR = 20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1}-V_{GS2}\rvert}\right]$, ΔV_{DD} = 10 V.

NQP

monolithic dual n-channel JFETs *designed for . . .*

- **Very High Input Impedance Differential Amplifiers**
  - **Electrometers**
- **Impedance Converters**

Siliconix

Performance Curves NNT
See Section 4

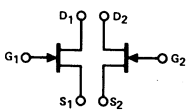
BENEFITS

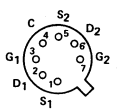
- **High Input Impedance**
  I_G = 0.25 pA Maximum (U421-3)
- **High Gain g_{fs} = 120 μmho Minimum @ I_D = 30 μA (U421-6)**
- **Low Power Supply Operation**
  $V_{GS(off)}$ = 2 V Maximum (U421-3)
- **Minimum System Error and Calibration**
  10 mV Maximum Offset
  90 dB Minimum CMRR (U421, U424)

ABSOLUTE MAXIMUM RATINGS (25°C)

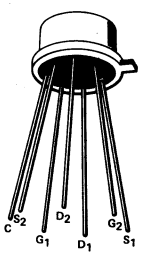
Gate-to-Gate Voltage ..... ±40 V
Gate-Drain or Gate-Source Voltage ..... -40 V
Gate Current ..... 10 mA
Device Dissipation (Each Side), T_A = 25°C
(Derate 3.2 mW/°C to 150°C) ..... 400 mW
Total Device Dissipation, T_A = 25°C
(Derate 6.0 mW/°C to 150°C) ..... 750 mW
Storage Temperature Range ..... -65°C to +150°C

TO-78
See Section 6





Bottom View



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U421-3 Min	U421-3 Typ	U421-3 Max	U424-6 Min	U424-6 Typ	U424-6 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-40	-60		-40	-60		V	I_G = -1 μA, V_{DS} = 0	
2		BV_{G1G2}	Gate-Gate Breakdown Voltage	±40			±40			V	I_G = -1 μA, I_D = 0, I_S = 0	
3		I_{GSS}	Gate Reverse Current (Note 1)			1.0			3.0	pA	T = +25°C	V_{GS} = -20 V, V_{DS} = 0
						1.0			3.0	nA	T = +125°C	
4		I_G	Gate Operating Current (Note 1)			.25			0.5	pA	T = +25°C	V_{DG} = 10 V, I_D = 30 μA
						250			500		T = +125°C	
5		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.4		-2.0	-0.4		-3.0	V	V_{DS} = 10 V, I_D = 1 nA	
6		V_{GS}	Gate-Source Voltage			-1.8			-2.9		V_{DG} = 10 V, I_D = 30 μA	
7		I_{DSS}	Saturation Drain Current	60		1000	60		1800	μA	V_{DS} = 10 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	300		1500	300		1500	μ℧	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
9		g_{os}	Common-Source Output Conductance			10			10			
10		C_{iss}	Common-Source Input Capacitance			3.0			3.0	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance			1.5			1.5			
12		g_{fs}	Common-Source Forward Transconductance	120		350	120		350	μ℧	V_{DG} = 10 V, I_D = 30 μA	f = 1 kHz
13		g_{os}	Common-Source Output Conductance			3.0			3.0			
14		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		20	70		20	70	nV/√Hz		f = 10 Hz
					10			10				f = 1 kHz
15		NF	Noise Figure			1.0			1.0	dB		f = 10 Hz, R_G = 10M Ω

		Characteristic		U421, 4 Min	U421, 4 Typ	U421, 4 Max	U422, 5 Min	U422, 5 Typ	U422, 5 Max	U423,6 Min	U423,6 Typ	U423,6 Max	Unit	Test Conditions
16	MATCH	$\lvert V_{GS1} - V_{GS2}\rvert$	Differential Gate-Source Voltage			10			15			25	mV	V_{DG} = 10 V, I_D = 30 μA
17		$\frac{\lvert V_{GS1} - V_{GS2}\rvert}{\Delta T}$	Differential Gate-Source Voltage Change With Temperature (Note 2)			10			25			40	μV/°C	V_{DG} = 10 V, I_D = 30 μA, T_A = -55°C, T_B = 25°C, T_C = 125°C
18		CMRR	Common Mode Rejection Ratio (Note 3)	90	95		80	90		80	90		dB	I_D = 30 μA, V_{DG} = 10 to 20 V

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Measured at end points T_A, T_B and T_C.
3. CMRR = $20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1} - V_{GS2}\rvert}\right]$ ΔV_{DD} = 10 V.
4. Case lead not connected.

NNT

monolithic dual n-channel JFETs *designed for . . .*

- **Very High Input Impedance Differential Amplifiers**
  - **Electrometers**
- **Impedance Converters**

Siliconix

Performance Curves NNT
See Section 4

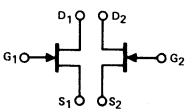
BENEFITS

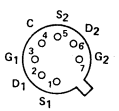
- **High Input Impedance**
  I_G = 5 pA (U427)
- **High Gain g_{fs} = 120 μmho Minimum @**
  I_D = 30 μA
- **Low Power Supply Operation**
  $V_{GS(off)}$ = 2 V Maximum (U427)
- **Minimum System Error and Calibration**
  25 mV Maximum Offset

ABSOLUTE MAXIMUM RATINGS (25°C)

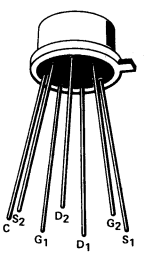
Gate-to-Gate Voltage	±40 V
Gate-Drain or Gate-Source Voltage	−40 V
Gate Current	10 mA
Device Dissipation (Each Side), T_A = 25°C (Derate 3.2 mW/°C to 150°C)	400 mW
Total Device Dissipation, T_A = 25°C (Derate 6.0 mW/°C to 150°C)	750 mW
Storage Temperature Range	−65 to +150°C

TO-78
See Section 6





Bottom View



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

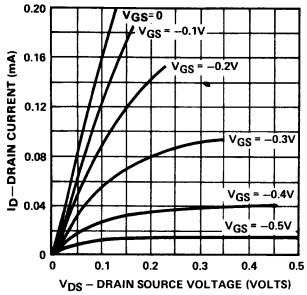
		Characteristic		U427 Min	U427 Typ	U427 Max	U428 Min	U428 Typ	U428 Max	Unit	Test Conditions
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−40	−60		−40	−60		V	I_G = −1 μA, V_{DS} = 0
2	STATIC	BV_{G1G2}	Gate-Gate Breakdown Voltage	±40			±40			V	I_G = −1 μA, I_D = 0, I_S = 0
3	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			5			10	pA	T = +25°C; V_{GS} = −20 V, V_{DS} = 0
						5			10	nA	T = +125°C
4	STATIC	I_G	Gate Operating Current (Note 1)			3			5	pA	T = +25°C; V_{DG} = 10 V, I_D = 30 μA
						3			5	nA	T = +125°C
5	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.4		−2.0	−0.4		−3.0	V	V_{DS} = 10 V, I_D = 1 nA
6	STATIC	V_{GS}	Gate-Source Voltage			−1.8			−2.9	V	V_{DG} = 10 V, I_D = 30 μA
7	STATIC	I_{DSS}	Saturation Drain Current	60		1000	60		1800	μA	V_{DS} = 10 V, V_{GS} = 0
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	300		800	300		1500	μ℧	V_{DS} = 10 V, V_{GS} = 0; f = 1 kHz
9	DYNAMIC	g_{os}	Common-Source Output Conductance			3.0			5.0	μ℧	V_{DS} = 10 V, V_{GS} = 0; f = 1 kHz
10	DYNAMIC	C_{iss}	Common-Source Input Capacitance			3.0			3.0	pF	V_{DS} = 10 V, V_{GS} = 0; f = 1 MHz
11	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance			1.5			1.5	pF	V_{DS} = 10 V, V_{GS} = 0; f = 1 MHz
12	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	120		350	120		350	μ℧	V_{DG} = 10 V, I_D = 30 μA; f = 1 kHz
13	DYNAMIC	g_{os}	Common-Source Output Conductance			0.5			1.0	μ℧	V_{DG} = 10 V, I_D = 30 μA; f = 1 kHz
14	DYNAMIC	$\overline{e_n}$	Equivalent Short Circuit Input Noise Voltage		20	50		20	70	nV/√Hz	V_{DG} = 10 V, I_D = 30 μA; f = 10 Hz
					10			10		nV/√Hz	V_{DG} = 10 V, I_D = 30 μA; f = 1 kHz
15	DYNAMIC	NF	Noise Figure			1.0			1.0	dB	V_{DG} = 10 V, I_D = 30 μA; f = 10 Hz, R_G = 10M Ω
16	MATCH	$\lvert V_{GS1} - V_{GS2}\rvert$	Differential Gate-Source Voltage			25			40	mV	V_{DG} = 10 V, I_D = 30 μA
17	MATCH	$\frac{\lvert V_{GS1} - V_{GS2}\rvert}{\Delta T}$	Differential Gate-Source Voltage Change With Temperature (Note 2)			40			80	μV/°C	V_{DG} = 10 V, I_D = 30 μA, T_A = −55°C, T_B = 25°C, T_C = 125°C
18	MATCH	CMRR	Common Mode Rejection Ratio (Note 3)		90			90		dB	I_D = 30 μA, V_{DG} = 10 to 20 V

NOTES.
1. Approximately doubles for every 10°C increase in T_A.
2. Measured at end points T_A, T_B and T_C.
3. CMRR = $20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1} - V_{GS2}\rvert}\right]$ ΔV_{DD} = 10 V.
4. Case lead not connected.

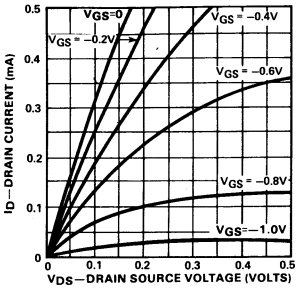
NNT

PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

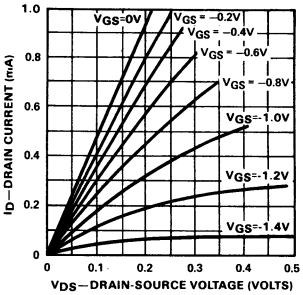
Output Characteristic
($V_{GS(off)}$ = −0.6V)



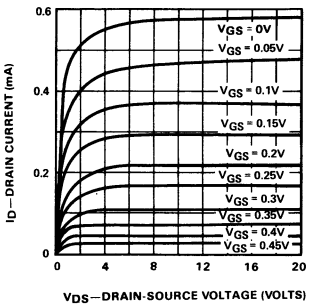
Output Characteristic
($V_{GS(off)}$ = −1.2V)



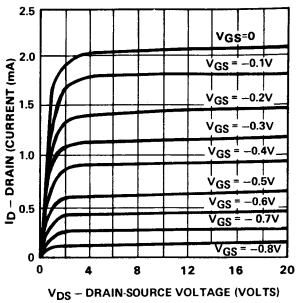
Output Characteristic
($V_{GS(off)}$ = −1.7V)



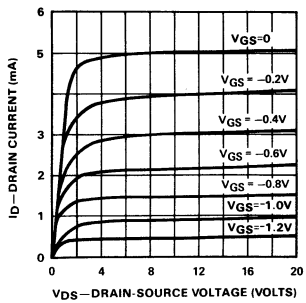
Output Characteristic
($V_{GS(off)}$ = −0.6V)



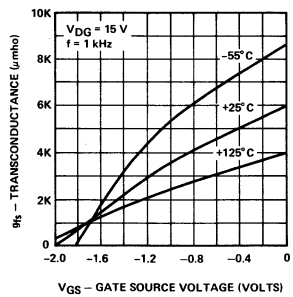
Output Characteristic
($V_{GS(off)}$ = −1.2V)



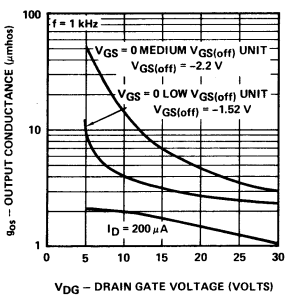
Output Characteristic
($V_{GS(off)}$ = −1.7V)



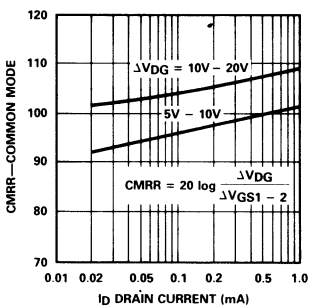
Transconductance vs Gate Source Voltage
Medium $V_{GS(off)}$ Unit (−2.0V)

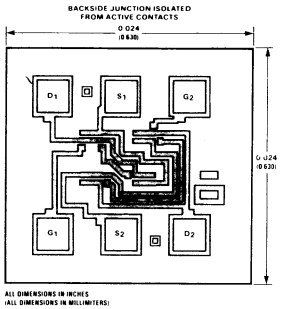


Output Conductance
vs Drain Gate Voltage



CMRR vs Drain Current





monolithic dual n-channel JFETs

designed for . . .

- Low Leakage FET Input Op Amps
- pH Meters
- Electrometers

BENEFITS:

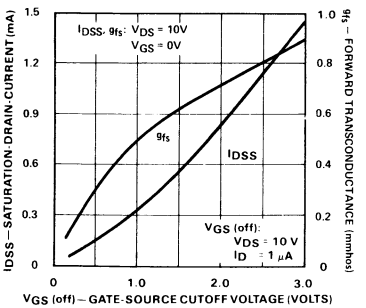
- Ultra-High Input Impedance
- Good Voltage Gain
- Low Noise

TYPE	PACKAGE	PRINCIPAL DEVICES
Dual	TO-78	U421-28
Dual	Chip	U423CHP-428CHP

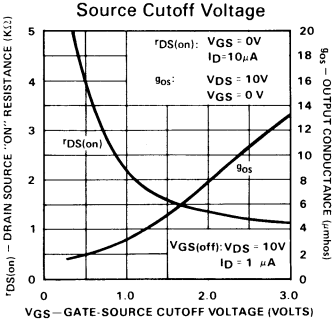
Improved Replacement for
2N5902-9 Series

PERFORMANCE CURVES (25°C unless otherwise noted)

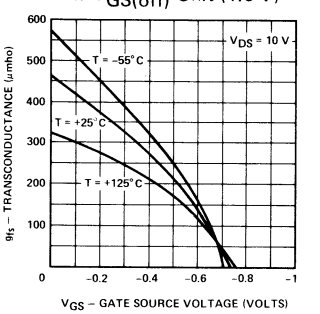
Drain Current & Transconductance vs Gate Source Cutoff Voltage



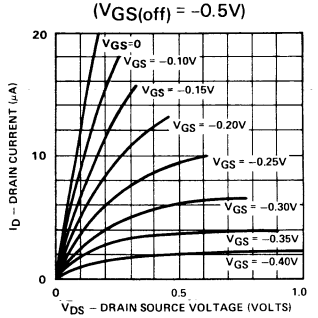
On Resistance & Output Conductance vs Gate-Source Cutoff Voltage



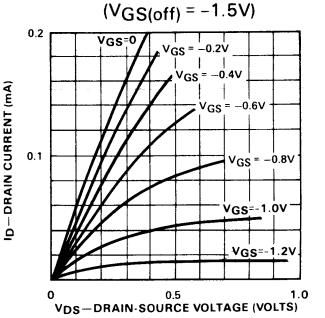
Transconductance vs Gate Source Voltage Low $V_{GS(off)}$ Unit (1.0 V)



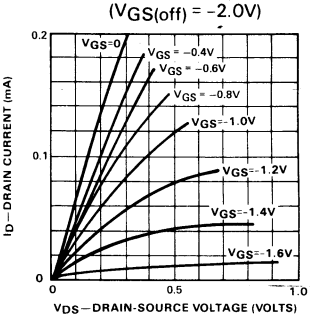
Output Characteristic ($V_{GS(off)}$ = -0.5V)



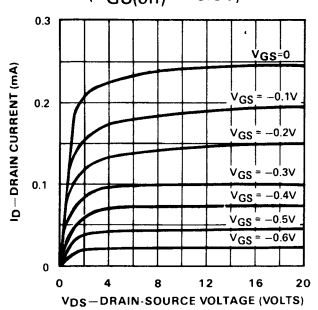
Output Characteristic ($V_{GS(off)}$ = -1.5V)



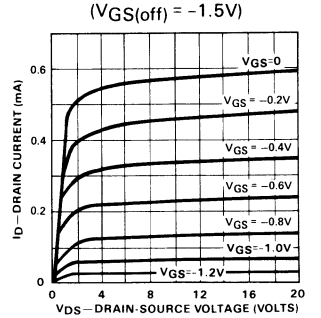
Output Characteristic ($V_{GS(off)}$ = -2.0V)



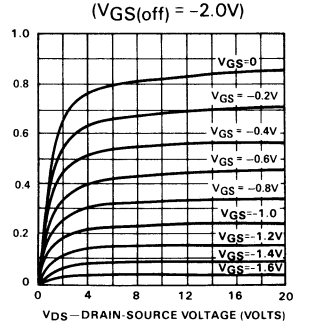
Output Characteristic ($V_{GS(off)}$ = -0.5V)



Output Characteristic ($V_{GS(off)}$ = -1.5V)

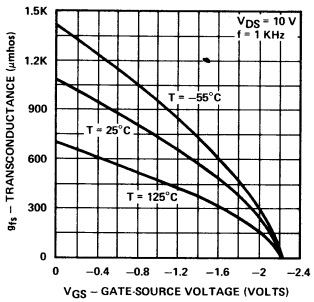


Output Characteristic ($V_{GS(off)}$ = -2.0V)

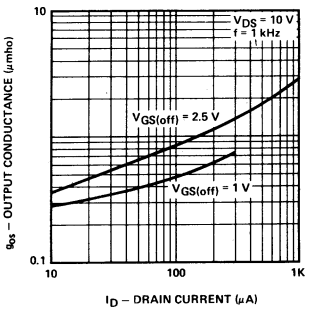


PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

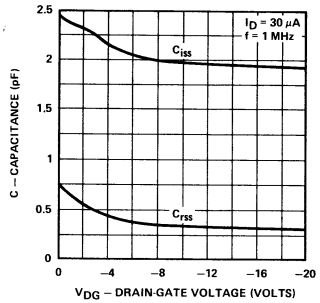
Transconductance vs Gate Source Voltage
High $V_{GS(off)}$ Unit (2.5 V)



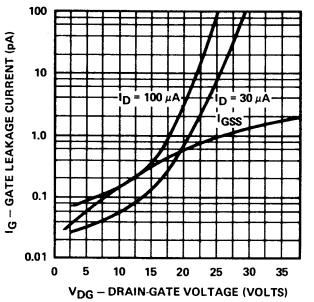
Common-Source Output Conductance vs Drain Current



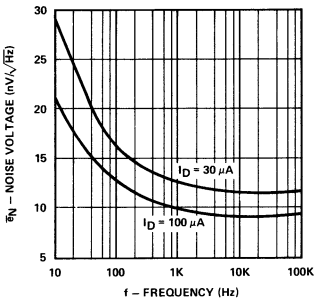
Capacitance vs Drain Gate Voltage



Gate Operating Current vs Drain-Gate Voltage



Equivalent Input Noise Voltage vs Frequency



CMRR vs Drain Current