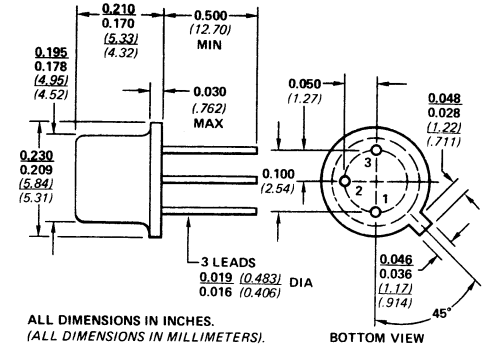
Performance Curves NC NP NT PE PF PJ

See Pages 4-23, 37, 45, 57, 58, 59

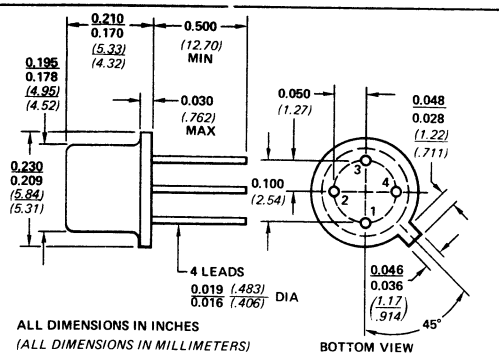
N-CHANNEL AND P-CHANNEL JUNCTION VOLTAGE-CONTROLLED RESISTOR FETS

VOLTAGE-VARIABLE RESISTORS FOR SMALL-SIGNAL ATTENUATORS, FILTERS, AND AMPLIFIER GAIN CONTROL

- Two Types, Positive and Negative Voltage Control
- High Impedance Control Terminal

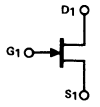


TO-18



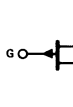
TO-72

VCR2N,4N



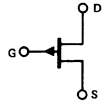
PIN	OUT
1	S
2	D
3	G,C

VCR6P



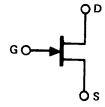
PIN	OUT
1	S
2	G,C
3	D

VCR3P, 5P



PIN	OUT
1	S
2	G
3	D
4	C

VCR7N



PIN	OUT
1	D
2	S
3	G
4	C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

N-Channel VCR FETs

		Characteristic		VCR2N Min	VCR2N Max	VCR4N Min	VCR4N Max	VCR7N Min	VCR7N Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-5		-0.2		-0.1	nA	V_{GS} = -15 V, V_{DS} = 0	
2	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-15		-15		-15		V	I_G = -1 μA, V_{DS} = 0	
3	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-3.5	-7	-3.5	-7	-2.5	-5.0	V	I_D = 1 μA, V_{DS} = 10 V	
4	STATIC	$r_{ds(on)}$	Drain Source ON Resistance	20	60	200	600	4000	8000	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
5	DY	C_{dgo}	Drain-Gate Capacitance		7.5		3		1.5	pF	V_{GD} = -10 V, I_S = 0	f = 1 MHz
6	DY	C_{sgo}	Source-Gate Capacitance		7.5		3		1.5	pF	V_{GS} = -10 V, I_D = 0	f = 1 MHz
					NC		NP		NT			

P-Channel VCR FETs

				VCR3P		VCR5P		VCR6P				
1	STATIC	I_{GSS}	Gate Reverse Current		20		10		50	nA	V_{GS} = 15 V, V_{DS} = 0	
2	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	15		15		15		V	I_G = 1 μA, V_{DS} = 0	
3	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	3.5	7	3.5	7	2	4	V	I_D = -1 μA, V_{DS} = -10 V	
4	STATIC	$r_{ds(on)}$	Drain-Source ON Resistance	70	200	300	900	400	900	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
5	DY	C_{dgo}	Drain-Gate Capacitance		6		3		25	pF	V_{GD} = 10 V, I_S = 0	f = 1 MHz
6	DY	C_{sgo}	Source-Gate Capacitance		6		3		25	pF	V_{GS} = 10 V, I_D = 0	f = 1 MHz
					PE		PF		PJ			

APPLICATIONS

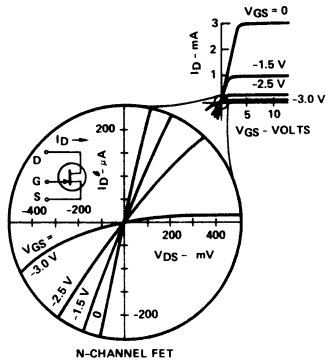


Fig. 1

P-Channel FET Output Characteristic Enlarged Around V_{DS} = 0

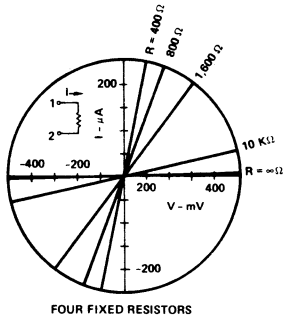


Fig. 2

V-I Characteristic of Four Fixed Resistors

The VCR FET has an a-c drain-source resistance, evaluated around V_{DS} = 0, that is controlled by d-c bias voltage V_{GS} applied to the high-impedance gate terminal. Minimum r_{ds} occurs when V_{GS} = 0 and, as V_{GS} approaches the pinch-off voltage, r_{ds} rapidly increases. Comparing Fig. 1 and 2, for $V_{DS} < \pm 0.1$ volt and V_{GS} = constant, the VCR FET has a bilateral characteristic with no offset voltage, just like a fixed resistor. However, when $V_{DS} > \pm 0.1$ volts, the VCR FET characteristic has noticeable curvature.

This series of junction FETs is intended for applications where the drain-source voltage is a low-level a-c signal with no d-c component. Thus the FET operating point will swing symmetrically around V_{DS} = 0. In the first quadrant, signal distortion depends on what extent the FET output characteristic deviates from a straight line or linear relation. Besides the linearity problem in the third quadrant, when V_{GS} is near zero and $v_{ds} > 0.5$ volt rms, the gate-channel junction will become forward biased and cause additional curvature in the characteristic. Also, whenever the gate becomes forward biased due to any combination of V_{GS} and v_{ds}, it ceases to be a high-impedance control terminal for the VCR.

Fig. 3 presents a normalized plot of r_{DS} versus normalized V_{GS} where V_P' is defined as that value of V_{GS} at I_D/I_{DSS} = 0.001. The dynamic range of r_{DS} is shown as greater than 100:1. For best control of r_{DS} the normalized V_{GS} should lie between 0 and 0.8 V_P because as V_{GS} approaches V_P, r_{DS} increases very rapidly so that r_{ds} control becomes very critical and unit-to-unit matching is almost impossible. In Fig. 4, $r_{ds(on)}$ (drain-source resistance at $V_{DS} = V_{GS} = 0$) varies as an inverse function of V_P. In Fig. 5 r_{ds} has a typical 0.7%/°C temperature coefficient for P-channels which

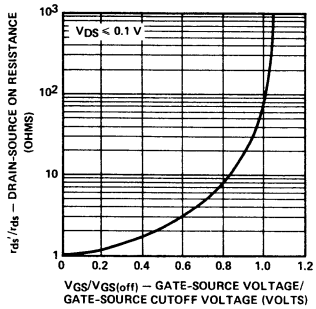


Fig. 3

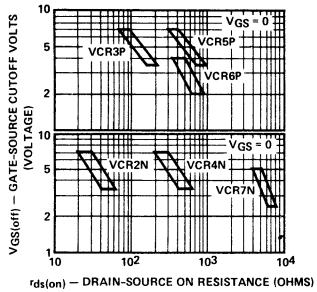


Fig. 4

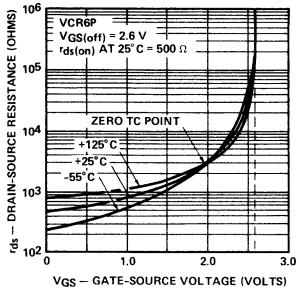


Fig. 5

decreases as V_{GS} approaches the zero t.c. point. N-channel devices have a typical 0.3%/°C t.c. Specific bias voltage to set operation at the zero t.c. point varies, as does V_P, from device to device.*

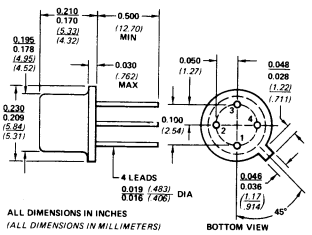
* L. Evans; "Biasing FETs for Zero DC Drift"; Electro Technology, August 1964.

Performance Curves NS
See Page 4-43

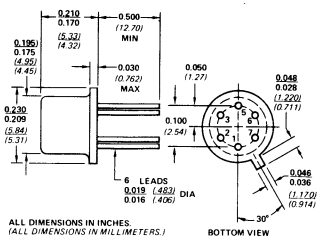
N-CHANNEL JUNCTION VOLTAGE-CONTROLLED RESISTOR FETS

SINGLE, MATCHED PAIR, AND MATCHED QUAD VOLTAGE-VARIABLE RESISTORS FOR SMALL-SIGNAL ATTENUATORS, FILTERS, AND AMPLIFIER GAIN CONTROL

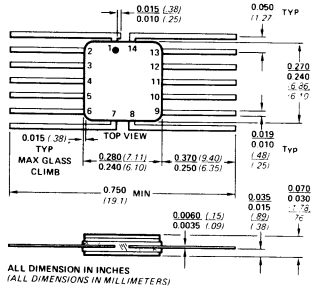
- Large Control Range, V_P = 20 V Typical
- Matched Resistance From 200 Ω to 2 kΩ
- High Impedance Control Terminal



TO-72



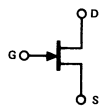
TO-71



TO-86

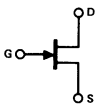
VCR10N

PIN	OUT
1	S
2	D
3	G
4	C



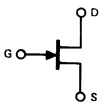
VCR11N

PIN	OUT
1	S_1
2	D_1
3	G_1
5	S_2
6	D_2
7	G_2



VCR12N, 13N

PIN	OUT	PIN	OUT
1	NC	8	D_4
2	G_1	9	S_3
3	G_2	10	D_3
4	G_3	11	S_2
5	G_4	12	D_2
6	NC	13	S_1
7	S_4	14	D_1



PERFORMANCE CURVES (25°C unless otherwise noted)

		Characteristic	VCR10N VCR11N VCR12N VCR13N Min	VCR10N VCR11N VCR12N VCR13N Max	Unit	Test Conditions	
1	STATIC	I_{GSS} Gate Reverse Current		-0.25	nA	V_{GS} = -15 V, V_{DS} = 0	
2	STATIC	BV_{GSS} Gate Reverse Breakdown Voltage	-25		V	I_G = -1 μA, V_{DS} = 0	
3	STATIC	$V_{GS(off)}$ Gate-Source Cutoff Voltage	-8	-12	V	I_D = 1 μA, V_{DS} = 10 V	
4	STATIC	$r_{ds(on)}$ Drain Source ON Resistance	100	200	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
5	DYNAMIC	C_{dgo} Drain-Gate Capacitance		6	pF	V_{GS} = -10 V, I_S = 0	f = 1 MHz
6	DYNAMIC	C_{sgo} Source-Gate Capacitance		6	pF	V_{GD} = -10 V, I_D = 0	f = 1 MHz

		Characteristic	VCR11N Min	VCR11N Max	VCR12N Min	VCR12N Max	VCR13N Min	VCR13N Max	Unit	Test Conditions	
7	MATCHING	$\frac{r_{DS(min)}}{r_{DS(max)}}$	0.95	1						V_{DS} = 100 mV, V_{GS1}[1] = V_{GS2}	r_{DS1} = 200 Ω
8	MATCHING	$\frac{r_{DS(min)}}{r_{DS(max)}}$	0.95	1						V_{DS} = 100 mV, V_{GS1}[1] = V_{GS2}	r_{DS1} = 2 kΩ
9	MATCHING	$\frac{r_{DS(min)}}{r_{DS(max)}}$			0.90	1				V_{DS} = 100 mV, V_{GS1}[1] = V_{GS2} = V_{GS3} = V_{GS4}	r_{DS1} = 200 Ω
10	MATCHING	$\frac{r_{DS(min)}}{r_{DS(max)}}$			0.90	1				V_{DS} = 100 mV, V_{GS1}[1] = V_{GS2} = V_{GS3} = V_{GS4}	r_{DS1} = 2 kΩ
11	MATCHING	$\frac{r_{DS(min)}}{r_{DS(max)}}$					0.95	1		V_{DS} = 100 mV, V_{GS1}[1] = V_{GS2} = V_{GS3} = V_{GS4}	r_{DS1} = 200 Ω
12	MATCHING	$\frac{r_{DS(min)}}{r_{DS(max)}}$					0.95	1		V_{DS} = 100 mV, V_{GS1}[1] = V_{GS2} = V_{GS3} = V_{GS4}	r_{DS1} = 2 kΩ

Note:
1 V_{GS1} = Control voltage necessary to force r_{DS1} to 200 Ω or 2 kΩ.

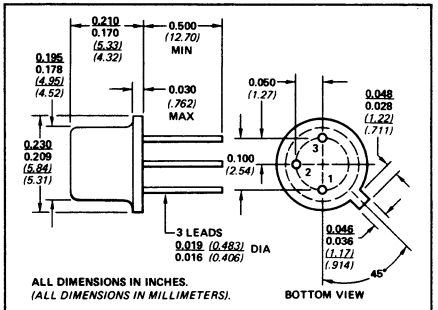
NS

Performance Curves NP
See Page 4-37

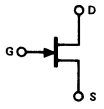
N-CHANNEL JUNCTION VOLTAGE-CONTROLLED RESISTOR FET

VOLTAGE-VARIABLE RESISTORS FOR SMALL-SIGNAL ATTENUATORS, FILTERS, AND AMPLIFIER GAIN CONTROL

- High Impedance Control Terminal



TO-18



PIN	OUT
1	S
2	D
3	G,C

2

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristics		Min	Max	Unit	Test Conditions	
1	S T	I_{GSS}	Gate Reverse Current		-1	nA	V_{GS} = -25 V, VDS = 0	
2		BV_{GSS}	Gate-Source Breakdown Voltage	-30		V	V_{DS} = 0, I_G = -1 μA	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-15	-25		V_{DS} = 5 V, I_D = 1 μA	
4	D Y	$r_{DS(on)}$	Drain-Source ON Resistance	80	160	Ω	V_{GS} = 0, V_{DS} = 0	f = 1 kHz
5		C_{dgo}	Drain-Gate ON Capacitance		3	pF	V_{DG} = 20 V	f = 1 MHz
6		C_{sgo}	Source-Gate ON Capacitance		3			

NP