n-channel enhancement-mode VMOS Power FETs *designed for . . .*

Siliconix

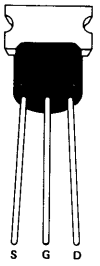
Performance Curves VNML, VNMK
See Section 3

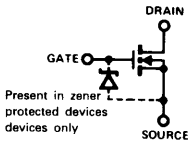
- **High Speed Line Drivers**
- **TTL to High Current Interface**
- **CMOS to High Current Interface**
- **Transformer Drivers**
- **Relay Drivers**
- **LED Digit Strobe Drivers**

BENEFITS

- Directly Interfaces to CMOS, TTL, DTL and MOS Logic Families
- Permits More Efficient and Compact Switching Designs
- Reduces Component Count and Design Time/Effort
  - Drives Inductive Loads Directly
  - Fan Out From CMOS Logic > 100
  - Easily Paralleled with Inherent Current Sharing Capability
  - High Gain
- Improves Reliability
  - Free From Secondary Breakdown Failures and Voltage Derating
  - Current Decreases as Temperature Increases
  - Input Protected From Static Discharge

M — Package
TO-237
(TO-92 PLUS)





ABSOLUTE MAXIMUM RATINGS

Maximum Drain-Source Voltage	100 V
Maximum Drain-Gate Voltage	100 V
Maximum Continuous Drain Current	0.5 A
Maximum Pulsed Drain Current	1.0 A
Maximum Continuous Forward Gate Current	0.5 mA
Maximum Pulsed Forward Gate Current (Note 1)	10 mA
Maximum Continuous Reverse Gate Current	10 mA
Maximum Forward Gate-Source Voltage *(15V see note 3)*	30V
Maximum Reverse Gate-Source Voltage *(0.3V see note 3)*	30V
Maximum Dissipation at 25°C Ambient Temperature[2]	1 W
Linear Derating Factor	8 mW/°C
Maximum Junction Temperatures	−40°C to +150°C
Maximum Storage Temperatures	−40°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

NOTE:

1. Pulse Test — 80 μs pulse, 1% duty cycle.

2. Power dissipation measured with device soldered to a minimum of 1 square inch of 2 ounce copper clad board and with a lead length ≤ 1/8 inch.

3. Lower voltage applies to zener protected devices which will be discontinued after 31 December, 1981.

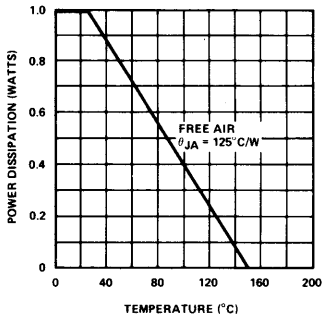
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	BV_{DSS}	Drain-Source Breakdown	100			V	V_{GS} = 0 V, I_D = 100 μA	
2		$V_{GS(th)}$	Gate Threshold Voltage			2.0	V	V_{DS} = V_{GS}, I_D = 15mA	
3		I_{GSS}	Gate-Body Leakage			10	μA	V_{GS} = 10 V, V_{DS} =0	Note 2
4		I_{DSS}	Zero Gate Voltage Drain Current			10	μA	V_{DS} = 60 V, V_{GS} =0	
5		$I_{D(on)}$	ON-State Drain Current	0.25			A	V_{DS} = 25 V, V_{GS} = 5 V	Note 1
6				0.50				V_{DS} = 25 V, V_{GS} = 10 V	
7		$V_{DS(on)}$	Drain-Source ON Voltage			1.2	V	V_{GS} = 5 V, I_D = 120mA	
8	DYNAMIC	g_{fs}	Forward Transconductance	100	200		m℧	V_{DS} = 15 V, I_D = 0.5 A	
9		C_{iss}	Input Capacitance		48		pF	V_{DS} = 25 V, f = 1 MHz	Note 2
10		C_{oss}	Output Capacitance		16				
11		C_{rss}	Feedback Capacitance		2				
12		t_{ON}	Turn-ON Time		10		ns	See Test Circuit for **VNML**, VNMK (Section 3)	
13		t_{OFF}	Turn-OFF Time		10				

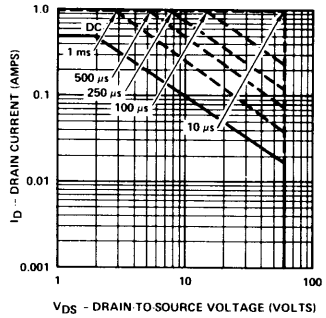
NOTES: 1. Pulse test – 80 μs pulse, 1% duty cycle.
2. Sample test.

VNML, VNMK

Power Dissipation vs Case or Ambient Temperature



DC Safe Operating Region
T_A = 25°C



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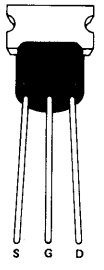

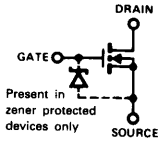

ABSOLUTE MAXIMUM RATINGS

Maximum Drain-Source Voltage	30 V
Maximum Drain-Gate Voltage	30 V
Maximum Continuous Drain Current	0.5 A
Maximum Pulsed Drain Current	1.0 A
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Maximum Forward Gate-Source Voltage *(15V see note 3)*	30V
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ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	BV_{DSS}	Drain-Source Breakdown	30			V	V_{GS} = 0 V, I_D = 100 μA	
2		$V_{GS(th)}$	Gate Threshold Voltage			2.0	V	V_{DS} = V_{GS}, I_D = 5mA	
3		I_{GSS}	Gate-Body Leakage			10	μA	V_{GS} = 10 V, V_{DS} =0	Note 2
4		I_{DSS}	Zero Gate Voltage Drain Current			10	μA	V_{DS} = 30 V V_{GS} =0	
5		$I_{D(on)}$	ON-State Drain Current	0.25			A	V_{DS} = 25 V, V_{GS} = 5 V	Note 1
6				0.50				V_{DS} = 25 V, V_{GS} = 10 V	
7		$V_{DS(on)}$	Drain-Source ON Voltage			2.5	V	V_{GS} = 10 V, I_D = 0.5 A	
8	DYNAMIC	g_{fs}	Forward Transconductance	100	200		m℧	V_{DS} = 15 V, I_D = 0.5 A	
9		C_{iss}	Input Capacitance		48		pF	V_{DS} = 25 V, f = 1 MHz	Note 2
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NOTES: 1. Pulse test – 80 μs pulse, 1% duty cycle.
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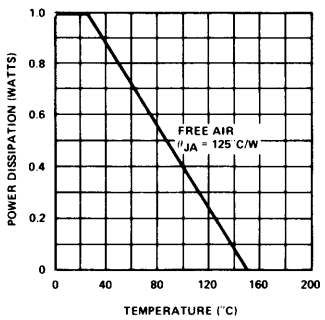

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