VNL001A ■ VNM001A ■ VNN002A ■ VNP002A

Siliconix

500V N-Channel Enhancement Mode MOSPOWER

These power FETs are designed especially for offline switching regulators, converters, solenoid and relay drivers.

FEATURES

- 200°C Rating
- High Voltage
- No Second Breakdown
- High Input Impedance
- Internal Drain-Source Diode
- Very Rugged: Excellent SOA
- Extremely Fast Switching

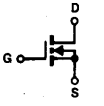
BENEFITS

- Reduced Component Count
- Improved Performance
- Simpler Designs
- Improved Reliability

200°C RATING

Product Summary

Part Number	PRO ELECTRON Part Number	BV_{DSS}	$R_{DS(on)}$	I_D	Package
VNL001A	BUP68	350V	1Ω	8A	TO-3
VNM001A	BUP69	400V			
VNN002A	BUP70	450V	1.5Ω	6.5A	
VNP002A	BUP71	500V			



ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Drain-Source Voltage
- VNL001A 350V
- VNM001A 400V
- VNN002A 450V
- VNP002A 500V

Drain-Gate Voltage
- VNL001A 350V
- VNM001A 400V
- VNN002A 450V
- VNP002A 500V

Drain Current
- Continuous[1]
  - VNL001A, VNM001A ..... ± 8.0A
  - VNN002A, VNP002A ..... ± 6.5A
- Pulsed[2]
  - VNL001A, VNM001A ..... ± 16A
  - VNN002A, VNP002A ..... ± 10A

Gate Current (Peak) ..... ± 3A

Gate-Source Voltage ..... ± 40V

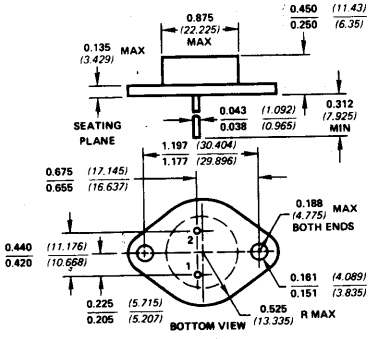
Total Power Dissipation 175W

Linear Derating Factor ..... 1.0W/°C

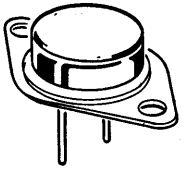
Storage and Junction Temperature ..... – 55 to 200°C

Notes:
1. Limited by package dissipation.
2. Pulse test—80μs to 300μs, 1% duty cycle.

PACKAGE DIMENSIONS



PIN 1 — Gate
PIN 2 — Source
CASE — Drain



ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Parameter		Part Number	Min	Max	Unit	Test Conditions
Static						
BV_{DSS}	Drain-Source Breakdown	VNL001A	350		V	V_{GS} = 0, I_D = 1 mA
		VNM001A	400			
		VNN002A	450			
		VNP002A	500			
$V_{GS(th)}$	Gate Threshold Voltage	All	3	6		V_{GS} = V_{DS}, I_D = 1 mA
I_{GSS}	Gate Body Leakage	All		100	nA	V_{GS} = 30V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current	All		1	mA	V_{DS} = Rated V_{DS}, V_{GS} = 0
				2.5		V_{DS} = Rated V_{DS}, V_{GS} = 0, T_C = 150°C
$V_{DS(on)}$	Drain-Source Saturation Voltage	VNL001A VNM001A		2	V	V_{GS} = 10V, I_D = 2A (Note 1)
		VNN002A VNP002A		3		
$r_{DS(on)}$	Drain-Source On Resistance	VNL001A VNM001A		1	Ω	V_{GS} = 10V, I_D = 2A (Note 1)
		VNN002A VNP002A		1.5		
$I_{D(on)}$	On-State Drain Current	All	8		A	V_{DS} = 30V, V_{GS} = 10V (Note 1)
Dynamic						
g_{fs}	Forward Transconductance	All	2.5		mS	V_{DS} = 30V, I_D = 2A (Note 1)
C_{iss}	Input Capacitance	All		1000	pF	V_{GS} = 0, V_{DS} = 30V, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance	All		40		
C_{oss}	Common-Source Output Capacitance	All		220		
$t_{d(on)}$	Turn-On Delay Time	All		50	ns	V_{DD} = 200V, I_D≈2A, R_L = 100Ω, R_g = 10Ω, (Figure 1)
t_r	Rise Time	All		50		
$t_{d(off)}$	Turn-Off Delay Time	All		100		
t_f	Fall Time	All		100		
Drain-Source Diode Characteristics						
			Typ			
V_{SD}	Forward On Voltage	All	−1.2		V	I_S = −4A, V_{GS} = 0 (Note 1)
t_{rr}	Reverse Recovery Time	All	400		ns	I_F = I_R = 4A, V_{GS} = 0 (Figure 2)

Note:
1. Pulse test—80μs to 300μs, 1% duty cycle.

Refer to VNDA / 200°C Design Curves (See Section 4)

TEST CIRCUITS

FIGURE 1 Switching Test Circuit

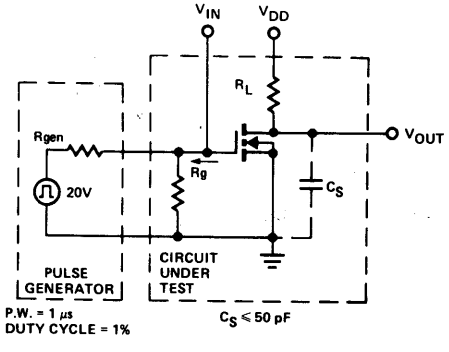
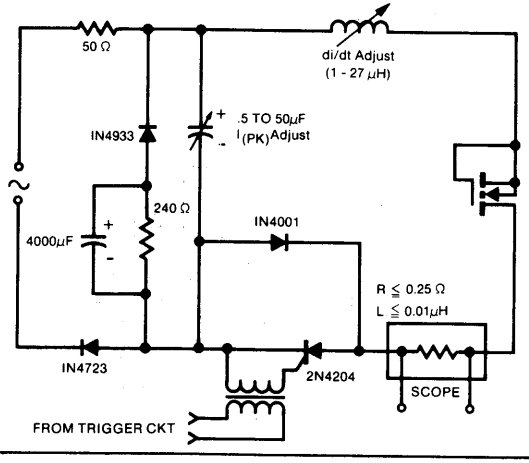


FIGURE 2 JEDEC Reverse Recovery Circuit



Siliconix incorporated

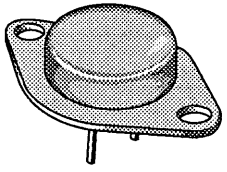
MOSPOWER

VNT008A, VNS008A VNT009A, VNS009A

N-Channel Enhancement Mode Transistors

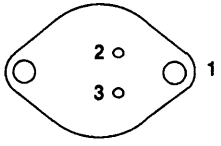
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
VNT008A	650	1.5	5.77
VNS008A	600	1.5	5.77
VNT009A	650	2.0	5.0
VNS009A	600	2.0	5.0



TO-204AA (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	VNT 008A	VNS 008A	VNT 009A	VNS 009A	Units
Drain-Source Voltage		V_{DS}	650	600	650	600	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	
Continuous Drain Current	T_C = 25°C	I_D	5.77	5.77	5.0	5.0	A
	T_C = 100°C		3.65	3.65	3.16	3.16	
Pulsed Drain Current[1]		I_{DM}	15	15	14	14	
Avalanche Current (see figure 9)		I_A	5.77	5.77	5.0	5.0	
Power Dissipation	T_C = 25°C	P_D	125	125	125	125	W
	T_C = 100°C		50	50	50	50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.0	K/W
Junction-to-Ambient	R_{thJA}	-	80	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 2000 µA	VNT008A, VNT009A VNS008A, VNT009A	$V_{(BR)DSS}$	650 600	– –	– –	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1000 µA		$V_{GS(th)}$	2.0	–	4.0	
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	2000	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	2000	
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	VNT008A, VNS008A VNT009A, VNS009A	$I_{D(on)}$	5.7 5.7	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.0 A	VNT008A, VNS008A VNT009A, VNS009A	$r_{DS(on)}$	– –	1.2 1.7	1.5 2.0	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.0 A, T_J = 125°C	VNT008A, VNS008A VNT009A, VNS009A	$r_{DS(on)}$	– –	2.4 3.4	3.75 6.0	
Forward Transconductance[2] V_{DS} = 15 V, I_D = 3.0 A		g_{fs}	3.0	3.3	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	1200	1500	pF
Output Capacitance		C_{oss}	–	140	150	
Reverse Transfer Capacitance		C_{rss}	–	40	50	
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 5.7 A (Gate charge is essentially independent of operating temperature)	Q_g	–	53	75	nC
Gate-Source Charge		Q_{gs}	–	12.9	–	
Gate-Drain Charge		Q_{gd}	–	26	–	
Turn-On Delay Time	V_{DD} = 325 V, R_L = 130Ω I_D ≅ 2.5 A, V_{GEN} = 10 V R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	15	20	ns
Rise Time		t_r	–	20	25	
Turn-Off Delay Time		$t_{d(off)}$	–	80	85	
Fall Time		t_f	–	45	50	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	VNT008A, VNS008A VNT009A, VNS009A	I_S	– –	– –	5.77 5.0	A
Pulsed Current[1]	VNT008A, VNS008A VNT009A, VNS009A	I_{SM}	– –	– –	15 14	
Forward Voltage[2] I_F = I_S, V_{GS} = 0	VNT008A, VNS008A VNT009A, VNS009A	V_{SD}	– –	– –	2.5 2.0	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs		t_{rr}	–	400	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs		Q_{rr}	–	2.5	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

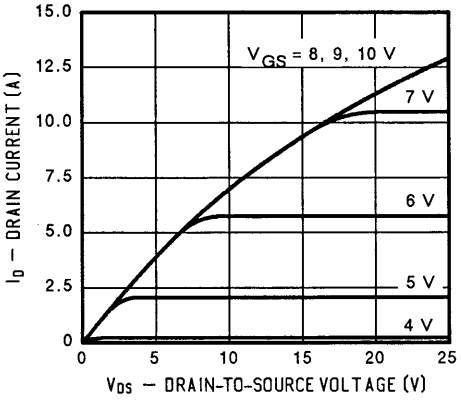


FIGURE 2: Typical Transfer Characteristics

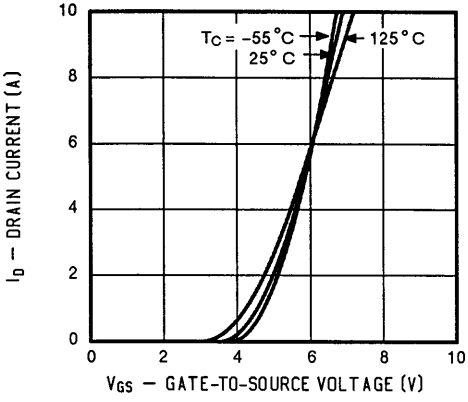


FIGURE 3: Typical Transconductance

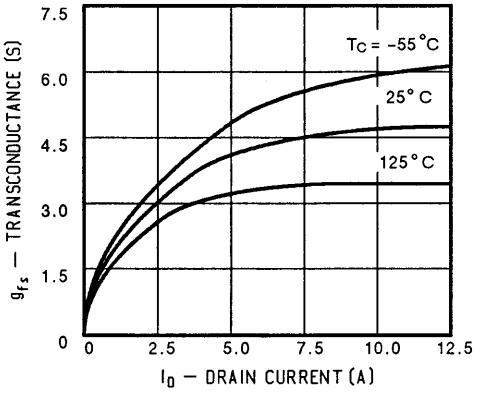


FIGURE 4: Typical On-Resistance

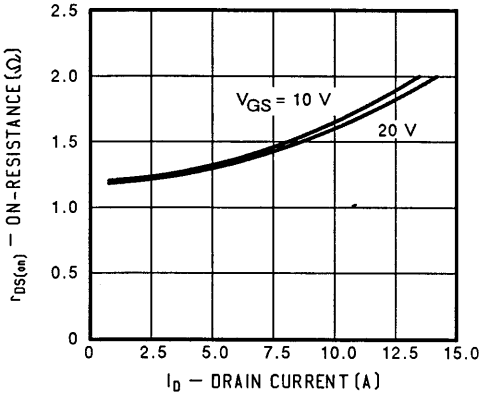


FIGURE 5: Typical Capacitance

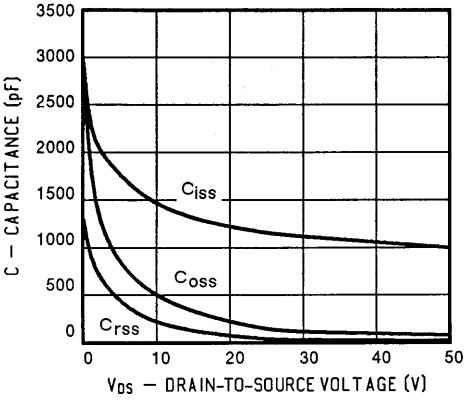
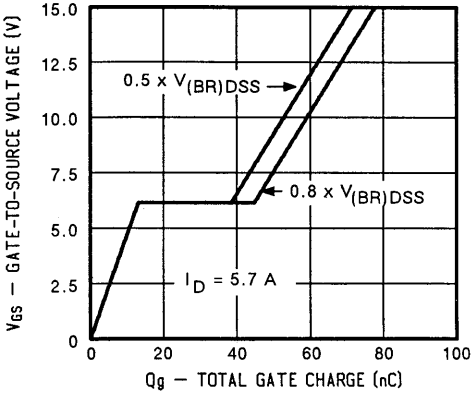


FIGURE 6: Typical Gate Charge



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Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

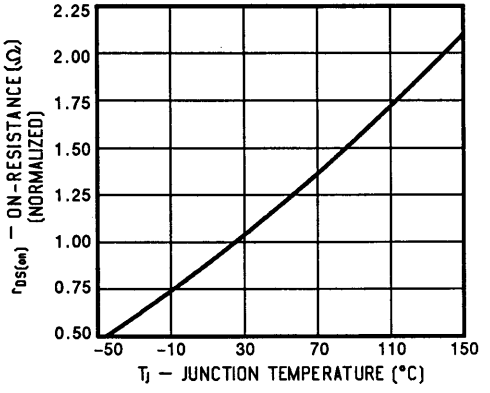


FIGURE 8: Typical Source-Drain Diode Forward Voltage

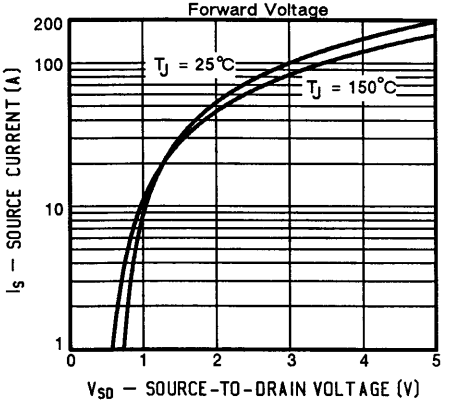


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

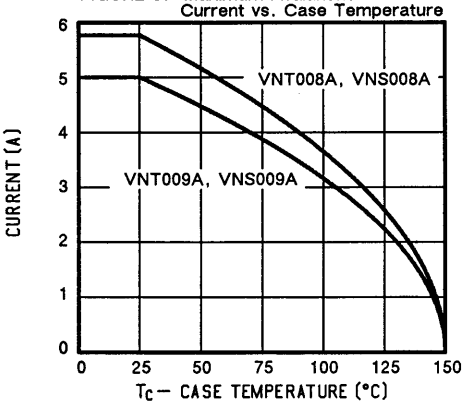
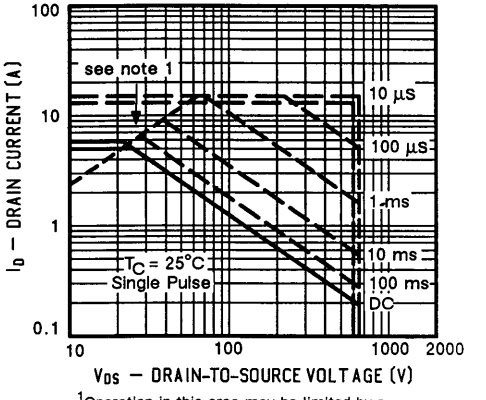
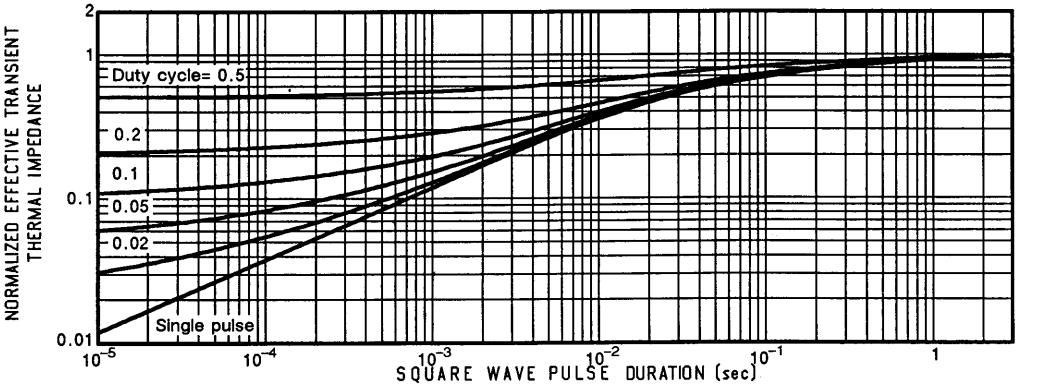


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case



Siliconix incorporated

MOSPOWER

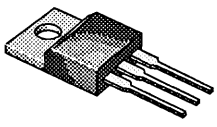
VNT008D, VNS008D
VNT009D, VNS009D

N-Channel Enhancement Mode Transistors

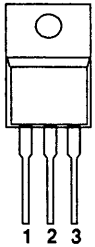
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
VNT008D	650	1.5	5.77
VNS008D	600	1.5	5.77
VNT009D	650	2.0	5.0
VNS009D	600	2.0	5.0

TO-220AB



TOP VIEW



1 GATE
2 DRAIN
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C= 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	VNT 008D	VNS 008D	VNT 009D	VNS 009D	Units
Drain-Source Voltage		V_{DS}	650	600	650	600	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	± 40	
Continuous Drain Current	T_C = 25°C	I_D	5.77	5.77	5.0	5.0	A
	T_C = 100°C		3.65	3.65	3.16	3.16	
Pulsed Drain Current[1]		I_{DM}	15	15	14	14	
Avalanche Current (see figure 9)		I_A	5.77	5.77	5.0	5.0	
Power Dissipation	T_C = 25°C	P_D	125	125	125	125	W
	T_C = 100°C		50	50	50	50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	1.0	K/W
Junction-to-Ambient	R_{thJA}	-	80	
Case-to-Sink	R_{thCS}	1.0	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 2000 µA	VNT008D, VNT009D VNS008D, VNS009D	$V_{(BR)DSS}$	650 600	– –	– –	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 1000 µA		$V_{GS(th)}$	2.0	–	4.0	
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	–	–	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	–	–	2000	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	–	–	2000	
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	VNT008D, VNS008D VNT009D, VNS009D	$I_{D(on)}$	5.7 5.7	– –	– –	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.0 A	VNT008D, VNS008D VNT009D, VNS009D	$r_{DS(on)}$	– –	1.2 1.7	1.5 2.0	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 3.0 A, T_J = 125°C	VNT008D, VNS008D VNT009D, VNS009D	$r_{DS(on)}$	– –	2.4 3.4	3.75 6.0	
Forward Transconductance[2] V_{DS} = 15 V, I_D = 3.0 A		g_{fs}	3.0	3.3	–	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	–	1200	1500	pF
Output Capacitance		C_{oss}	–	140	150	
Reverse Transfer Capacitance		C_{rss}	–	40	50	
Total Gate Charge	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 5.7 A (Gate charge is essentially independent of operating temperature)	Q_g	–	53	65	nC
Gate-Source Charge		Q_{gs}	–	12.9	–	
Gate-Drain Charge		Q_{gd}	–	26	–	
Turn-On Delay Time	V_{DD} = 325 V, R_L = 130Ω I_D = 2.5 A, V_{GEN} = 10 V R_G = 4.7Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	–	15	20	ns
Rise Time		t_r	–	20	25	
Turn-Off Delay Time		$t_{d(off)}$	–	80	85	
Fall Time		t_f	–	45	50	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	VNT008D, VNS008D VNT009D, VNS009D	I_S	– –	– –	5.77 5.0	A
Pulsed Current[1]	VNT008D, VNS008D VNT009D, VNS009D	I_{SM}	– –	– –	15 14	
Forward Voltage[2] I_F = I_S, V_{GS} = 0	VNT008D, VNS008D VNT009D, VNS009D	V_{SD}	– –	– –	2.5 2.0	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs		t_{rr}	–	400	–	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs		Q_{rr}	–	2.5	–	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 1: Typical Output Characteristics

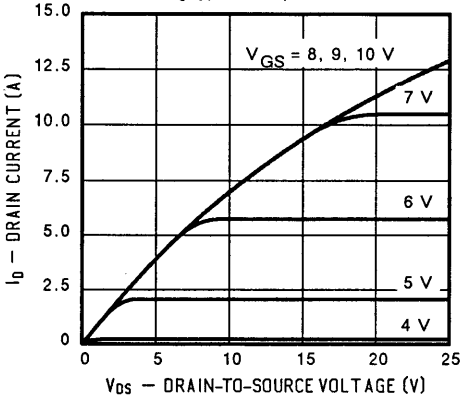


FIGURE 2: Typical Transfer Characteristics

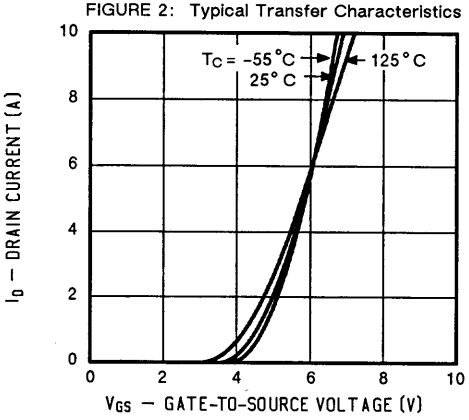


FIGURE 3: Typical Transconductance

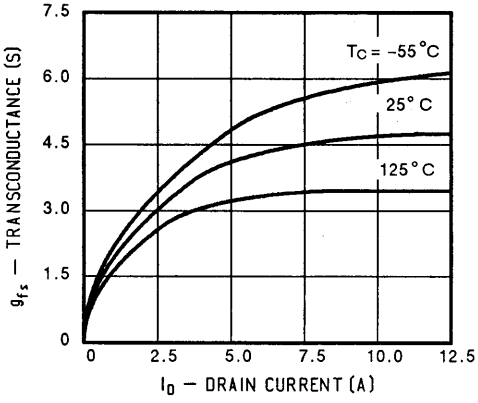


FIGURE 4: Typical On-Resistance

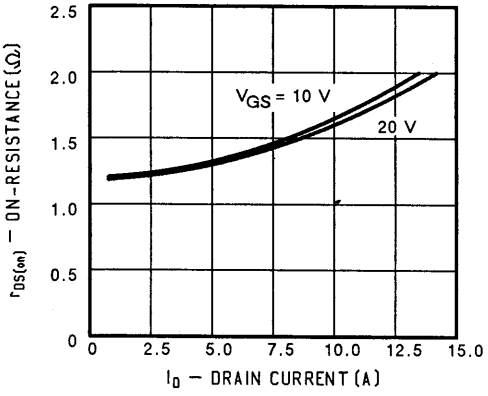


FIGURE 5: Typical Capacitance

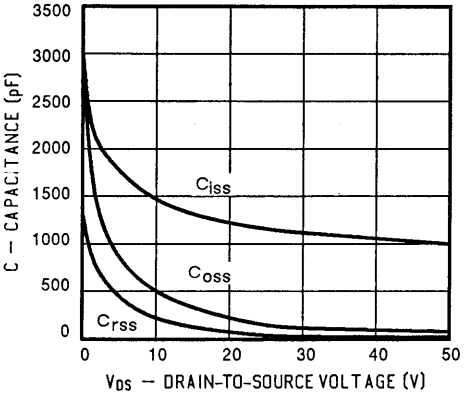
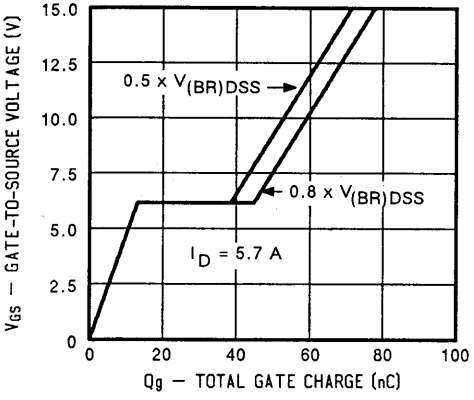


FIGURE 6: Typical Gate Charge



Siliconix incorporated

PERFORMANCE CURVES (25°C Unless otherwise noted)

FIGURE 7: On-Resistance vs. Junction Temperature

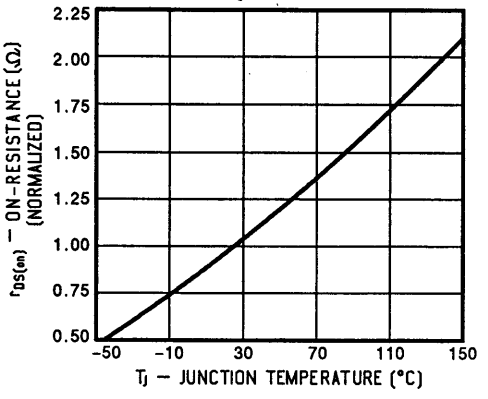


FIGURE 8: Typical Source-Drain Diode Forward Voltage

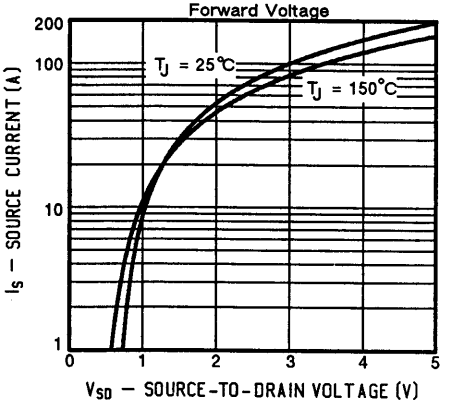


FIGURE 9: Maximum Avalanche and Drain Current vs. Case Temperature

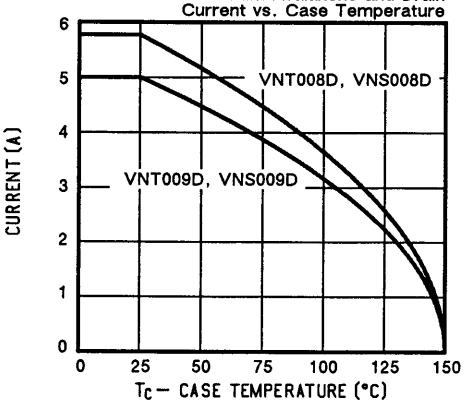
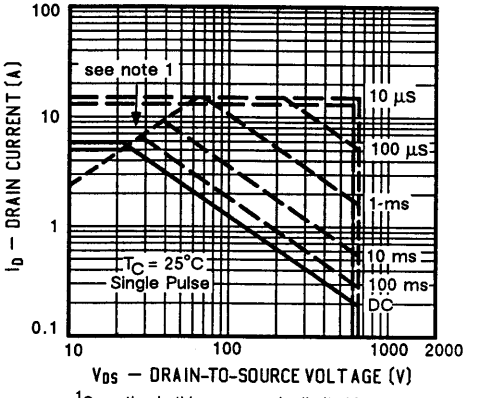


FIGURE 10: Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

FIGURE 11: Normalized Effective Transient Thermal Impedance, Junction-to-Case