N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-3	TO-220	Dice†
550V	6Ω	1.5A	VN0355N1	VN0355N5	VN0355ND
600V	6Ω	1.5A	VN0360N1	VN0360N5	VN0360ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)
- ☐ Amplifiers
- ☐ Switches

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

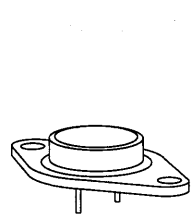
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

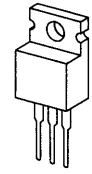
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermallyinduced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options (Note 1)



TO-3



TO-220

Note 1: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-3	2.5A	6A	100W	30	1.25	2.5A	6.0A
TO-220	1.5A	6A	50W	2.5	2.5	1.5A	6.0A

* I_D (continuous) is limited by max rated T_j.

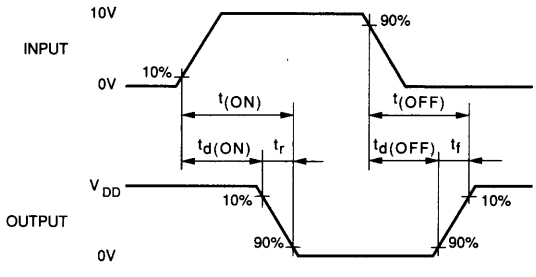
Electrical Characteristics (@ 25°C unless otherwise specified)

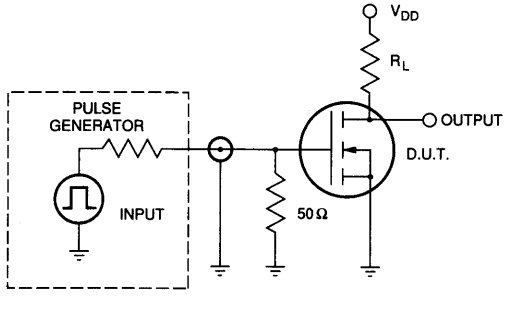
(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0360	600			V	V_{GS} = 0, I_D = 10mA
		VN0355	550				
$V_{GS(th)}$	Gate Threshold Voltage		2		4	V	V_{GS} = V_{DS}, I_D = 10mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-4.8	-6.0	mV/°C	V_{GS} = V_{DS}, I_D = 10mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ±20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				100	µA	V_{GS} = 0, V_{DS} = Max Rating
					2.0	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current			2.1		A	V_{GS} = 5V, V_{DS} = 25V
			1.5	3.2			V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			5.5		Ω	V_{GS} = 5V, I_D = 0.5A
				4.5	6.0		V_{GS} = 10V, I_D = 0.5A
$\Delta R_{DS(th)}$	Change in $R_{DS(th)}$ with Temperature			1	2	%/°C	V_{GS} = 10V, I_D = 0.5A
G_{FS}	Forward Transconductance		0.5	1		℧	V_{DS} = 25V, I_D = 0.5A
C_{ISS}	Input Capacitance			550	650	pF	V_{GS} = 0, V_{DS} = 25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance			75	125		
C_{RSS}	Reverse Transfer Capacitance			25	50		
$t_{d(ON)}$	Turn-ON Delay Time			8	15	ns	V_{DD} = 25V, I_D = 0.5A, R_S = 50Ω
t_r	Rise Time			8	15		
$t_{d(OFF)}$	Turn-OFF Delay Time			65	100		
t_f	Fall Time			12	25		
V_{SD}	Diode Forward Voltage Drop			1.1	1.5	V	V_{GS} = 0, I_{SD} = 5A
t_{rr}	Reverse Recovery Time			450		ns	V_{GS} = 0, I_{SD} = 5A

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300ms pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

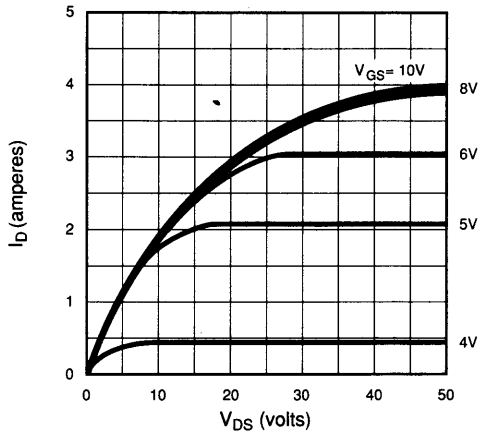
Switching Waveforms and Test Circuit



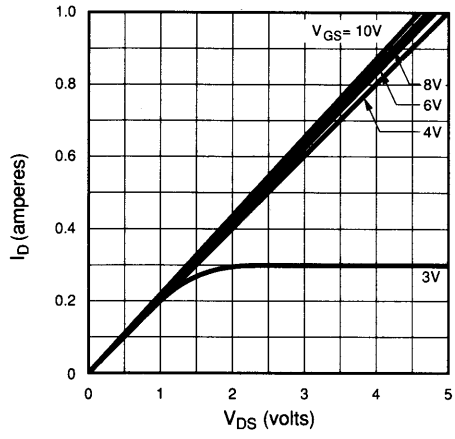


Typical Performance Curves

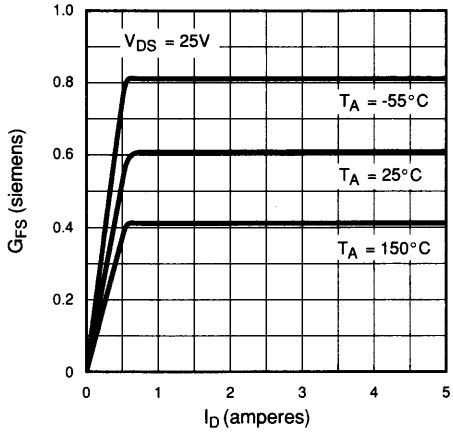
Output Characteristics



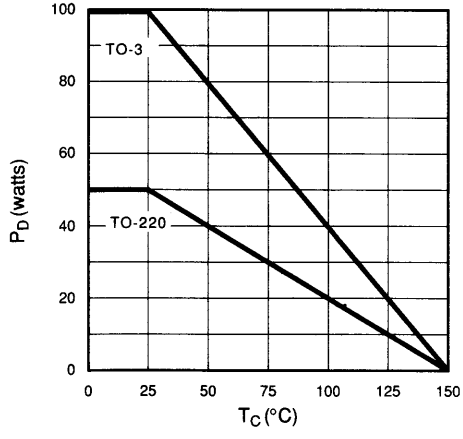
Saturation Characteristics



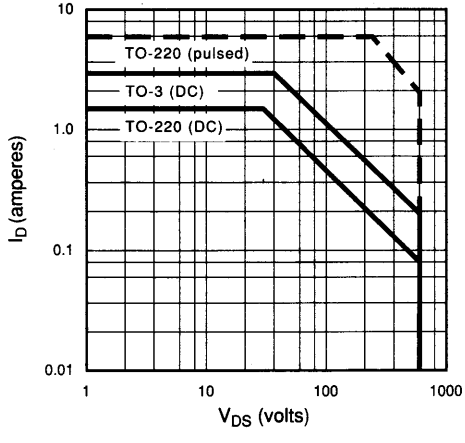
Transconductance vs. Drain Current



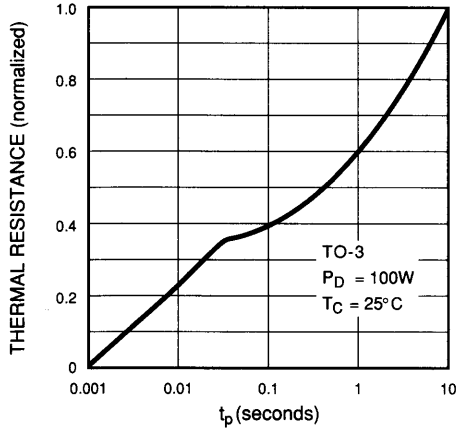
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area



Thermal Response Characteristics



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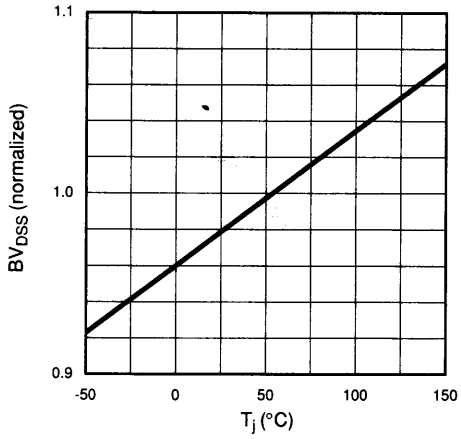
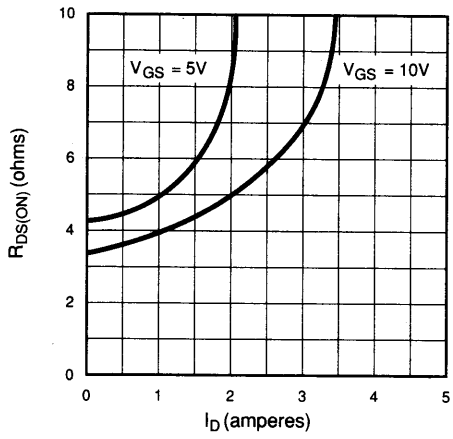
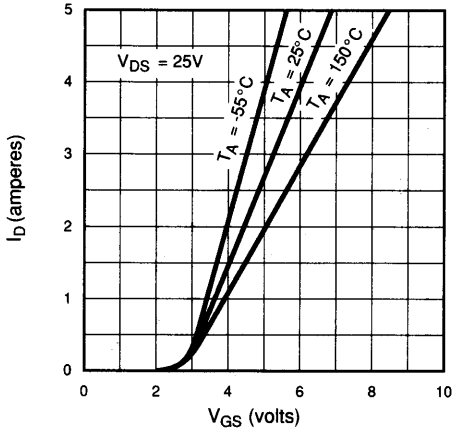
BV$_{DSS}$ Variation with Temperature



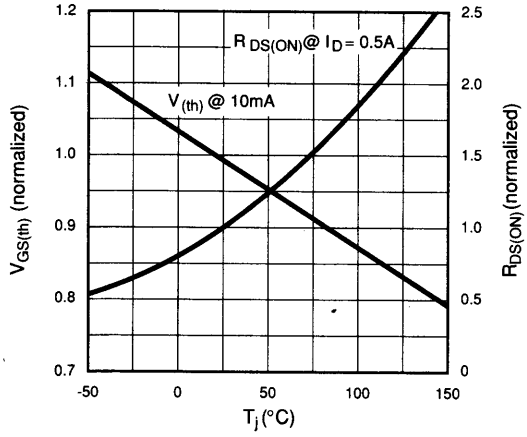
On-Resistance vs. Drain Current



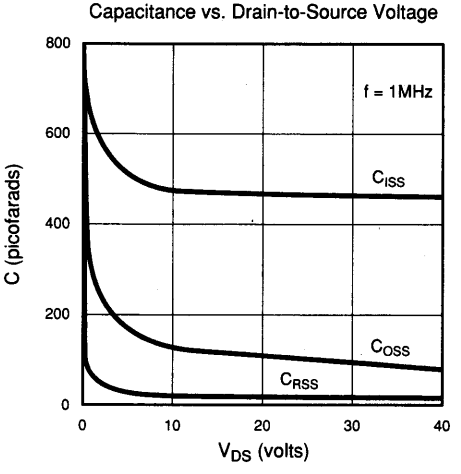
Transfer Characteristics



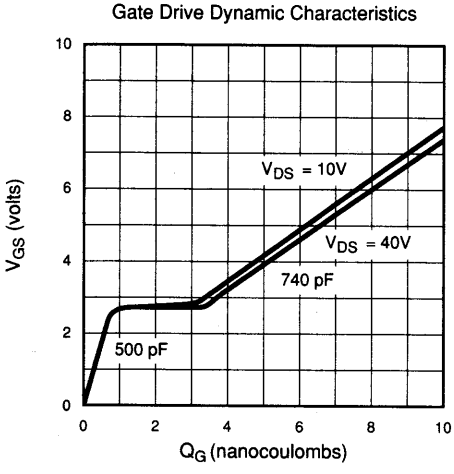
$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



P-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

Standard Commercial Devices

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package	
			TO-92	DICE†
40V	0.9Ω	-4A	VP2204N3	VP2204ND
60V	0.9Ω	-4A	VP2206N3	VP2206ND
-100V	0.9Ω	-4A	VP2210N3	VP2210ND

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	±20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermallyinduced secondary breakdown.

Supertex Vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options (Note 1)

TO-92

Note 1: See Package Outline section for discrete pinouts.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W	I_{DR}*	I_{DRM}
TO-92	-0.65A	-4.0A	1.0W	170	125	-0.65A	-4.0A

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VP2204	-40			V	V_{GS} = 0, I_D = -10mA
		VP2206	-60				
		VP2210	-100				
$V_{GS(th)}$	Gate Threshold Voltage		-1.0		-3.5	V	V_{GS} = V_{DS}, I_D = -10mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			4.3	5.5	mV/°C	V_{GS} = V_{DS}, I_D = -10mA
I_{GSS}	Gate Body Leakage			-1	-100	nA	V_{GS} = ± 20V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				-50	µA	V_{GS} = 0, V_{DS} = Max Rating
					-10	mA	V_{GS} = 0, V_{DS} = 0.8 Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current		-1.5	-2		A	V_{GS} = -5V, V_{DS} = -25V
			-4	-8			V_{GS} = -10V, V_{DS} = -25V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			1.3	1.5	Ω	V_{GS} = -5V, I_D = -1A
				0.75	0.9		V_{GS} = -10V, I_D = -3.5A
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.85	1.2	%/°C	V_{GS} = -10V, I_D = -3.5A
G_{FS}	Forward Transconductance		0.8	1.2		℧	V_{DS} = -25V, I_D = -2A
C_{ISS}	Input Capacitance				450	pF	V_{GS} = 0, V_{DS} = -25V, f = 1 MHz
C_{OSS}	Common Source Output Capacitance				180		
C_{RSS}	Reverse Transfer Capacitance				40		
$t_{d(ON)}$	Turn-ON Delay Time			10	15	ns	V_{DD} = -25V, I_D = -3.5A, R_S = 50Ω
t_r	Rise Time			10	15		
$t_{d(OFF)}$	Turn-OFF Delay Time			30	50		
t_f	Fall Time			30	50		
V_{SD}	Diode Forward Voltage Drop			-1.2	-1.6	V	V_{GS} = 0, I_{SD} = -3.5A
t_{rr}	Reverse Recovery Time			500		ns	V_{GS} = 0, I_{SD} = -1A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit