VN30AA, VN35AA, VN67AA, VN89AA, VN90AA
n-Channel Enhancement-mode VMOS Power FETs

FEATURES

- **High speed, high current switching**
- **Current sharing capability when paralleled**
- **Directly interface to CMOS, DTL, TTL logic**
- **simple DC biasing**
- **Extended safe operating area**
- **Inherently temperature stable**

APPLICATIONS

- **Switching power supplies**
- **DC to DC inverters**
- **CMOS and TTL to high current interface**
- **Line drivers**
- **Logic buffers**
- **Pulse amplifiers**

ABSOLUTE MAXIMUM RATINGS
(25°C unless otherwise noted)

Drain-source Voltage
- VN30AA, VN35AA 35V
- VN67AA 60V
- VN89AA 80V
- VN90AA 90V

Drain-gate Voltage
- VN30AA, VN35AA 35V
- VN67AA 60V
- VN89AA 80V
- VN90AA 90V

Continuous Drain Current (see note 1) 2.4A
Peak Drain Current (see note 2) 3.0A
Continuous Forward Gate Current 2.0mA
Peak-gate Forward Current 100mA
Peak-gate Reverse Current 100mA
Gate-source Forward (Zener) Voltage ..... +15V
Gate-source Reverse (Zener) Voltage ..... −0.3V
Thermal Resistance, Junction to Case ..... 5.0°C/W
Continuous Device Dissipation at (or below)
- 25°C Case Temperature 25W

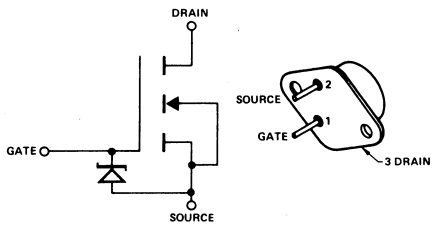
Linear Derating Factor ..... 200mW/°C
Operating Junction
- Temperature Range ..... −55 to +150°C

Storage Temperature Range ..... −55 to +150°C
Lead Temperature
- (1/16 in. from case for 10 sec) ..... +300°C

Note 1. T_C = 25°C; controlled by typical $R_{DS(on)}$ and maximum power dissipation.

Note 2. Pulse width 80μsec, duty cycle 1.0%.

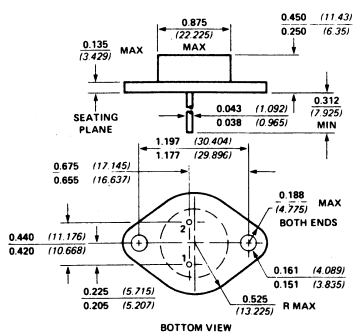
SCHEMATIC DIAGRAM



Body internally connected to source
Drain common to case

PACKAGE DIMENSIONS

PKG: JEDEC TO-3



Dimensions shown in inches and *(mm)*.

VN30AA, VN35AA, VN67AA, VN89AA, VN90AA

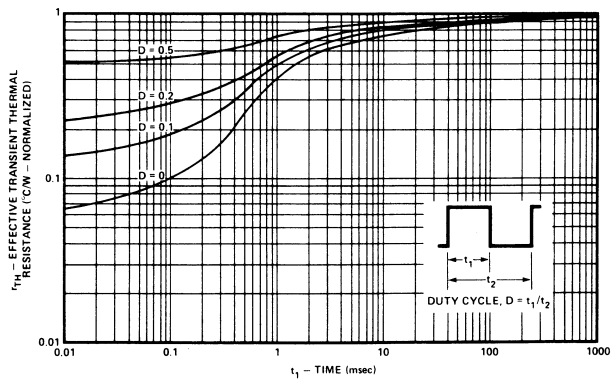
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		CHARACTERISTIC		VN30AA			VN35AA			VN67AA			VN89AA			VN90AA			UNIT	TEST CONDITIONS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
1	STATIC	BV_{DSS}	Drain Source Breakdown	35			35			60			80			90			V	I_D = 10μA, V_{GS} = 0
2		$V_{GS(th)}$	Gate Threshold Voltage	0.8	1.2		0.8	1.2		0.8	1.2		0.8	1.2		0.8	1.2			I_D = 1.0mA, V_{DS} = V_{GS}
3		I_{GSS}	Gate-Body Leakage		0.01	0.5		0.01	0.5		0.01	0.5		0.01	0.5		0.01	0.5	μA	V_{GS} = 10V, V_{DS} = 0
4		I_{DSS}	Zero Gate Voltage Drain Current			10			10			10			10			10		V_{DS} = 25V, V_{GS} = 0
5		$R_{DS(on)}$	Drain-Source ON-State Resistance (Note 1)		2.2	6.0 5.0		2.2	4.5 2.5		2.2	5.1 3.5		2.2	5.1 4.5		2.2	6.0 5.0	Ω	V_{GS} = 5V, I_D = 300mA V_{GS} = 10V, I_D = 1.0A
6		$I_{D(on)}$	ON-State Drain Current (Note 1)	1.0	2.0		1.0	2.0		1.0	2.0		1.0	2.0		1.0	2.0		A	V_{DS} = 25V, V_{GS} = 10V
7		g_{fs}	Forward Transconductance (Note 1)	150	250		150	250		150	250		150	250		150	250		mU	V_{DS} = 25V, I_D = 0.5A
8	DYNAMIC	C_{iss}	Input Capacitance (Note 2)			50			50			50			50			50	pF	V_{GS} = 0, V_{DS} = 24V, f = 1.0MHz
9		C_{rss}	Reverse Transfer Capacitance (Note 2)			10			10			10			10			10		
10		C_{oss}	Common Source Output Capacitance (Note 2)			40			40			40			40			40		
11		t_{on}	Turn-ON Time (Note 2)			10			10			10			10			10	ns	
12		t_{off}	Turn-OFF Time (Note 2)			10			10			10			10			10		

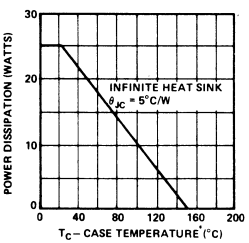
Note 1. Pulse Test — 80μs, 1% duty cycle.

Note 2. Sample Test.

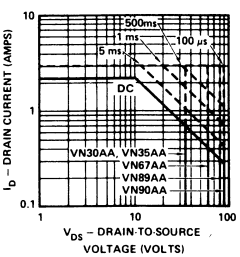
THERMAL RESPONSE



POWER DISSIPATION vs CASE TEMPERATURE



DC SAFE OPERATING REGION T_C = 25°C



VN30AB, VN35AB, VN67AB, VN89AB, VN90AB
n-Channel Enhancement-mode VMOS Power FETs

FEATURES

- **High speed, high current switching**
- **Current sharing capability when paralleled**
- **Directly interface to CMOS, DTL, TTL logic**
- **simple DC biasing**
- **Extended safe operating area**
- **Inherently temperature stable**

APPLICATIONS

- **Switching power supplies**
- **DC to DC inverters**
- **CMOS and TTL to high current interface**
- **Line drivers**
- **Logic buffers**
- **Pulse amplifiers**

ABSOLUTE MAXIMUM RATINGS
(25°C unless otherwise noted)

Drain-source Voltage
- VN30AB, VN35AB 35V
- VN67AB 60V
- VN89AB 80V
- VN90AB 90V

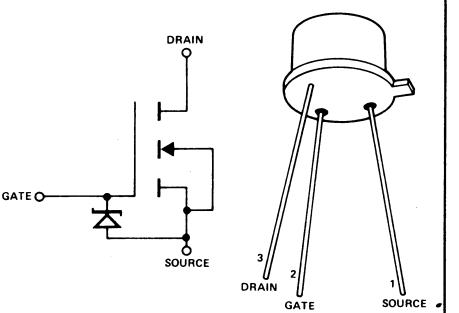
Drain-gate Voltage
- VN30AB, VN35AB 25V
- VN67AB 60V
- VN89AB 80V
- VN90AB 90V

Continuous Drain Current (see note 1) 1.2A
Peak Drain Current (see note 2) 3.0A
Continuous Forward Gate Current 2.0mA
Peak-gate Forward Current 100mA
Peak-gate Reverse Current 100mA
Gate-source Forward (Zener) Voltage ..... +15V
Gate-source Reverse (Zener) Voltage ..... –0.3V
Thermal Resistance, Junction to Case ..... 20°C/W
Continuous Device Dissipation at (or below)
25°C Case Temperature 6.25W
Linear Derating Factor ..... 50mW/°C
Operating Junction
Temperature Range ..... –55 to +150°C
Storage Temperature Range ..... –55 to +150°C
Lead Temperature
(1/16 in. from case for 10 sec) ..... +300°C

Note 1. T_C = 25°C; controlled by typical $R_{DS(on)}$ and maximum power dissipation.

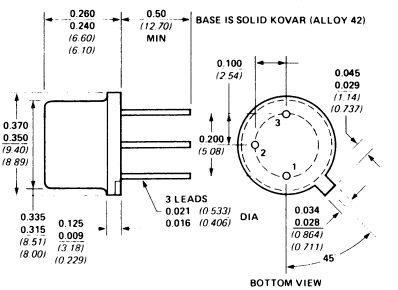
Note 2. Pulse width 80μsec, duty cycle 1.0%.

SCHEMATIC DIAGRAM



Body internally connected to source.
Drain common to tab.

PACKAGE DIMENSIONS
PKG: JEDEC TO-39



Dimensions shown in inches and *(mm)*.

VN30AB, VN35AB, VN67AB, VN89AB, VN90AB

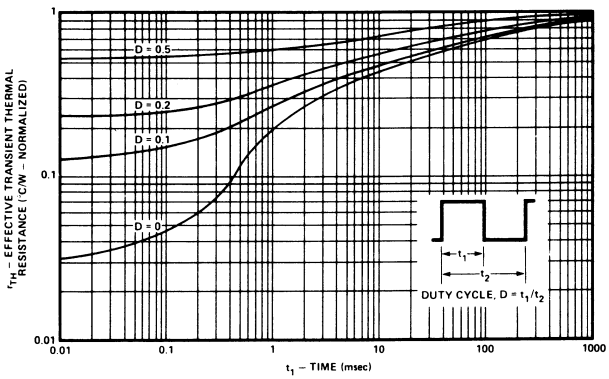
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		CHARACTERISTIC		VN30AB			VN35AB			VN67AB			VN89AB			VN90AB			UNIT	TEST CONDITIONS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
1		BV_{DSS}	Drain Source Breakdown	35			35			60			80			90			V	I_D = 10μA, V_{GS} = 0
2		$V_{GS(th)}$	Gate Threshold Voltage	0.8	1.2		0.8	1.2		0.8	1.2		0.8	1.2		0.8	1.2			I_D = 1.0mA, V_{DS} = V_{GS}
3	STATIC	I_{GSS}	Gate-Body Leakage		0.01	0.5		0.01	0.5		0.01	0.5		0.01	0.5		0.01	0.5	μA	V_{GS} = 10V, V_{DS} = 0
4	STATIC	I_{DSS}	Zero Gate Voltage Drain Current			10			10			10			10			10	μA	V_{DS} = 25V, V_{GS} = 0
5	STATIC	$R_{DS(on)}$	Drain-Source ON-State Resistance (Note 1)			6.0			4.5			5.1			5.1			6.0	Ω	V_{GS} = 5V, I_D = 300mA
					2.2	5.0		2.2	2.5		2.2	3.5		2.2	4.5		2.2	5.0		V_{GS} = 10V, I_D = 1.0A
6	STATIC	$I_{D(on)}$	ON-State Drain Current (Note 1)	1.0	2.0		1.0	2.0		1.0	2.0		1.0	2.0		1.0	2.0		A	V_{DS} = 25V, V_{GS} = 10V
7		g_{fs}	Forward Transconductance		250			250			250			250			250		m℧	V_{DS} = 25V, I_D = 0.5A
8	DYNAMIC	C_{iss}	Input Capacitance (Note 2)			50			50			50			50			50	pF	V_{GS} = 0, V_{DS} = 24V, f = 1.0MHz
9	DYNAMIC	C_{rss}	Reverse Transfer Capacitance (Note 2)			10			10			10			10			10		
10	DYNAMIC	C_{oss}	Common Source Output Capacitance (Note 2)			40			40			40			40			40		
11		t_{on}	Turn-ON Time (Note 2)			10			10			10			10			10	ns	
12		t_{off}	Turn-OFF Time (Note 2)			10			10			10			10			10		

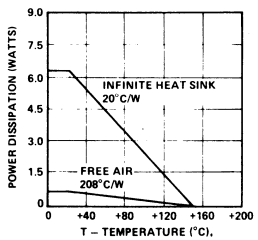
Note 1. Pulse Test — 80μs, 1% duty cycle.

Note 2. Sample Test.

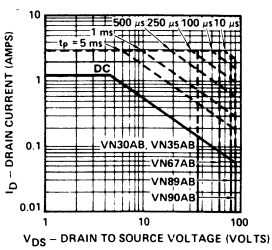
THERMAL RESPONSE



POWER DISSIPATION vs CASE OR AMBIENT TEMPERATURE



DC SAFE OPERATING REGION T_C = 25°C



VN35AJ, VN66AJ, VN67AJ, VN98AJ, VN99AJ
n-Channel Enhancement-mode VMOS Power FETs

FEATURES

- **High speed, high current switching**
- **High gain-bandwidth product**
- **Inherently temperature stable**
- **Extended safe operating area**
- **simple DC biasing**
- **Requires almost zero current drive**

APPLICATIONS

- **High current analog switches**
- **RF power amplifiers**
- **Laser diode pulsers**
- **Line drivers**
- **Logic buffers**
- **Pulse amplifiers**

ABSOLUTE MAXIMUM RATINGS
(25°C unless otherwise noted)

Drain-source Voltage
- VN35AJ 35V
- VN66AJ, VN67AJ 60V
- VN98AJ, VN99AJ 90V

Drain-gate Voltage
- VN35AJ 35V
- VN66AJ, VN67AJ 60V
- VN98AJ, VN99AJ 90V

Continuous Drain Current (see note 1) 2.4A
Peak Drain Current (see note 2) 3.0A
Gate-source Forward Voltage ..... +30V
Gate-source Reverse Voltage ..... −30V
Thermal Resistance, Junction to Case ..... 5.0°C/W
Continuous Device Dissipation at (or below)
- 25°C Case Temperature 25W

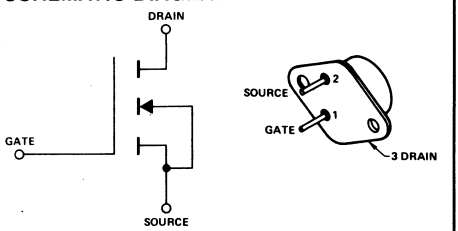
Linear Derating Factor ..... 200mW/°C
Operating Junction
- Temperature Range ..... −55 to +150°C

Storage Temperature Range ..... −55 to +150°C
Lead Temperature
- (1/16 in. from case for 10 sec) ..... +300°C

Note 1. T_C = 25°C; controlled by typical $R_{DS(on)}$ and maximum power dissipation.

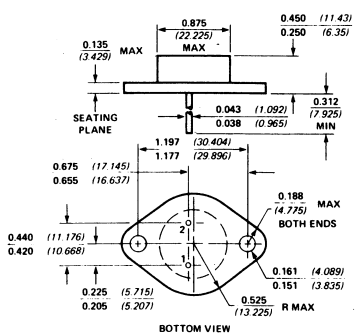
Note 2. Pulse width 80μsec, duty cycle 1.0%.

SCHEMATIC DIAGRAM



Body internally connected to source.
Drain common to case.

PACKAGE DIMENSIONS
PKG: JEDEC TO-3



Dimensions shown in inches and *(mm)*.

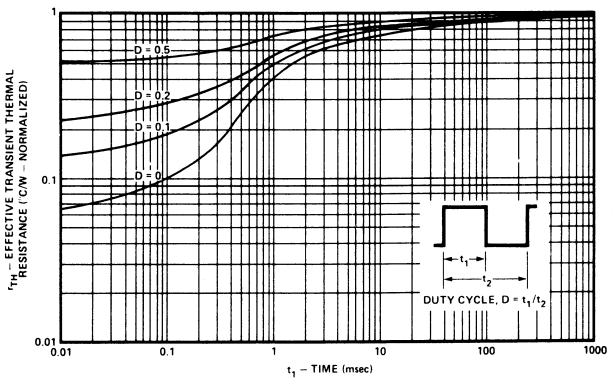
VN35AJ, VN66AJ, VN67AJ, VN98AJ, VN99AJ

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

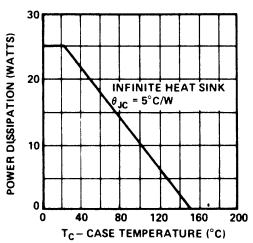
		CHARACTERISTIC		VN35AJ			VN66AJ VN67AJ			VN98AJ VN99AJ			UNIT	TEST CONDITIONS	
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
1		BV_{DSS}	Drain-Source Breakdown	35			60			90			V	V_{GS} = 0, I_D = 10μA	
2		$V_{GS(th)}$	Gate-Threshold Voltage	0.8		2.0	0.8		2.0	0.8		2.0		V_{DS} = V_{GS}, I_D = 1mA	
3		I_{GSS}	Gate-Body Leakage		0.5	100		0.5	100		0.5	100	nA	V_{GS} = 15V, V_{DS} = 0	
4						500			500			500		V_{GS} = 15V, V_{DS} = 0, T_A = 125°C (Note 2)	
5	S	I_{DSS}	Zero Gate Voltage Drain Current			10			10			10	μA	V_{DS} = Max. Rating, V_{GS} = 0	
6	T					500			500			500		V_{DS} = 0.8 Max. Rating, V_{GS} = 0, T_A = 125°C (Note 2)	
7	A				100			100			100		nA	V_{DS} = 25V, V_{GS} = 0	
8	T	$I_{D(on)}$	ON-State Drain Current	1.0	2.0		1.0	2.0		1.0	2.0		A	V_{DS} = 25V, V_{GS} = 10V	
9	I	$V_{DS(on)}$	Drain-Source Saturation Voltage VN66AJ					1.0			1.1		V	V_{GS} = 5V, I_D = 0.3A	(Note 1)
10	C		VN98AJ					2.2	3.0		2.2	4.0		V_{GS} = 10V, I_D = 1.0A	
11			VN35AJ VN67AJ VN99AJ		1.0			1.1			1.2			V_{GS} = 5V, I_D = 0.3A	
12					2.2	2.5		2.2	3.5		2.2	4.5		V_{GS} = 10V, I_D = 1.0A	
13		g_{fs}	Forward Transconductance	170	250		170	250		170	250		m℧	V_{DS} = 24V, I_D = 0.5A	
14	D	C_{iss}	Input Capacitance		40	50		40	50		40	50	pF	V_{GS} = 0, V_{DS} = 24V, f = 1MHz	(Note 2)
15	Y	C_{oss}	Common Source Output Capacitance		38	45		35	40		32	40			
16	N	C_{rss}	Reverse Transfer Capacitance		7	10		6	10		5	10			
17	A	t_{on}	Turn ON Time		3	8		3	8		3	8	ns		
18	M	t_{off}	Turn OFF Time		3	8		3	8		3	8			
	I														
	C														

Note 1. Pulse test — 80μs pulse, 1% duty cycle.
Note 2. Sample test.

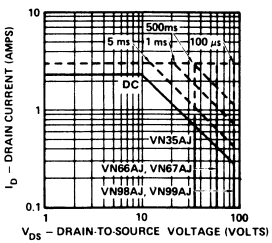
THERMAL RESPONSE



POWER DISSIPATION vs CASE TEMPERATURE



DC SAFE OPERATING REGION T_C = 25°C



VN46AF, VN66AF, VN88AF
n-Channel Enhancement-mode VMOS Power FETs

FEATURES

- **High speed, high current switching**
- **Current sharing capability when paralleled**
- **Directly interface to CMOS, DTL, TTL logic**
- **simple DC biasing**
- **Extended safe operating area**
- **Inherently temperature stable**

APPLICATIONS

- **Switching power supplies**
- **DC to DC inverters**
- **CMOS and TTL to high current interface**
- **Line drivers**
- **Logic buffers**
- **Pulse amplifiers**

ABSOLUTE MAXIMUM RATINGS
(25°C unless otherwise noted)

Drain-source Voltage
- VN46AF 40V
- VN66AF 60V
- VN88AF 80V

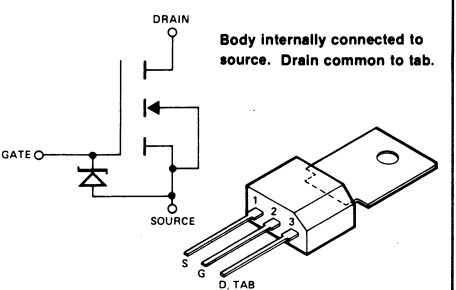
Drain-gate Voltage
- VN46AF 40V
- VN66AF 60V
- VN88AF 80V

Continuous Drain Current (see note 1) 1.7A
Peak Drain Current (see note 2) 3.0A
Continuous Forward Gate Current 2.0mA
Peak-gate Forward Current 100mA
Peak-gate Reverse Current 100mA
Gate-source Forward (Zener) Voltage ..... +15V
Gate-source Reverse (Zener) Voltage ..... −0.3V
Thermal Resistance, Junction to Case ..... 10.4°C/W
Continuous Device Dissipation at (or below)
25°C Case Temperature 12W
Linear Derating Factor ..... 96mW/°C
Operating Junction
Temperature Range ..... −40 to +150°C
Storage Temperature Range ..... −40 to +150°C
Lead Temperature
(1/16 in. from case for 10 sec) ..... +300°C

Note 1. T_C = 25°C; controlled by typical $R_{DS(on)}$ and maximum power dissipation.

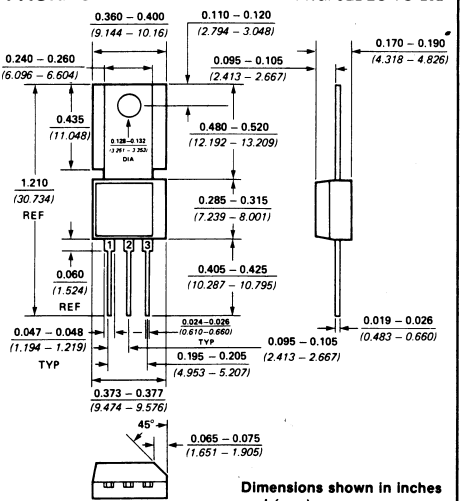
Note 2. Pulse width 80μsec, duty cycle 1.0%.

SCHEMATIC DIAGRAM



PACKAGE DIMENSIONS

PKG: JEDEC TO-202



Dimensions shown in inches and *(mm)*.

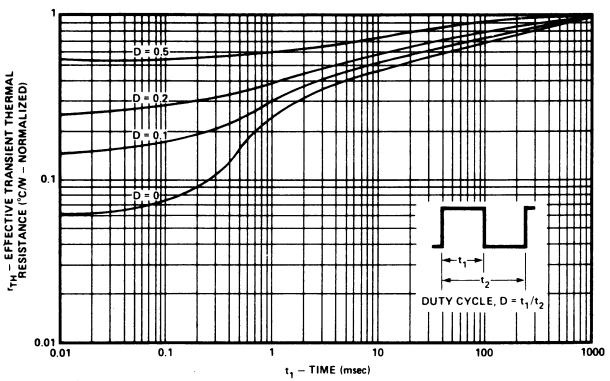
VN46AF, VN66AF, VN88AF

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

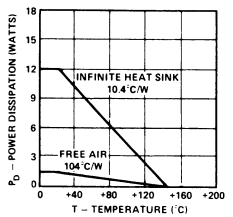
		CHARACTERISTIC		VN46AF			VN66AF			VN88AF			UNIT	TEST CONDITIONS	
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DSS}	Drain-Source Breakdown	40			60			80			V	V_{GS} = 0, I_D = 10μA	
2				40			60			80				V_{GS} = 0, I_D = 2.5mA	
3		$V_{GS(th)}$	Gate-Threshold Voltage	0.8	1.7		0.8	1.7		0.8	1.7			V_{DS} = V_{GS}, I_D = 1mA	
4		I_{GSS}	Gate-Body Leakage		0.01	10		0.01	10		0.01	10	μA	V_{GS} = 10V, V_{DS} = 0	
5						100			100			100		V_{GS} = 10V, V_{DS} = 0, T_A = 125°C (Note 2)	
6		I_{DSS}	Zero Gate Voltage Drain Current			10			10			10		V_{DS} = Max. Rating, V_{GS} = 0	
7						100			100			100		V_{DS} = 0.8 Max. Rating, V_{GS} = 0, T_A = 125°C (Note 2)	
8					100			100			100		nA	V_{DS} = 25V, V_{GS} = 0	
9		$I_{D(on)}$	ON-State Drain Current	1.0	2		1.0	2		1.0	2		A	V_{DS} = 25V, V_{GS} = 10V	
10		$V_{DS(on)}$	Drain-Source Saturation Voltage		0.3			0.3			0.4		V	V_{GS} = 5V, I_D = 0.1A	(Note 1)
11					1.0	1.5		1.0	1.5		1.4	1.7		V_{GS} = 5V, I_D = 0.3A	
12					1.0			1.0			1.3			V_{GS} = 10V, I_D = 0.5A	
13					2.2	3.0		2.2	3.0		2.2	4.0		V_{GS} = 10V, I_D = 1.0A	
14		g_{fs}	Forward Transconductance	150	250		150	250		150	250		mU	V_{DS} = 24V, I_D = 0.5A	
15	DYNAMIC	C_{iss}	Input Capacitance			50			50			50	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0MHz	(Note 2)
16		C_{rss}	Reverse Transfer Capacitance			10			10			10			
17		C_{oss}	Common-Source Output Capacitance			50			50			50			
18		$t_{d(on)}$	Turn-ON Delay Time		2	5		2	5		2	5	ns		
19		t_r	Rise Time		2	5		2	5		2	5			
20		$t_{d(off)}$	Turn-OFF Delay Time		2	5		2	5		2	5			
21		t_f	Fall Time		2	5		2	5		2	5			

Note 1. Pulse test — 80μs pulse, 1% duty cycle. **Note 2.** Sample test.

THERMAL RESPONSE



POWER DISSIPATION vs CASE OR AMBIENT TEMPERATURE



DC SAFE OPERATING REGION
T_C = 25°C