n-channel enhancement-mode VMOS Power FET *designed for . . .*

Siliconix

Performance Curves VNMG See Section 3

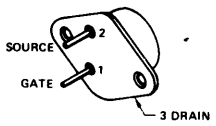
- **Motor Controllers**
- **Switching Power Supplies**
- **Linear Amplifiers**
- **Switching Amplifiers**

BENEFITS

- Directly Interfaces to CMOS, TTL, DTL and MOS Logic Families
  Low Drive Current ($I_{GSS} < 100$ nA)
- Permits Very Efficient High Density Switching Designs
  Typical t_{on} and $t_{off} < 50$ nsec

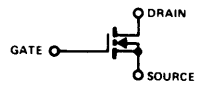
A-, J-Package

TO-3



ABSOLUTE MAXIMUM RATINGS

Maximum Drain-Source Voltage	60 V
Maximum Drain-Gate Voltage	60 V
Maximum Continuous Drain Current	12.5 A
Maximum Pulse Drain Current (Note 1)	15 A
Maximum Gate-Source Voltage	±30 V
Maximum Dissipation at 25°C Case Temperature	80 W
Linear Derating Factor	640 mW/°C
Temperature (Operating and Storage)	−55 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C



NOTE:

1. Pulse test – 300 μsec pulse, 1% duty cycle.

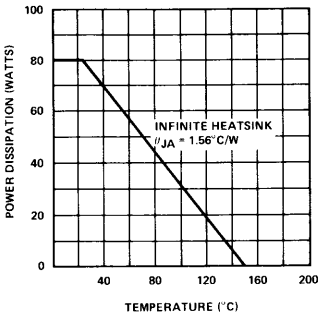
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions
1	STATIC	BV_{DSS}	Drain-Source Breakdown	60			V	V_{GS} = 0V, I_D = 500 μA
2		$V_{GS(th)}$	Gate Threshold Voltage	1.0	2.7	4.0		V_{DS} = V_{GS}, I_D = 10 mA
3		I_{GSS}	Gate-Body Leakage		0.3	100	nA	V_{GS} = 12 V, V_{DS} = 0
4		I_{DSS}	Zero Gate Voltage Drain Current			500	μA	V_{DS} = Max. Rating, V_{GS} = 0
5		$I_{D(on)}$	ON-State Drain Current	12.5			A	V_{DS} = 25 V, V_{GS} = 12 V (Note 1)
6		$R_{DS(on)}$	Drain-Source ON Resistance		0.3	0.4	Ω	V_{GS} = 12 V, I_D = 10 A
7	DYNAMIC	g_{fs}	Forward Transconductance	1.5	2.2		℧	V_{DS} = 20 V, I_D = 5 A (Note 1)
8		C_{iss}	Input Capacitance		700		pF	V_{GS} = 0, V_{DS} = 25 V, f = 1.0 MHz
9		C_{rss}	Reverse Transfer Capacitance		25			
10		C_{oss}	Output Capacitance		325			
11		t_{on}	Turn-ON Time		45		ns	V_{DS} = 10 V, I_D = 10 A (Note 2) R_L = 1 Ω, R_S = 50 Ω
12		t_{off}	Turn-OFF Time		45			

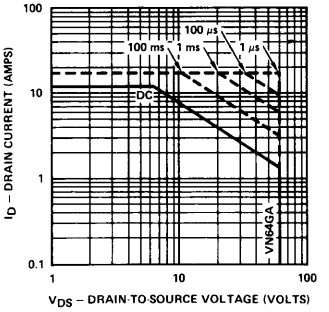
NOTES: 1. Pulse Test — 300 μs, 1% duty cycle
2. See switching time test circuit

VNMG

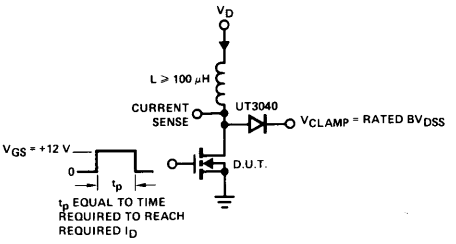
Power Dissipation vs Case or Ambient Temperature



DC and Inductive Safe Operating Region T_C = 25°C



Inductive Safe Operating Area Test Circuit



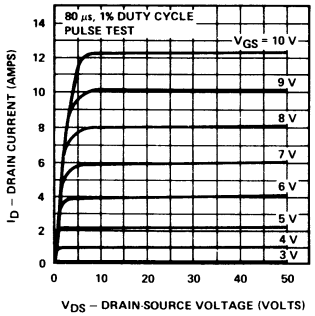
n-channel
enhancement-mode
VMOS Power FETs

Siliconix

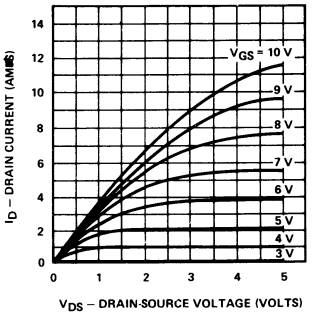
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-3	VN64GA

TYPICAL PERFORMANCE CURVES (25°C unless otherwise noted)

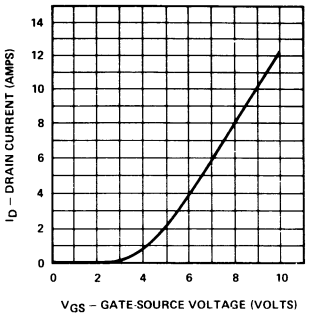
Output Characteristics



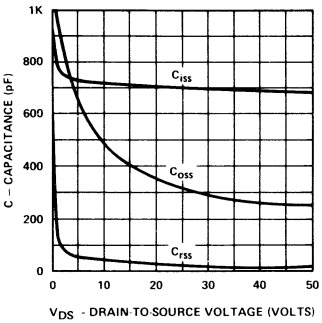
Saturation Characteristics



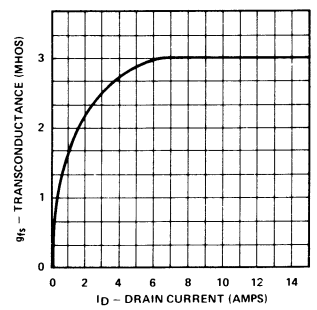
Transfer Characteristic



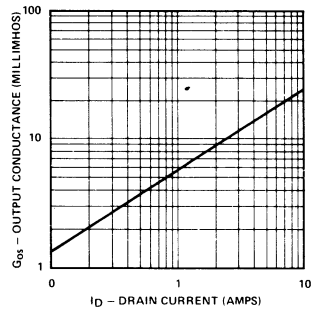
Capacitance vs
Drain-to-Source Voltage



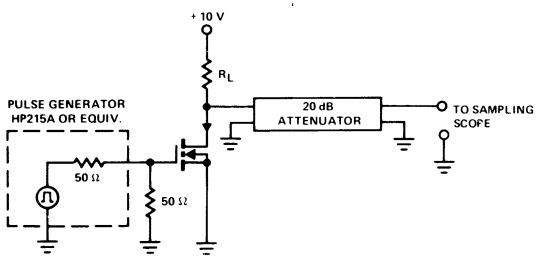
Transconductance vs
Drain Current



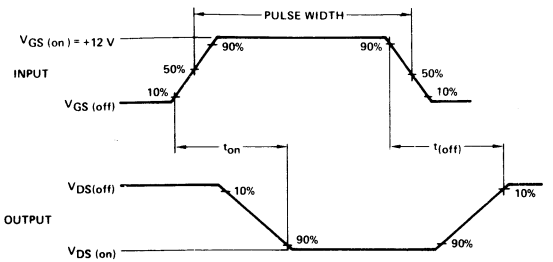
Output Conductance vs
Drain Current



Switching Time Test Circuit

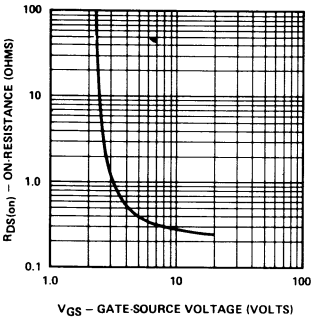


Switching Time Test Waveforms

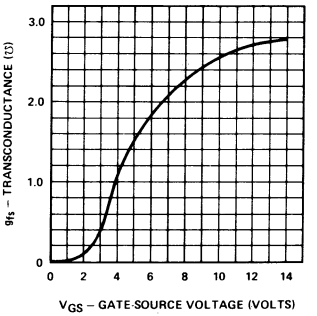


TYPICAL PERFORMANCE CURVES (Cont'd) (25° C unless otherwise noted)

ON-Resistance vs
Gate-Source Voltage



Transconductance vs
Gate-Source Voltage



Normalized Drain-Source
ON-Resistance vs Temperature