Quad VMOS Power FETs

Siliconix

High Speed Logic Compatible Interface TTL & CMOS

N-Channel 60 Volts 0.3/0.5 Amps 5 Ohms

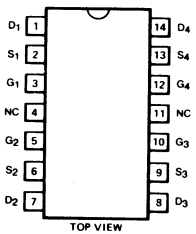
FEATURES

- Very high input impedance
- Very high speed
- Low on-resistance
- No second breakdown
- High reliability

APPLICATIONS

- Logic to high current interface
- High speed line driver
- LED digit strobe driver
- Linear amplifiers
- Stepper motor drive

DUAL-IN-LINE PACKAGE



Order Number

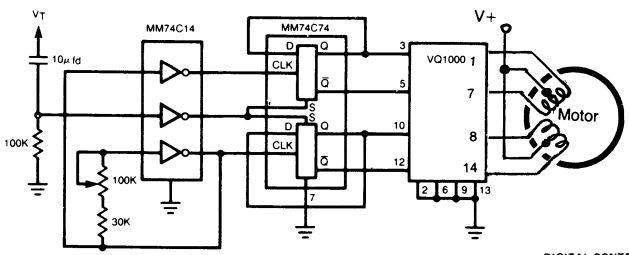
VQ1000 J — Plastic
VQ1000 P — Ceramic

Performance Curves VNML VNMK
See Section 3

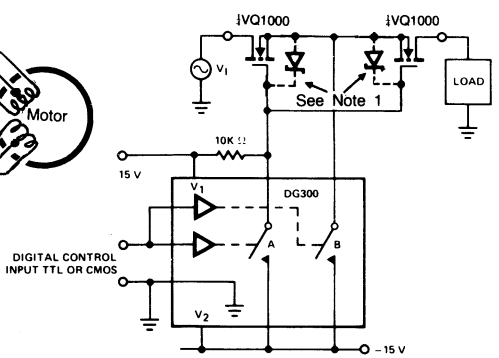
ABSOLUTE MAXIMUM RATINGS

Drainage-Source Voltage	60 V	Reverse Gate-Source Voltage	0.3 V
Drain-Gate Voltage	60 V	Drain-Source Diode Continuous Current	0.5A
Continuous Drain Current (per device)		Drain-Source Diode Pulsed Current	1.0A
VQ1000 J	0.3A	Temperature Range (Operating and Storage)	
VQ1000 P	0.5A	VQ1000J	−40 to +125°C
Pulsed Drain Current (per device)	1.0A	VQ1000P	−55 to +150°C
Forward Gate-Source Voltage	15 V		

Stepper Motor Drive Circuit



A General Purpose Bidirectional Analog Switch



Note 1: Applies to zener protected devices which will be discontinued after 31 December, 1981.

Siliconix

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

Symbol	Characteristic	Min	Typ	Max	Units	Test Conditions	
BV_{DSS}	Drain-Source Breakdown	60			V	V_{GS} = 0V, I_D = 100μA	
$V_{GS(th)}$	Gate Threshold Voltage	0.8			V	V_{GS} = V_{DS}, I_D = 1mA	
I_{GSS}	Gate-Body Leakage			100	nA	V_{GS} = 10 V, V_{DS} = 0	
I_{DSS}	Zero Gate Voltage Drain Current			10	μA	V_{DS} = 40 V, V_{GS} = 0	
$I_{D(on)}$	ON State Drain Current	0.20			A	V_{DS} = 25 V, V_{GS} = 5 V	Note 1
		0.5			A	V_{DS} = 25 V, V_{GS} = 10 V	
$V_{DS(on)}$	Drain-Source On Resistance			1.5	V	I_D = 0.3 A, V_{GS} = 5 V	
				1.65	V	I_D = 0.5 A, V_{GS} = 10 V	
g_{fs}	Forward Transconductance	100			mΩ	V_{DS} = 15 V, I_D = 0.5 A	
C_{iss}	Input Capacitance		48		pF	V_{DS} = 25 V, f = 1 MHz	Note 2
C_{oss}	Output Capacitance		16		pF		
C_{rss}	Feedback Capacitance		2		pF		
t_{on}	Turn-ON Time			10	ns	I_D = 0.3 A, R_L = 23 Ω	
t_{off}	Turn-OFF Time			10	ns	R_S = 50 Ω	
t_{rr}	Drain-Source Diode Recovery Time		230		ns	I_F = I_R = 1 A, i_{rr} = 0.1 A	
			165		ns	I_F = I_R = 0.3 A, i_{rr} = 0.03 A	

NOTES: 1) Pulse Test — 80 μs pulse, % duty cycle.
2) Sample Test.

POWER RATINGS (Tambient = 25°C)

Test	Unit	Each Transistor		All Four Transistors	
		VQ1000 J	VQ1000 P	VQ1000 J	VQ1000 P
Total Power Dissipation	Watts	0.50	1.30	1.20	2.0
Linear Derating Factor	mW/°C	4.0	10.5	9.6	16
Thermal Resistance	°C/W	250	96	104	62.5
Thermal Coupling Factor (K) Q_1-Q_4 or Q_2-Q_3 Q_1-Q_2, Q_3-Q_4, Q_1-Q_3, or Q_4-Q_2	 % %	 50 16	 60 50		

Siliconix

THERMAL COUPLING AND EFFECTIVE THERMAL RESISTANCE

In multiple chip devices, coupling of heat between die occurs. The junction temperature can be calculated as follows:

(1) $\Delta T_{J1} = R_{\theta 1} P_{D1} + R_{\theta 2} K_{\theta 2} P_{D2} + R_{\theta 3} K_{\theta 3} P_{D3} + R_{\theta 4} K_{\theta 4} P_{D4}$

where ΔT_{J1} is the change in junction temperature of die 1
$R_{\theta 1}$ thru 4 is the thermal resistance of die 1 through 4
P_{D1} thru 4 is the power dissipated in die 1 through 4
$K_{\theta 2}$ thru 4 is the thermal coupling between die 1 and die 2 through 4

An effective package thermal resistance can be defined as follows:

(2) $R_{\theta(EFF)} = \Delta T_{J1}/P_{DT}$

Where: P_{DT} is the total package power dissipation.

Assuming equal thermal resistance for each die, equation (1) simplifies to:

(3) $\Delta T_{J1} = R_{\theta 1} (P_{D1} + K_{\theta 2} P_{D2} + K_{\theta 3} P_{D3} + K_{\theta 4} P_{D4})$

For the conditions where $P_{D1} = P_{D2} = P_{D3} = P_{D4}$ $P_{DT} = 4P_D$ equation (3) can be further simplified and by substituting into equation (2) results in:

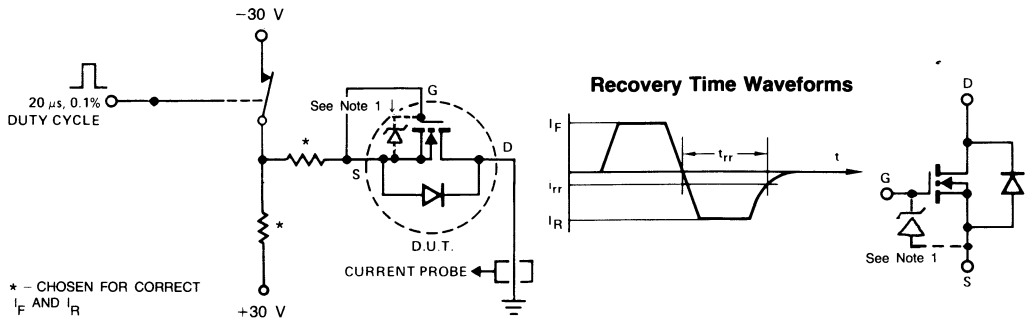
(4) $R_{\theta(EFF)} = R_{\theta 1} (1 + K_{\theta 2} + K_{\theta 3} + K_{\theta 4})/4$

Values for the coupling factors when the ambient is used as a reference are given in the table on page 2. If significant power is to be dissipated in two die, die at the opposite ends of the package should be used so that lowest position junction temperatures will result.

DRAIN-SOURCE DIODE (t_{rr} — REVERSE RECOVERY TIME)

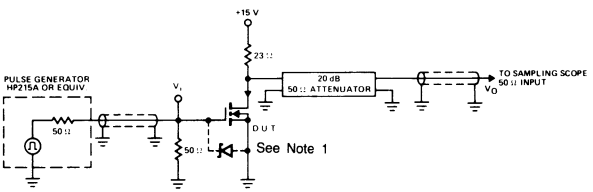
The internal drain-source diodes of VMOS Power FETs may be used as catch diodes or free-wheeling diodes. Current ratings for these diodes are the same as the continuous and peak drain current ratings for the VMOS FET.

Reverse recovery time is measured using the circuit below. Forward and reverse current I_F and I_R are equal and are tested at the condinuous and peak current ratings of the VMOS.

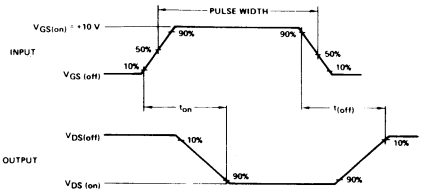


Note 1. Applies to zener protected devices which will be discontinued after 31 December, 1981.

Switching Time Test Circuit



Switching Time Test Waveforms



Quad VMOS Power FETs

Siliconix

N&P Channel 30 Volts

1 Ohm N-Channel 2 Ohm P-Channel

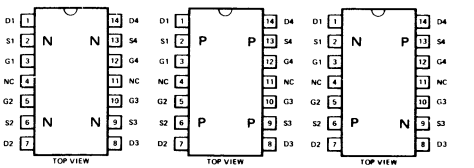
FEATURES

- Four devices per package—Complementary or same polarity available
- Low on-resistance
- High input impedance
- High speed

APPLICATIONS

- Bubble memory driver
- Line drivers
- Pin drivers
- Stepper motor drivers
- Logic to high power interface
- Low resistance analog switches

PACKAGE COMBINATIONS



ORDER NUMBER:

VQ1001P	VQ2001P	VQ3001P

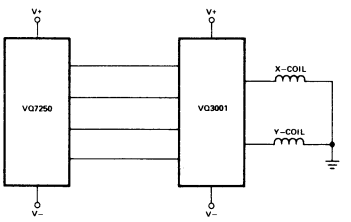
TO-116 ceramic side braze package

ABSOLUTE MAXIMUM RATINGS* (T_A = 25° C unless otherwise noted)

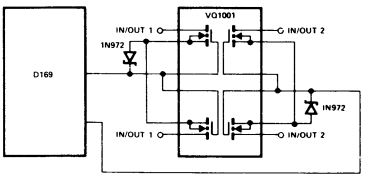
Drain-Source Voltage	30 V
Drain-Gate Voltage	30 V
Continuous Drain Current (Single Device, T_A = 25°C)	
P-Channel	600mA
N-Channel	850mA
Pulsed Drain Current	
P-Channel	2.0 Amp
N-Channel	3.0 Amp
Gate-Source Voltage	±20 V
Body-Drain Diode Continuous Current (Single Device, T_A = 25°C)	
N-Channel	1.0 Amp
P-Channel	0.8 Amp
Body-Drain Diode Pulsed Current	3.0 Amp
Temperature Range (Operating and Storage)	−40 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

*reverse polarities for P-Channel

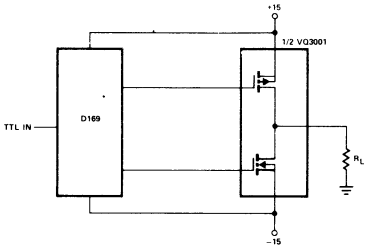
TYPICAL APPLICATIONS



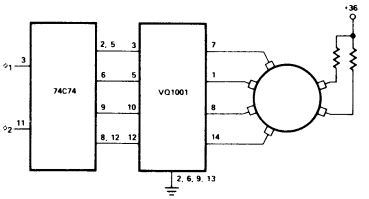
Bubble Memory Driver



Dual Bidirectional Analog Switch



High Current Line Driver



Stepper Motor Drive Circuit

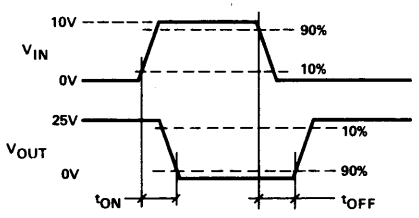
Siliconix

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

N-Channel

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μA)	$V_{(BR)DSS}$	30			V
Zero Gate Voltage Drain Current (V_{GS} = 0, V_{DS} = 30V)	I_{DSS}			10	μA
Gate Body Leakage Current (V_{GS} = 16V, V_{DS} = 0)	I_{GSS}		1	100	nA
On Characteristics (Note 1)					
Gate Threshold Voltage (V_{GS} = V_{DS}, I_D = 1 mA)	$V_{GS(th)}$	0.8			V
Drain-Source On Voltage (V_{GS} = 5V, I_D = 200 mA) (V_{GS} = 12V, I_D = 1A)	$V_{DS(on)}$		0.28 0.90	0.35 1.0	V
On-State Drain Current (V_{GS} = 12V, V_{DS} = 25V)	$I_{D(on)}$	2.0			A
Dynamic Characteristics					
Forward Transconductance (V_{DS} = 15V, I_D = 500 mA)	g_{fs}	250	340		mmhos
Input Capacitance (V_{DS} = 25V, V_{GS} = 0, f = 1 MHz)	C_{iss}		80	100	pF
Output Capacitance (V_{DS} = 25V, V_{GS} = 0, f = 1 MHz)	C_{oss}		65	80	pF
Reverse Transfer Capacitance (V_{DS} = 25V, V_{GS} = 0, f = 1 MHz)	C_{rss}		39	55	pF
Switching Characteristics					
Turn-on Time (See Figure 1)	t_{on}			30	ns
Turn-off Time (See Figure 1)	t_{off}			30	ns
Body-Drain Diode Characteristics					
Forward Recovery Time (I_F = 0.5A, See Figure 3)	t_{fr}		40	50	ns
Reverse Recovery Time I_F = I_R = 0.5A, See Figure 3)	t_{rr}		36	50	ns
Forward Voltage (V_{GS} = 0, I_S = 0.5A)	V_{SD}		0.9		V

Note 1: Pulsed test 80 μs pulse ≤ 1% duty cycle. VNMH-30
Note 2: Electrical specifications are subject to change without notice.



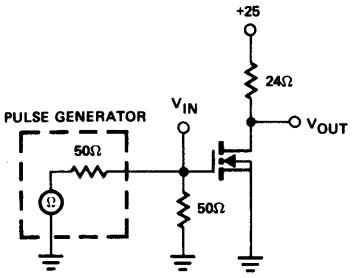


Figure 1. N-Channel Switching Time Test Circuit

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Siliconix

P-Channel

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = −10 μA)	$V_{(BR)DSS}$	30			V
Zero Gate Voltage Drain Current (V_{GS} = 0, V_{DS} = −30V)	I_{DSS}			10	μA
Gate Body Leakage Current (V_{GS} = −16, V_{DS} = 0)	I_{GSS}		1	100	nA
On Characteristics (Note 1)					
Gate Threshold Voltage (V_{GS} = V_{DS}, I_D = −1 mA)	$V_{GS(th)}$	0.8			V
Drain-Source On Voltage (V_{GS} = −5V, I_D = −200 mA) (V_{GS} = −12V, I_D = −1A)	$V_{DS(on)}$		1.0 1.6	1.5 2.0	V
On-State Drain Current (V_{GS} = −12V, V_{DS} = −25V)	$I_{D(on)}$	1.5			A
Dynamic Characteristics					
Forward Transconductance (V_{DS} = −15V, I_D = −500 mA)	g_{fs}	200	300		mmhos
Input Capacitance (V_{DS} = −25V, V_{GS} = 0, f = 1 MHz)	C_{iss}		110	150	pF
Output Capacitance (V_{DS} = −25V, V_{GS} = 0, f = 1 MHz)	C_{oss}		70	100	pF
Reverse Transfer Capacitance (V_{DS} = −25V, V_{GS} = 0, f = 1 MHz)	C_{rss}		48	60	pF
Switching Characteristics					
Turn-on Time (See Figure 2)	t_{on}			30	ns
Turn-off Time (See Figue 2)	t_{off}			30	ns
Body-Drain Diode Characteristics					
Forward Recovery Time (I_F = −0.5A, See Figure 3)	t_{fr}		40	50	ns
Reverse Recovery Time (I_F = I_R = −0.5A, See Figure 3)	t_{rr}		52	65	ns
Forward Voltage (V_{GS} = 0, I_S = −0.5A)	V_{SD}		1.2		V

Note 1: Pulsed test, 80 μs pulse ≤ 1% duty cycle. **VPMH-30**

Note 2: Electrical specifications are subject to change without notice.

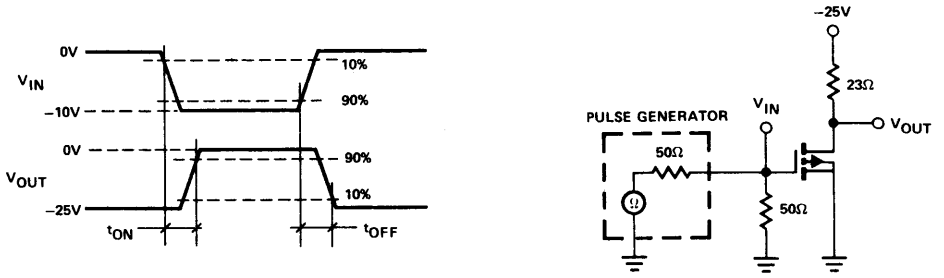


Figure 2. P-Channel Switching Time Test Circuit

POWER RATINGS (25° C ambient)

Test	Unit	Single Transistor	All Four Transistors
Total Power Dissipation	watts	1.30	2.0
Linear Derating Factor	mW/°C	10.4	16
Thermal Resistance	°C/W	96.2	62.5
Thermal Coupling Factor (K) Q_1-Q_4 or Q_2-Q_3 Q_1-Q_2, Q_3-Q_4, Q_1-Q_3, or Q_2-Q_4	 % %	 60 50	

THERMAL COUPLING AND EFFECTIVE THERMAL RESISTANCE

In multiple chip devices, coupling of heat between die occurs. The junction temperature can be calculated as follows:

(1) $\Delta T_{J1} = R_{\theta 1} P_{D1} + R_{\theta 2} K_{\theta} P_{D2} + R_{\theta 3} K_{\theta 3} P_{D3} + R_{\theta 4} K_{\theta 4} P_{D4}$

Where ΔT_{J1} is the change in junction temperature of die $R_{\theta 1-4}$ is the thermal resistance of die 1–4; P_{D1-4} is the power dissipated in die 1–4 and $K_{\theta 2-4}$ is the thermal coupling between die 1 and 2–4.

An effective package thermal resistance can be defined as follows:

(2) $R_{\theta(EFF)} = \Delta T_{J1}/P_{DT}$

where: P_{DT} is the total package power dissipation.

Assuming equal thermal resistance for each die, equation (1) simplifies to:

(3) $\Delta T_{J1} = R_{\theta 1} (P_{D1}+K_{\theta 2} P_{\theta 2}+K_{\theta 3} P_{D3}+K_{\theta 4} P_{D4})$

For the conditions where $P_{D1} = P_{D2} = P_{D3} = P_{D4}$, $P_{DT} = 4P_D$. Equation (3) can be further simplified and by substituting into equation (2) results in:

(4) $R_{\theta(EFF)} = R_{\theta 1} (1 + K_{\theta 2} + K_{\theta 3} + K_{\theta 4})/4$

Values for the coupling factors when the ambient is used as a reference are given in the table above. If significant power is to be dissipated in two die, die at the opposite ends of the package should be used so that lowest possible junction temperatures will result.

INTERNAL BODY DRAIN DIODE (t_{rr} and t_{fr} recovery times)

The internal reverse diodes of Power FETs may be used as catch diodes or free-wheeling diodes. Current ratings for these diodes are the same or higher as the continuous and peak drain current ratings for the MOSFET.

Forward and reverse recovery time is measured using the circuit below. Forward and reverse currents I_F and I_R are equal and are tested at the peak current rating of the MOSFET.

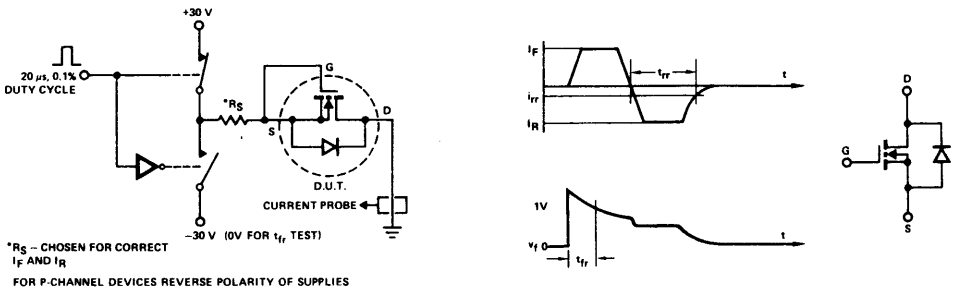


Figure 3. Recovery Time Waveforms

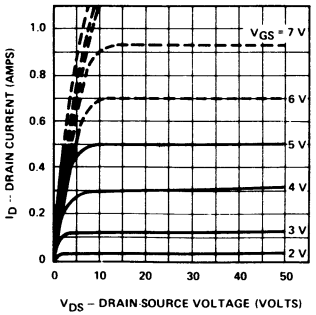
n-channel
enhancement-mode
VMOS Power FETs

Siliconix

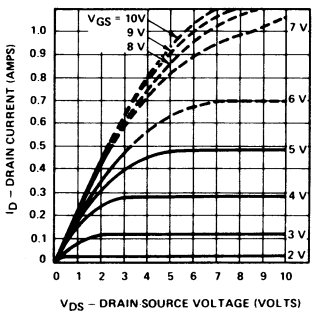
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-237	VN10KM, VK1010, VK1011
	TO-52	VN10KE
Quad	14 pin Plastic	VQ1000J
	14 pin S/B	VQ1000P

TYPICAL PERFORMANCE CURVES (25°C unless otherwise noted)

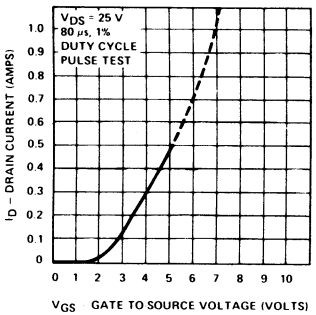
Output Characteristics



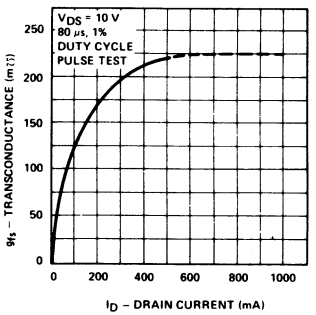
Saturation Characteristics



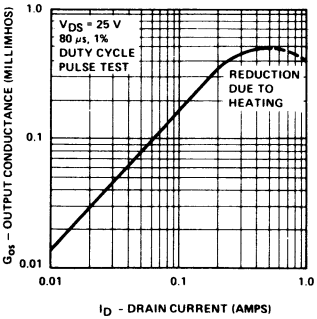
Transfer Characteristics



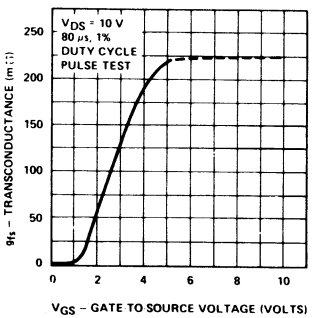
Transconductance vs Drain Current



Output Conductance vs Drain Current



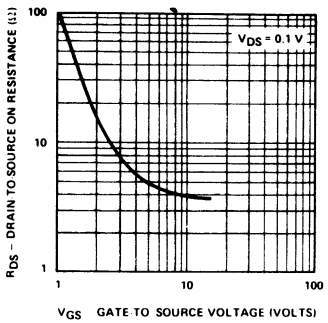
Transconductance vs Gate-Source Voltage



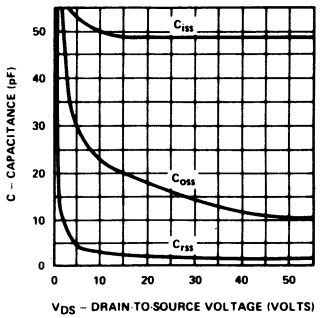
3

TYPICAL PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

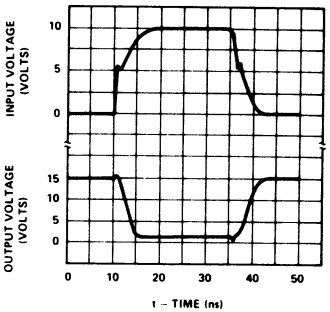
Drain-to-Source ON Resistance vs Gate-to-Source Voltage



Capacitance vs Drain-to-Source Voltage



Switching Waveforms



Switching Time Test Waveforms