

# CA1310E

## RC Phase-Locked-Loop Stereo Decoder

For FM Multiplex Systems

**Features:**

- Low distortion (THD): 0.3% typ.
- Excellent SCA (storecast) rejection: 75 dB typ.
- RC oscillator
- High audio channel separation: 40 dB
- Operates from a wide range of power supplies: 8 to 14 V dc
- Requires only one adjustment for complete alignment
- Drives a stereo indicator lamp up to 75 mA – surge current limiting

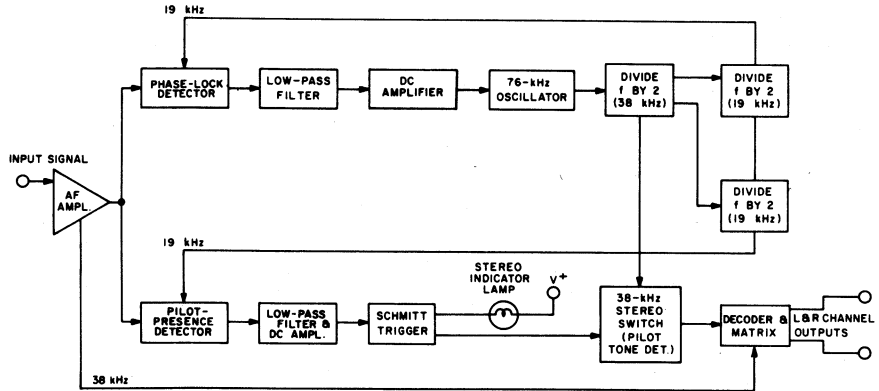


Fig. 1 – Functional block diagram system using the CA1310E.

92CS-23500

RCA-CA1310E is a monolithic silicon integrated circuit RC phase-lock-loop stereo decoder intended for FM solid-state stereo multiplex systems.

The CA1310E is a direct replacement for industry types MC1310P, LM1310, and SN76115N.

This decoder uses a minimum of external components. In addition the stereo decoder requires only one adjustment (oscillator frequency) for complete alignment.

The CA1310E is supplied in a 14-lead dual-in-line plastic package and operates over an ambient temperature range of -40 to +85°C.

### ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS (Referenced to Fig. 3) $V^+ = 12\text{ V}$ $T_A = 25^\circ\text{C}$ Composite Multiplex Input Signal = 560 mV RMS (2.8 V p-p) Only L or R Channel modulated; and with 100-mV RMS (10%) Pilot Level	LIMITS			UNITS
		Min.	Typ.	Max.	
<b>Static Characteristics</b>					
DC Supply Voltage	For 8-V operation, reduce load to 2.7 k $\Omega$	8	–	14	V
Total Current	Lamp "OFF"	–	13	–	mA
<b>Dynamic Characteristics</b>					
Input Impedance		20	50	–	k $\Omega$
Channel Separation (Stereo)	50 Hz – 15 kHz	30	40	–	dB
Audio Output Voltage (For any one channel)		–	485	–	mV RMS
Channel Balance (Monaural)	Pilot Tone "OFF"	–	–	1.5	dB
Capture Range (Permissible tuning error of internal oscillator)		–	$\pm 3.5$	–	%
Total Harmonic Distortion		–	0.3	–	%
Ultrasonic Frequency Rejection:					
19 kHz		–	34.4	–	dB
38 kHz		–	45	–	dB
SCA (Storecast) Rejection	f = 67 kHz, 9-kHz beat note measured with 1-kHz modulation "OFF"	–	75	–	dB
Stereo Switch Level:					
19-kHz Input Level (For lamp on)		–	–	20	mV RMS
19-kHz Input Level (For lamp off)		5	–	–	mV RMS
Maximum Composite (Stereo) Input	0.5% THD	2.8	–	–	V p-p
Maximum Monaural Input	1% THD	2.8	–	–	V p-p

**MAXIMUM RATINGS, Absolute-Maximum Values at  $T_A = 25^\circ\text{C}$**

DC Supply Voltage	14 V
Current (Lamp) at Term. 6	75 mA
Device Dissipation:	
Up to $T_A = 25^\circ\text{C}$	625 mW
Above $T_A = 25^\circ\text{C}$ derate linearly	5 mW/ $^\circ\text{C}$
Ambient Temperature Range:	
Operating	-40 to +85 $^\circ\text{C}$
Storage	-65 to +150 $^\circ\text{C}$
Lead Temperature (During soldering):	
At distance not less than 1/32" (0.79 mm) from case for 10 s max.	+265 $^\circ\text{C}$

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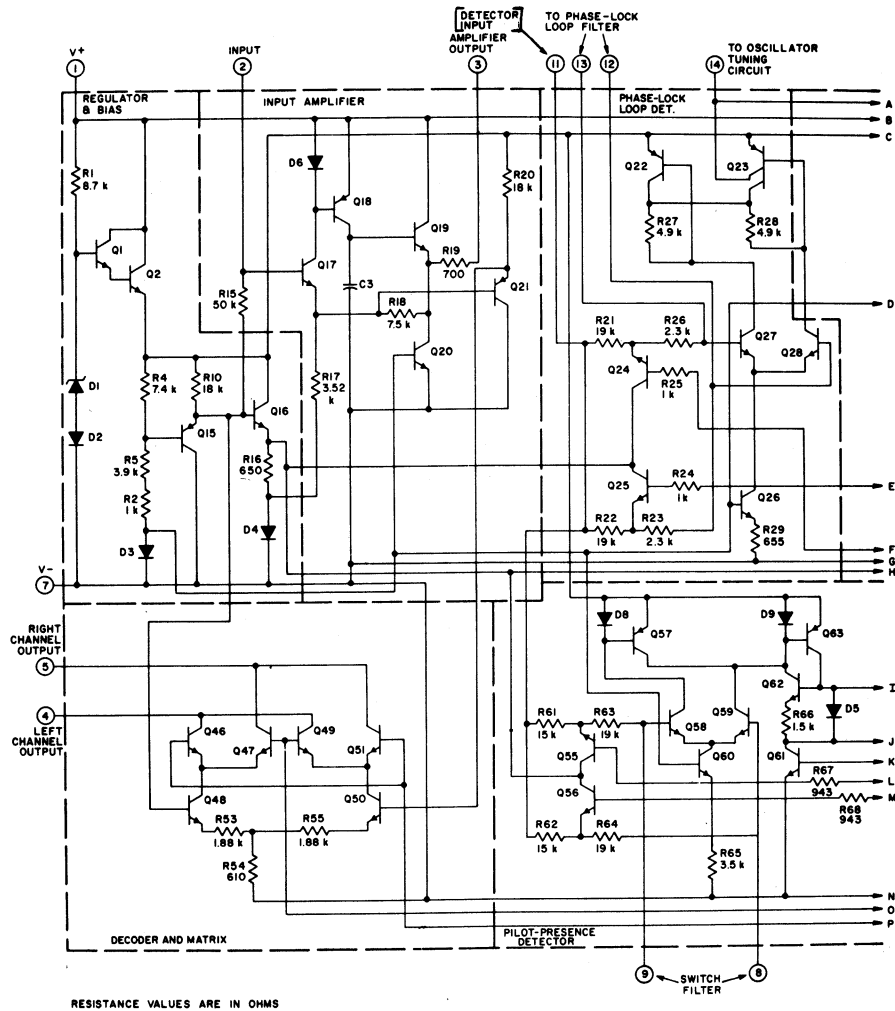


Fig. 2 - Schematic diagram of the CA1310E.

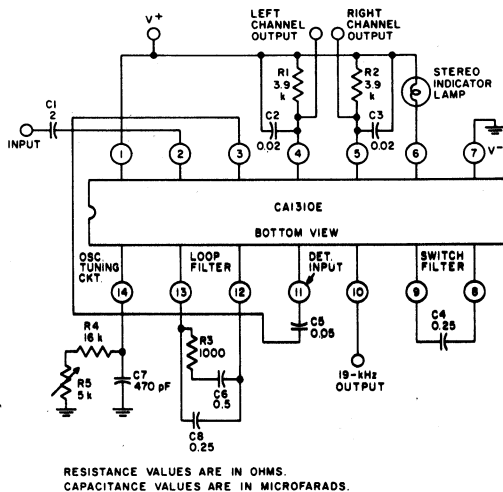


Fig. 3 - Test circuit for measurement of dynamic characteristics.

### NOTES

A buffered 3-volt positive-going square wave is available at Term. 10. The alignment of the free-running oscillator frequency may be checked at this point with a frequency counter.

C1: A lower value input coupling capacitor may be used in place of the 2- $\mu$ F value if reduced separation at low frequencies is acceptable.

C4: The time constant for the stereo switch level detector circuit is calculated by  $C4 \times 53,000$  ohms  $\pm 30\%$  with a maximum dc voltage drop across C4 of 0.25 volt (Term. 8 positive) and a pilot level voltage of 100 mV RMS. Signal voltage across C4 is negligible.

C5: The recommended 0.05- $\mu$ F capacitor provides a 1.75° phase lead at 19 kHz.

R1, R2: Load resistance values are related to supply voltage as follows:  
 Minimum Supply Voltage 8 10 12 V  
 Maximum Load Resistance 2.7 4.3 6.2 k $\Omega$

R3, C6, C8: C8 may be omitted, R3 = 100 ohms and C6 = 0.25  $\mu$ F, if relaxed circuit performance is acceptable.

R4, R5, C7: If a capture range greater than  $\pm 3\%$  typ. is required, reduce value of C7 and increase values of R4, R5 proportionally. However, beat-note distortion is increased at high signal levels because of oscillator-phase jitter. R4, C7 =  $\pm 1\%$  in test circuit and  $\pm 5\%$  in typical application.

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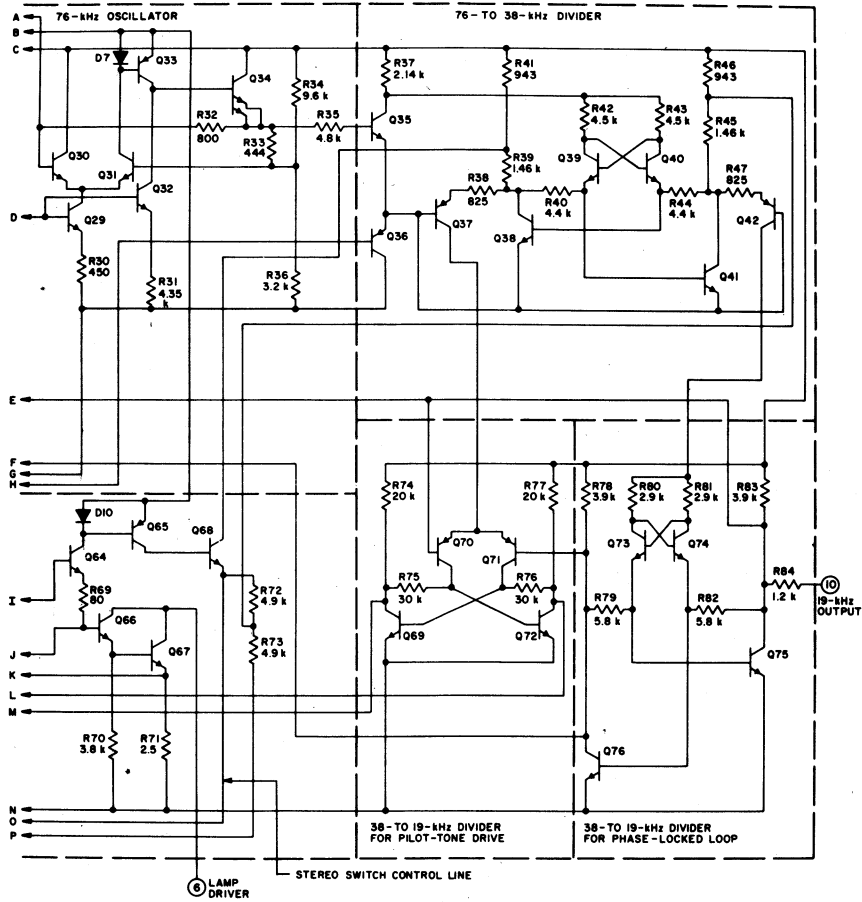


Fig. 2 - Schematic diagram of the CA1310E (Cont'd).