CA1541D

Dual-Input Memory Sense Amplifier

RCA-CA1541D , a monolithic silicon integrated circuit, is a dual-input memory sense amplifier intended for core memory applications.

The sense amplifier, consisting of two differential input amplifiers, a common second stage amplifier, and an output logic gate (See Fig. 1), converts low-level core-memory "1" pulses to saturated logic-level output pulses. Either one of the input amplifiers may be gated ON with a saturated logic signal so that an incoming "1" pulse of positive or negative polarity can be detected from either of two sense lines.

The CA1541D features an external switching threshold adjustment, plus its gate and strobe inputs are compatible with saturated logic levels. The sense amplifier is suitable for operation with core memories having cycle times equal to or greater than 0.4 μs and is unilaterally interchangeable with industry types 1541L and 1441.

The CA1541D is supplied in 14-lead dual-in-line ceramic package and is rated for operation over the full military temperature range of −55°C to +125°C.

Features

- Complete dual input core memory sense amplifier
- Two available outputs: −Saturated logic output
  −Linear output (positive output for either polarity input)
- Nominal threshold voltage: 17 mV
- Adjustable threshold: 10 to 35 mV
- Low threshold uncertainty range: ±3 mV
- Fast overload recovery time: −Differential-Mode: 15 ns typ.
  −Common-Mode: 30 ns typ.
- Independent channel gate and strobe terminals compatible with saturated logic levels
- Suitable for core memories having cycle times ⩾ 0.4 μs
- Input offset voltage: 6 mV max.

MAXIMUM RATINGS, Absolute Maximum Values, at T_A = 25°C

Except for Differential Input Voltage, all voltages are measured with respect to ground (Term. 8).

DC Supply Voltage:	
V^+ (Term. 2)	+10 V
V^- (Term. 7)	−10 V
Differential Input Voltage	±5 V
Common-Mode Input Voltage	±5 V
"A" or "B"-Gate Input Voltage*	V^- to V^+
Strobe Terminal Voltage	V^- to +6V
Output Terminal Load Current	±25 mA
Device Dissipation:	
Up to T_A = 75°C	750 mW
Above T_A = 75°C	Derate Linearly 8 mW/°C
Ambient Temperature Range:	
Operating	−55 to +125 °C
Storage	−65 to +150 °C
Lead Temperature (during soldering):	
At distance not less than 1/32 inch (0.79 mm) from case for 10 seconds max.	+265°C

*Note: The "A" or "B"-Gate Input Voltage is also referred to, as the Channel-Gate Input Voltage.

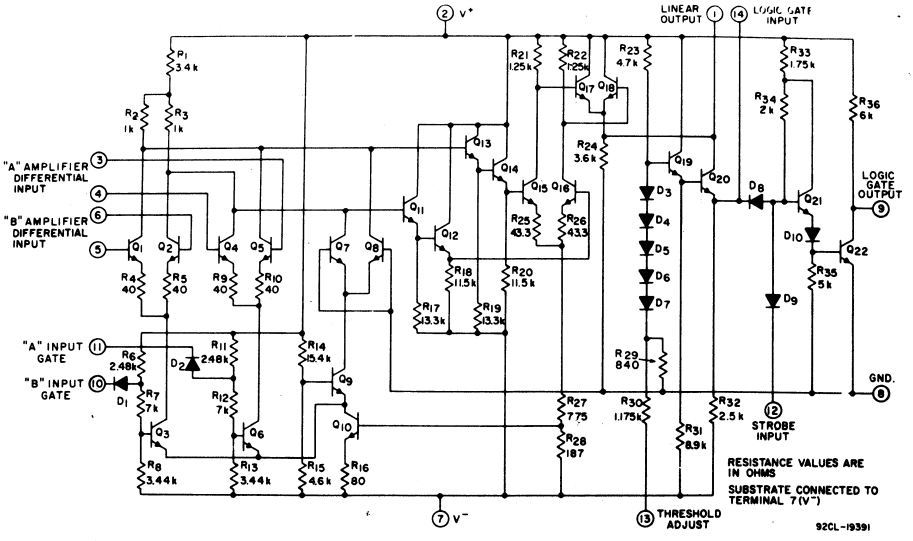


Fig. 2 – Schematic diagram of the CA1541D.

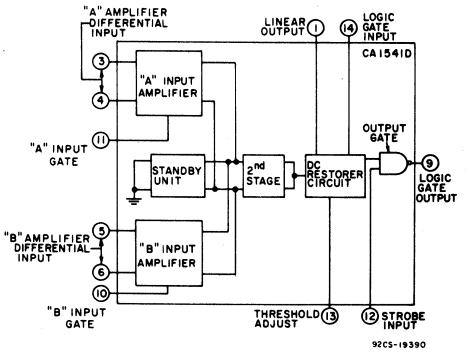


Fig. 1 – Functional block diagram of the CA1541D.

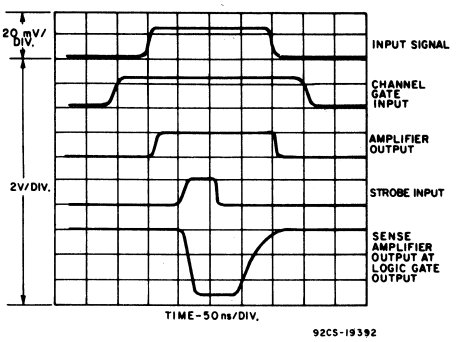


Fig. 3 – Typical operational wave forms.

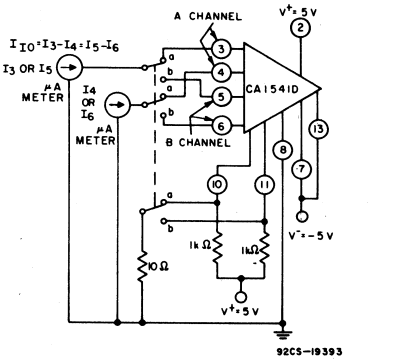


Fig. 4 – Input bias (I_{IB}) and input-offset current (I_{IO}) test circuit.

CA1541D

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS: $V^+ = 5V$, $V^- = -5V$; V_{TH} ADJ. = $-5V \pm 1\%$, (Term. 13) $C_{EXT} = 0.01\ \mu F$; $T_A = 25°C$ (unless indicated otherwise)		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Static (DC) Characteristics							
Power Dissipation	P_D			–	140	180	mW
Input Offset Current	I_{IO}			–	1	2	μA
Input Bias Current:							
$T_A = 25°C$	I_{IB}		$V_5 = V_6 = V_3 = V_4 = 0$	–	5	25	μA
$T_A = -55°C$				–	–	50	
Output Voltage:							
High	V_{OH}	$I_{OM} = 200\ \mu A$		3	–	–	V
Low –							
$T_A = 25°C$	V_{OL}	$V_{14} = 5\ V$, $I_9 = 10\ mA$		–	–	350	mV
$T_A = 125°C$				–	–	400	
Strobe Load Current	I_S	$V_{12} = 0$		–	–	1.5	mA
Strobe Reverse Current:							
$T_A = 25°C$	I_{SR}	$V_{12} = 5V$		–	–	2	μA
$T_A = 125°C$				–	–	25	
Input Gate Load Current	I_G	$V_{10} = V_{11} = 0$		–	–	2.5	mA
Input Gate Reverse Current:							
$T_A = 25°C$	I_{GR}	$V_{10} = V_{11} = 5V$		–	–	2	μA
$T_A = 125°C$				–	–	25	
Switching Characteristics							
Input Threshold Voltage:							
$T_A = 25°C$	V_{TH}			14	17	20	mV
$T_A = -55$ to $125°C$				12	17	22	
Input Offset Voltage	V_{IO}			–	1	6	mV
Input Gate Voltage:							
High	V_{GH}	$V_3 = V_5 = 25$ mV,		–	1.6	–	V
Low	V_{GL}	$V_4 = V_6 = 0$		–	0.7	–	
Common-Mode Range:							
Input Gate High	V_{CM}			–	±1.5	–	V
Input Gate Low				–	±1.5	–	
Differential-Mode Range:							
Input Gate High	V_{DH}			–	±600	–	mV
Input Gate Low	V_{DL}			–	±1.5	–	V
Propagation Delay:							
Input to Amplifier Output	t_{IA}	$V_3 = 25$ mV (pulsed),		–	10	15	ns
Input to Output	t_{IO}	$V_{12} = 2V$		–	20	30	
Strobe to Output	t_{SO}	$V_3 = V_4 = V_5 = V_6 = 0$, $V_{12} = 2V$ (pulsed)		–	15	20	
Gate Input to Amplifier Output	t_{GA}	$V_{11} = 2V$ (pulsed)		–	10	15	
Gate Input to Amplifier Input	t_{GI}	$V_3 = 25$ mV		–	30	35	
Common-Mode Recovery Time:							
Input Gate High	t_{CMR}	$V_3 = V_5 = 1.5\ V$		–	15	30	ns
Input Gate Low				–	15	30	
Differential-Mode Recovery Time:							
Input Gate High	t_{DR}	$V_3 = V_5 = 400$ mV		–	30	–	ns
Input Gate Low				–	0	–	

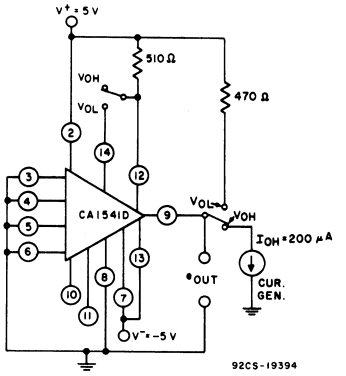
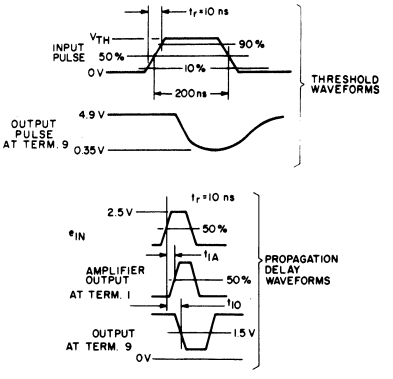


Fig. 5 – Test circuit for measurement of low (V_{OL}) and high (V_{OH}) output voltage levels.



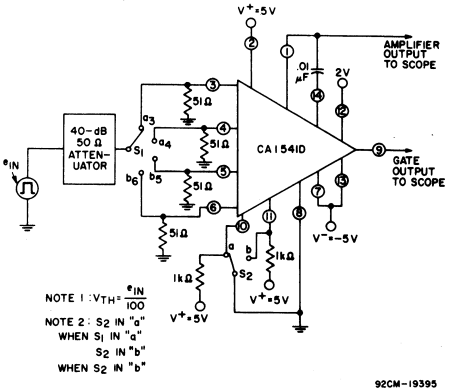


Fig. 6 – Threshold propagation delay, gate and input-offset test circuit with associated pulse wave forms.

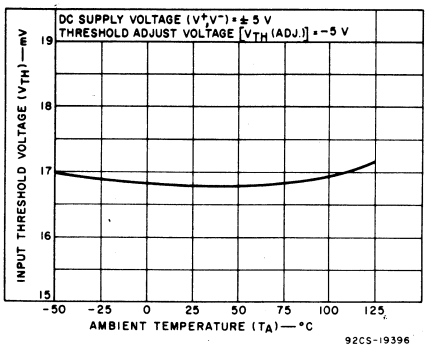


Fig. 7a – Input V_{TH} vs. T_A.

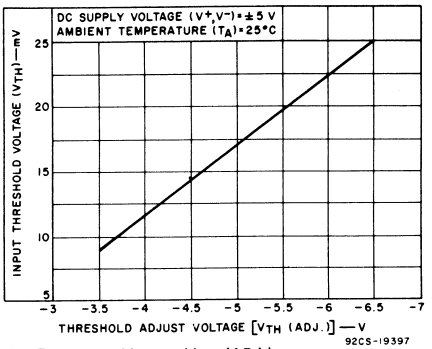


Fig. 7b – Input V_{TH} vs. V_{TH} (ADJ.).

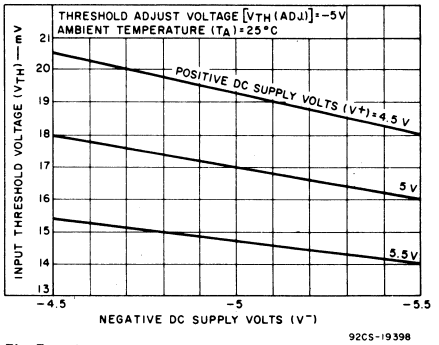


Fig. 7c – Input V_{TH} vs V^-.

CA1541D

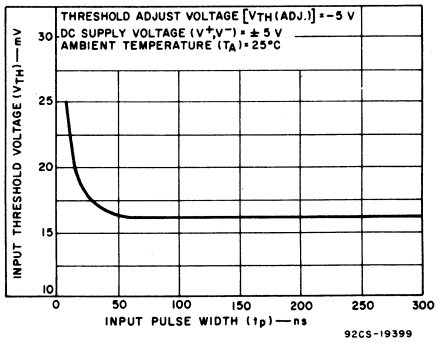
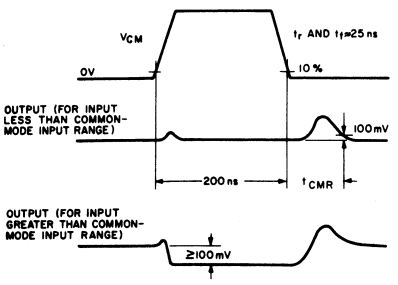


Fig. 7d – Input V_{TH} vs. input pulse width.



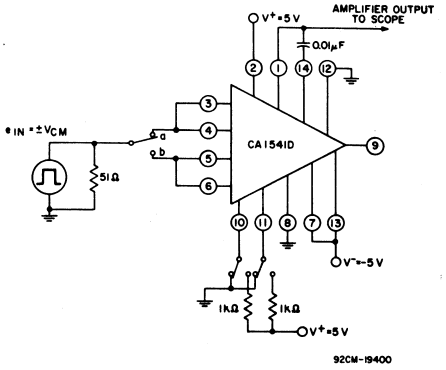


Fig. 8 – Common-mode input range test circuit with associated pulse wave forms.

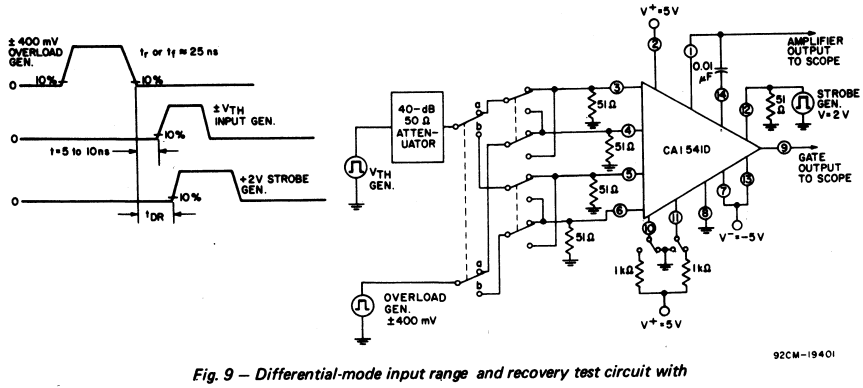


Fig. 9 – Differential-mode input range and recovery test circuit with associated pulse wave forms.

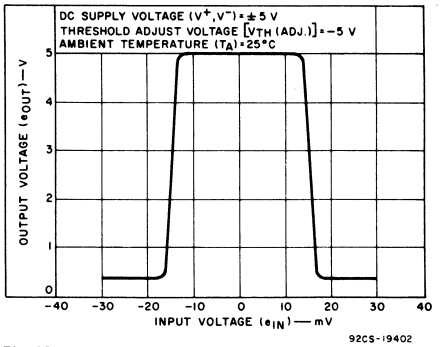


Fig. 10 – Input-output transfer characteristics.

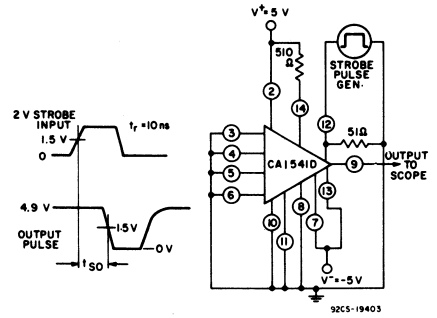


Fig. 11 – Strobe to output test circuit with associated pulse wave-forms.

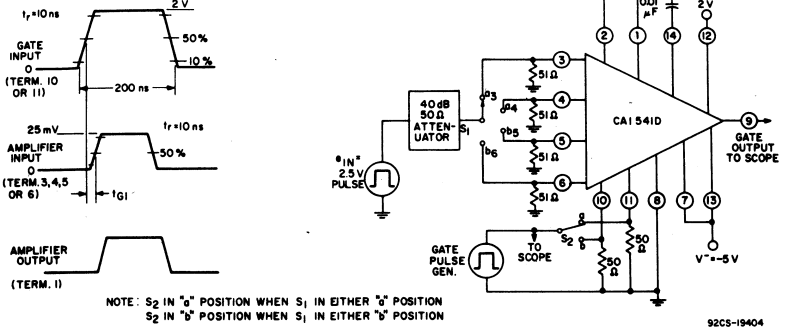


Fig. 12 – Gate input to amplifier input (t_{GI}) test circuit with associated pulse wave forms.

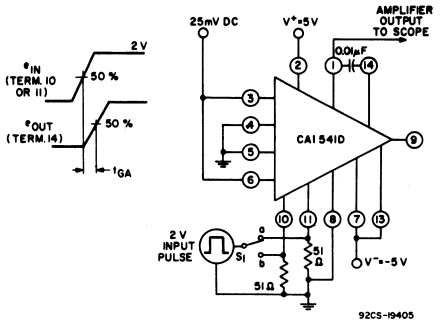


Fig. 13 – Gate input to amplifier output (t_{GA}) with associated pulse wave forms.