CA3011, CA3012

Wide-Band Amplifiers

FEATURES & APPLICATIONS

- exceptionally high amplifier gain: power gain at 4.5 MHz – 75 dB typ.
- excellent limiting characteristics – Input limiting voltage (knee) = 600 μV typ. at 10.7 MHz
- wide frequency capability – 100 kHz to > 20 MHz
- supplied in the hermetic 10-lead TO-5 style package

ABSOLUTE-MAXIMUM VOLTAGE LIMITS AT T_A = 25° C

Indicated voltage limits for each terminal can be applied under the specified voltage conditions for other terminals. All voltages are with respect to ground (Terminal 8).

NOTE: TERMINALS 6, 7, AND 9 OF RCA-CA3011 AND CA3012 ARE USED FOR INTERNAL CONNECTIONS. DO NOT APPLY VOLTAGES OR MAKE EXTERNAL CONNECTIONS TO THESE TERMINALS.

CA3011

TERMINAL	VOLTAGE LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS						
			1	2	3	4	5	8	10
1	-3	+3	–	Same as 1	Do Not Apply External Voltage	+2.5 to +7.5	+7.5	Ground	+7.5
2	-3	+3	Same as 2	–		+2.5 to +7.5	+7.5	Ground	+7.5
3	-3	+3	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Ground	+7.5
4	+2.5	+7.5	-3 to +3	Same as 1		–	+7.5	Ground	+7.5
5	0	+10	-3 to +3	Same as 1		+2.5 to +7.5	–	Ground	+7.5
8	-3	+7.5	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Ground	+7.5
10	0	+10	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Ground	–
CASE	INTERNALLY CONNECTED TO TERMINAL NO.8 (GROUND TERMINAL)								

CA3012

TERMINAL	VOLTAGE LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS						
			1	2	3	4	5	8	10
1	-3	+3	–	Same as 1	Do Not Apply External Voltage	+2.5 to +10	+10	Ground	+10
2	-3	+3	Same as 2	–		+2.5 to +10	+10	Ground	+10
3	-3	+3	-3 to +3	Same as 1		+2.5 to +10	+10	Ground	+10
4	+2.5	+10	-3 to +3	Same as 1		–	+10	Ground	+10
5	0	+13	-3 to +3	Same as 1		+2.5 to +10	–	Ground	+10
8	-3	+10	-3 to +3	Same as 1		+2.5 to +10	+10	Ground	+10
10	0	+13	-3 to +3	Same as 1		+2.5 to +10	+10	Ground	–
CASE	INTERNALLY CONNECTED TO TERMINAL NO.8 (GROUND TERMINAL)								

OPERATING-TEMPERATURE RANGE ..... -55 to +125° C
STORAGE-TEMPERATURE RANGE ..... -65 to +150° C

LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. ..... +265°C

MAXIMUM INPUT-SIGNAL VOLTAGE:
Between Terminals 1 and 2 ..... ±3 V

MAXIMUM DEVICE DISSIPATION ..... 300 mW

RECOMMENDED MINIMUM DC SUPPLY VOLTAGE (V_{CC}) .. 5.5 V

Example of Use of LIMITS TABLE:

For RCA-3012, a maximum voltage of ±3 volts may be applied to Terminal 1 under the following conditions:

Terminal 2 is at the same dc potential as Terminal 1
Terminal 3: do not apply external voltage
Terminal 4 is at any dc potential between +2.5 and +10 volts
Terminal 5 is at a dc potential of +10 volts
Terminals 6, 7, and 9 are at 0 dc potential (NOT USED)
Terminal 8 is at dc ground potential
Terminal 10 is at a dc potential of +10 volts

BLOCK DIAGRAM OF TYPICAL FM RECEIVER USING RCA-CA3011 OR CA3012 INTEGRATED CIRCUIT WIDE-BAND AMPLIFIER

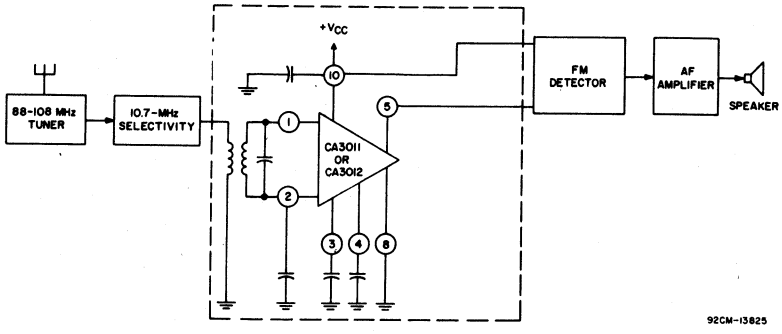


Fig. 4

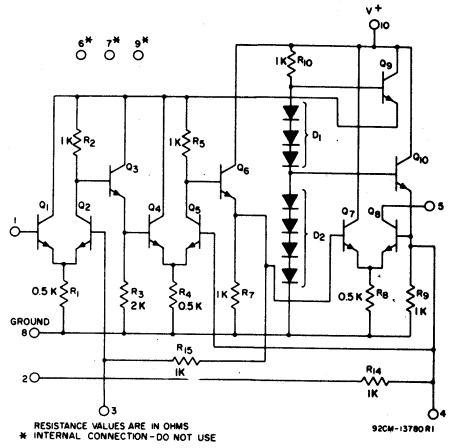


Fig. 1 – Schematic diagram for CA3011 and CA3012.

INPUT-IMPEDANCE COMPONENTS VS FREQUENCY

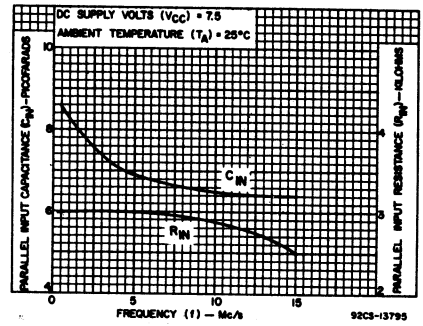


Fig. 2

OUTPUT-IMPEDANCE COMPONENTS VS FREQUENCY

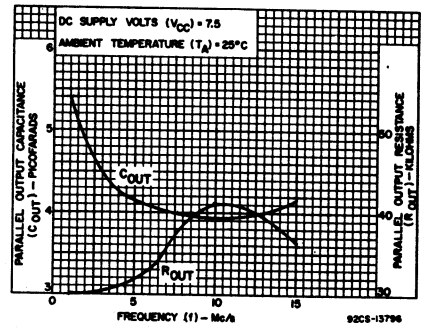


Fig. 3

VOLTAGE GAIN AND INPUT LIMITING VOLTAGE VS FREQUENCY

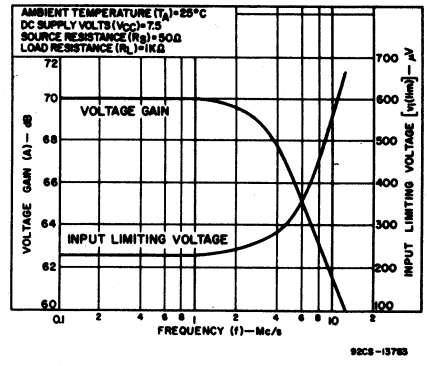


Fig. 5

CA3011, CA3012

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS				LIMITS						UNITS	TYPICAL CHARACTERISTICS CURVES
		SETUP & PROCEDURE	FREQUENCY	DC SUPPLY VOLTAGE	AMBIENT TEMPERATURE	RCA CA3011			RCA CA3012				
		Fig.	Mc/s	Volts	°C	Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
Total Device Dissipation*	P_T	6	-	6	-55	-	80	-	66	80	135	mW	
					+25	60	90	133	66	90	121	mW	
					+125	-	70	-	65	70	121	mW	
			-	7.5	-55	-	130	-	97	130	190	mW	
					+25	95	120	187	97	120	167	mW	
					+125	-	100	-	95	100	167	mW	
			-	10	-55	-	-	-	150	210	275	mW	
					+25	-	-	-	150	190	255	mW	
					+125	-	-	-	150	160	255	mW	
Voltage Gain**	A	9	1	6	-55	-	55	-	50	55	-	dB	
					+25	60	66	-	60	66	-	dB	
					+125	-	61	-	50	61	-	dB	
		9	1	7.5	-55	-	59	-	55	59	-	dB	
					+25	65	70	-	65	70	-	dB	
					+125	-	65	-	55	65	-	dB	
		9	1	10	-55	-	-	-	55	61	-	dB	
					+25	-	-	-	65	71	-	dB	
					+125	-	-	-	55	66	-	dB	
		9	4.5	7.5	+25	60	67	-	60	67	-	dB	5
			10.7	7.5	+25	55	61	-	55	61	-	dB	
Input-Impedance Components: Parallel Input Resistance	R_{IN}	7	4.5	7.5	+25	-	3	-	-	3	-	kΩ	2
Parallel Input Capacitance	C_{IN}	7	4.5	7.5	+25	-	7	-	-	7	-	pF	2
Output Impedance Components: Parallel Output Resistance	R_{OUT}	8	4.5	7.5	+25	-	31.5	-	-	31.5	-	kΩ	3
Parallel Output Capacitance	C_{OUT}	8	4.5	7.5	+25	-	4.2	-	-	4.2	-	pF	3
Noise Figure	NF	10	4.5	7.5	+25	-	8.7	-	-	8.7	-	dB	
Input Limiting Voltage (Knee)	$v_{i(lim)}$	9	4.5	7.5	+25	-	300	450	-	300	400	μV	

* The total current drain may be determined by dividing P_T by V_{CC}.

** Recommended minimum dc supply voltage (V_{CC}) is 5.5 V. Nominal load current flowing into terminal 5 is 1.5 mA at 7.5 V.

DISSIPATION TEST SETUP

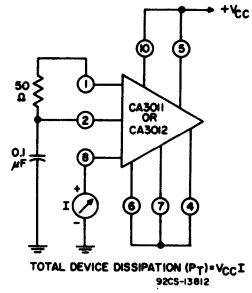


Fig. 6

INPUT-IMPEDANCE COMPONENTS TEST SETUP

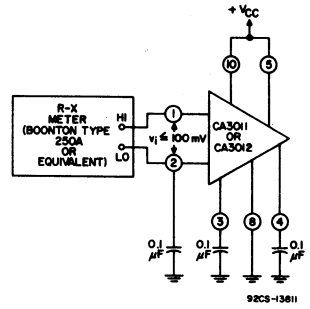


Fig. 7

OUTPUT-IMPEDANCE COMPONENTS TEST SETUP

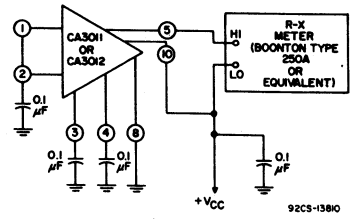


Fig. 8

VOLTAGE-GAIN TEST SETUP

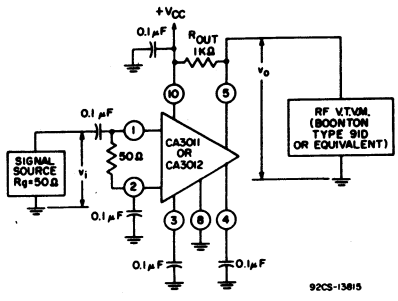


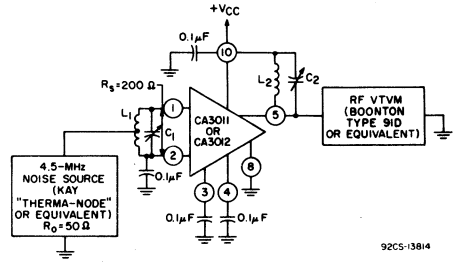
Fig. 9

PROCEDURES

A - Voltage Gain:
1) Set input frequency at desired value, v_i = 100 μV rms.
2) Record v_o.
3) Calculate Voltage Gain A from $A = 20 \log_{10} v_o/v_i$
4) Repeat Steps 1, 2, and 3 for each frequency and/or for temperature desired.

B - Input Limiting Voltage (Knee):
1) Repeat Steps A1 and A2, using v_i = 100 mV
2) Decrease v_i to the level at which v_o is 3 dB below its value for v_i = 100 mV.
3) Record v_i as Input Limiting Voltage (Knee).

NOISE FIGURE TEST SETUP



L_1 = 82 μH, center-tapped
L_2 = 2.36 μH
C_1,C_2 = Arco Type 423 padder, or equivalent

Fig. 10

CA3013, CA3014

Wide-Band Amplifier-Discriminators

SCHEMATIC DIAGRAM FOR CA3013 AND CA3014

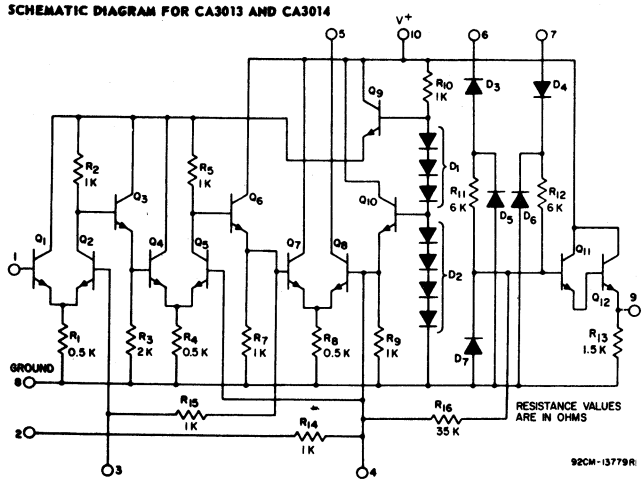


Fig. 1

BLOCK DIAGRAM OF TYPICAL TELEVISION RECEIVER USING RCA INTEGRATED-CIRCUIT SOUND-IF AMPLIFIER AND DETECTOR SECTION

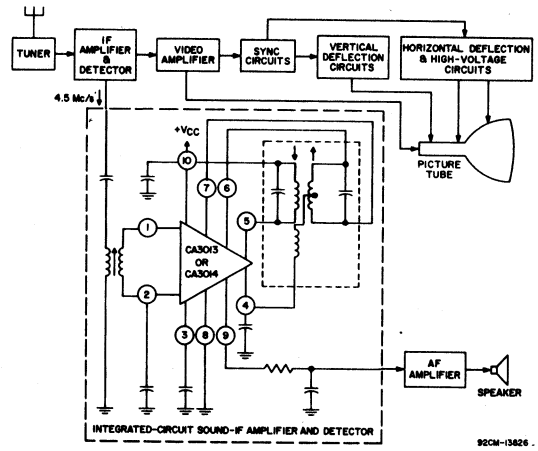


Fig. 2

FEATURES & APPLICATIONS:

- **exceptionally high gain:**
  power gain at 4.5 MHz — 75 dB typ.
- **excellent limiting characteristics — input limiting voltage (knee) = 300 μV typ. at 4.5 MHz**
- **excellent AM rejection: > 50 dB at 4.5 MHz**
- **high audio-voltage recovery — 220 mV typ. at 4.5 MHz 25 kHz deviation**
- **wide frequency capability — 100 kHz to > 20 MHz**
- **comprehensive circuit functions:**
  if amplifier, AM and noise limiter, FM detector, audio preamplifier
- **supplied in the hermetic 10-lead TO-5 style package**

TYPICAL CHARACTERISTICS AND TEST SETUPS

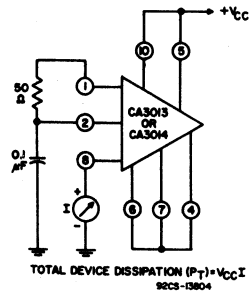


Fig.3

ABSOLUTE-MAXIMUM VOLTAGE LIMITS AT T_A = 25° C

Indicated voltage limits for each terminal can be applied under the specified voltage conditions for other terminals. All voltages are with respect to ground (Terminal 8).

CA3013

TERMINAL	VOLTAGE LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS									
			1	2	3	4	5	6	7	8	9	10
1	-3	+3	-	Same as 1	Do Not Apply External Voltage	+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	AF Output	+7.5
2	-3	+3	Same as 2	-		+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	AF Output	+7.5
3	-3	+3	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	AF Output	+7.5
4	+2.5	+7.5	-3 to +3	Same as 1		-	+7.5	Same as 4	Same as 4	Ground	AF Output	+7.5
5	0	+10	-3 to +3	Same as 1		+2.5 to +7.5	-	Same as 4	Same as 4	Ground	AF Output	+7.5
6	+2.5	+7.5	-3 to +3	Same as 1		Same as 6	+7.5	-	Same as 4	Ground	AF Output	+7.5
7	+2.5	+7.5	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Same as 4	-	Ground	AF Output	+7.5
8	-3	+7.5	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	AF Output	+7.5
9	0	+7.5	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	-	+7.5
10	0	+10	-3 to +3	Same as 1		+2.5 to +7.5	+7.5	Same as 4	Same as 4	Ground	AF Output	-
CASE	INTERNALLY CONNECTED TO TERMINAL No.8 (GROUND TERMINAL)											

CA3014

TERMINAL	VOLTAGE LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS									
			1	2	3	4	5	6	7	8	9	10
1	-3	+3	-	Same as 1	Do Not Apply External Voltage	+2.5 to +10	+10	Same as 4	Same as 4	Ground	AF Output	+10
2	-3	+3	Same as 2	-		+2.5 to +10	+10	Same as 4	Same as 4	Ground	AF Output	+10
3	-3	+3	-3 to +3	Same as 1		+2.5 to +10	+10	Same as 4	Same as 4	Ground	AF Output	+10
4	+2.5	+10	-3 to +3	Same as 1		-	+10	Same as 4	Same as 4	Ground	AF Output	+10
5	0	+13	-3 to +3	Same as 1		+2.5 to +10	-	Same as 4	Same as 4	Ground	AF Output	+10
6	+2.5	+10	-3 to +3	Same as 1		Same as 6	+10	-	Same as 4	Ground	AF Output	+10
7	+2.5	+10	-3 to +3	Same as 1		+2.5 to +10	+10	Same as 4	-	Ground	AF Output	+10
8	-3	+10	-3 to +3	Same as 1		+2.5 to +10	+10	Same as 4	Same as 4	Ground	AF Output	+10
9	0	+10	-3 to +3	Same as 1		+2.5 to +10	+10	Same as 4	Same as 4	Ground	-	+10
10	0	+13	-3 to +3	Same as 1		+2.5 to +10	+10	Same as 4	Same as 4	Ground	AF Output	-
CASE	INTERNALLY CONNECTED TO TERMINAL No.8 (GROUND TERMINAL)											

OPERATING-TEMPERATURE RANGE	55 to +125°C
STORAGE-TEMPERATURE RANGE	65 to +150°C
LEAD TEMPERATURE (During Soldering): At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max	+265°C
MAXIMUM INPUT-SIGNAL VOLTAGE: Between Terminals 1 and 2	± 3 V
MAXIMUM DEVICE DISSIPATION	300 mW
RECOMMENDED MINIMUM DC SUPPLY VOLTAGE (V_{CC})	5.5 V

Example of use of LIMITS TABLE:

For RCA-CA3013, a maximum voltage of ±3 volts may be applied to Terminal 1 under the following conditions:

Terminal 2 is at the same dc potential as Terminal 1
Terminal 3: do not apply external voltage
Terminal 4 is at any dc potential between +2.5 and +7.5 volts
Terminal 5 is at a dc potential of +7.5 volts
Terminals 6 and 7 are at the same dc potential as Terminal 4
Terminal 8 is at dc ground potential
Terminal 9 is used as the af output terminal
Terminal 10 is at a dc potential of +7.5 volts

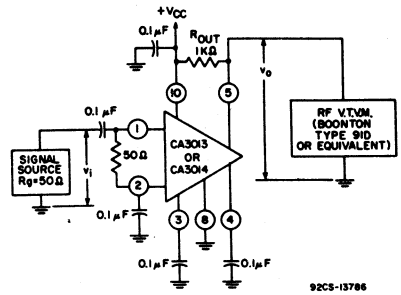
CA3013, CA3014

ELECTRICAL CHARACTERISTICS (See Page 8 for Definitions of Terms)	SYMBOLS	TEST CONDITIONS: SETUP & PROCEDURE	FREQUENCY f	DC SUPPLY VOLTAGE V_{CC}	AMBIENT TEMPERATURE T_A	LIMITS: RCA CA3013 Min.	Typ.	Max.	RCA CA3014 Min.	Typ.	Max.	UNITS	TYPICAL CHARACTERISTICS CURVES
		Fig.	Mc/s	volts	°C								Fig.
Total Device Dissipation*	P_T	3	–	6	-55	–	80	–	73	80	120	mW	
					+25	60	90	133	73	90	110	mW	
					+125	–	70	–	60	70	110	mW	
		3	–	7.5	-55	–	130	–	106	130	170	mW	
					+25	87	120	187	106	120	150	mW	
					+125	–	100	–	90	100	150	mW	
		3	–	10	-55	–	–	–	165	210	250	mW	
					+25	–	–	–	165	190	230	mW	
					+125	–	–	–	150	160	230	mW	
Voltage Gain**	A	4	1	6	-55	–	55	–	50	55	–	dB	
					+25	60	66	–	60	66	–	dB	
					+125	–	61	–	50	61	–	dB	
		4	1	7.5	-55	–	59	–	55	59	–	dB	
					+25	65	70	–	65	70	–	dB	
					+125	–	65	–	55	65	–	dB	
		4	1	10	-55	–	–	–	55	61	–	dB	
					+25	–	–	–	65	71	–	dB	
					+125	–	–	–	55	66	–	dB	
		4	4.5	7.5	+25	60	67	–	60	67	–	dB	5
			10.7	7.5	+25	55	60	–	55	60	–	dB	
Input-Impedance Components: Parallel Input Resistance	R_{IN}	6	4.5	7.5	+25	–	3	–	–	3	–	kΩ	7
Parallel Input Capacitance	C_{IN}	6	4.5	7.5	+25	–	7	–	–	7	–	pF	7
Output-Impedance Components: Parallel Output Resistance	R_{OUT}	8	4.5	7.5	+25	–	31.5	–	–	31.5	–	kΩ	9
Parallel Output Capacitance	C_{OUT}	8	4.5	7.5	+25	–	4.2	–	–	4.2	–	pF	9
Noise Figure	NF	10	4.5	7.5	+25	–	8.7	–	–	8.7	–	dB	11
Input Limiting Voltage (Knee)	v_i(lim)	14	4.5	7.5	+25	–	300	450	–	300	400	μV	13
Recovered AF Voltage	v_o(af)	14	4.5	6	+25	–	155	–	–	155	–	mV	13
				7.5	+25	128	188	–	135	188	–	mV	
				10	+25	–	–	–	–	220	–	mV	
Amplitude-Modulation Rejection	AMR	15	4.5	7.5	+25	–	50	–	–	50	–	dB	–
Discriminator Output Resistance	R_O(disc)	–	4.5	7.5	+25	–	60	–	–	60	–	Ω	–
Total Harmonic Distortion	THD	14	4.5	7.5	+25	–	1.8	–	–	1.8	–	%	12

* Total current drain may be determined by dividing P_T by V_{CC}.

** Recommended minimum dc supply voltage (V_{CC}) is 5.5 V. Nominal load current flowing into terminal 5 is 1.5 mA at 7.5 V.

VOLTAGE-GAIN TEST SETUP



PROCEDURE:

1) Set input frequency at desired value, v_i = 100 μV rms.
2) Record v_o.
3) Calculate Voltage Gain A from A = 20 $\log_{10} v_o/v_i$.
4) Repeat Steps 1, 2, and 3 for each frequency and/or temperature desired.

Fig. 4

VOLTAGE GAIN vs. FREQUENCY

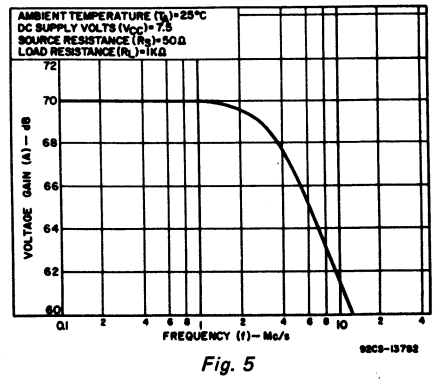


Fig. 5

INPUT-IMPEDANCE COMPONENTS TEST SETUP

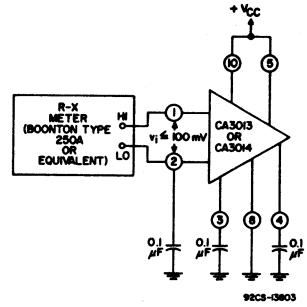


Fig. 6

INPUT-IMPEDANCE COMPONENTS vs. FREQUENCY

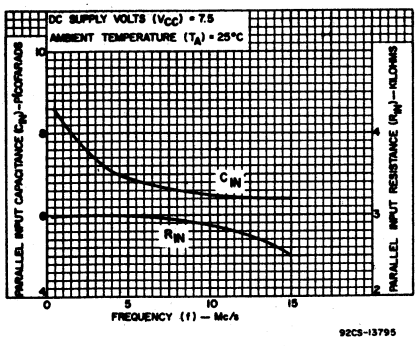


Fig. 7

OUTPUT-IMPEDANCE COMPONENTS TEST SETUP

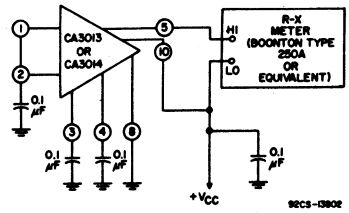


Fig. 8

OUTPUT-IMPEDANCE COMPONENTS vs. FREQUENCY

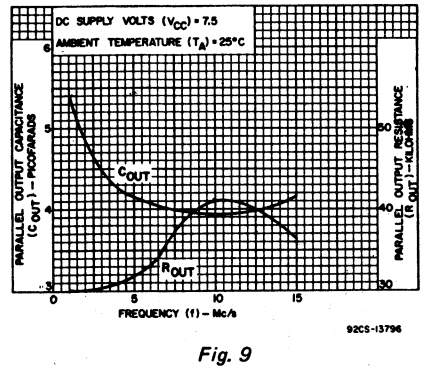
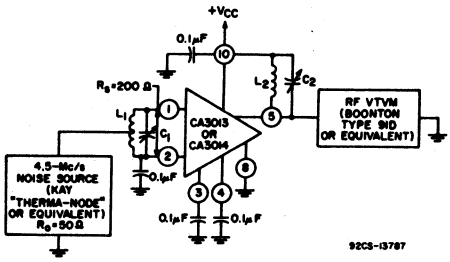


Fig. 9

CA3013, CA3014

NOISE FIGURE TEST SETUP



L_1 = 82 μH, center-tapped

L_2 = 2.36 μH

C_1, C_2 = Arco Type 423 padder, or equivalent

Fig. 10

NOISE FIGURE vs. DC SUPPLY VOLTAGE

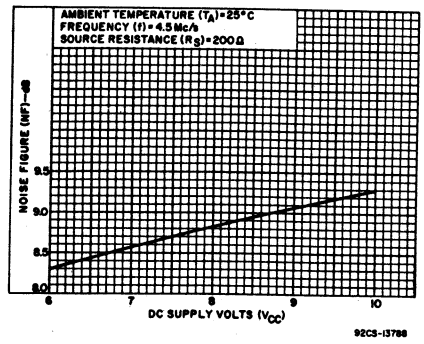


Fig. 11

TOTAL HARMONIC DISTORTION vs. DC SUPPLY VOLTAGE

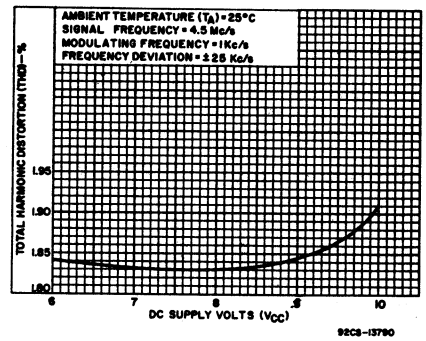
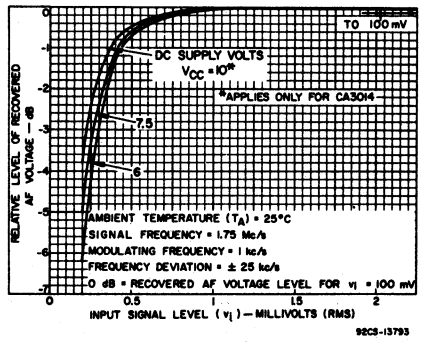


Fig. 12

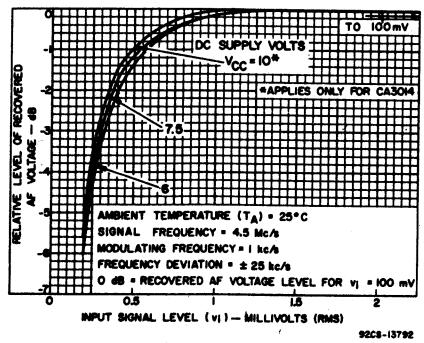
INPUT LIMITING VOLTAGE (KNEE) AND RECOVERED AF VOLTAGE

at 1.75 Mc/s



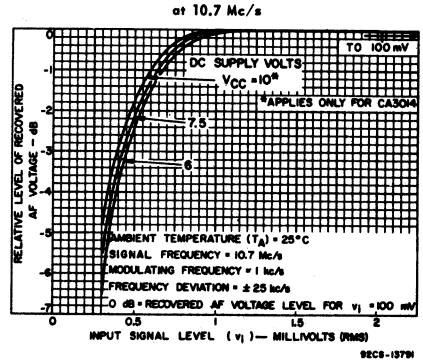
(a)

at 4.5 Mc/s



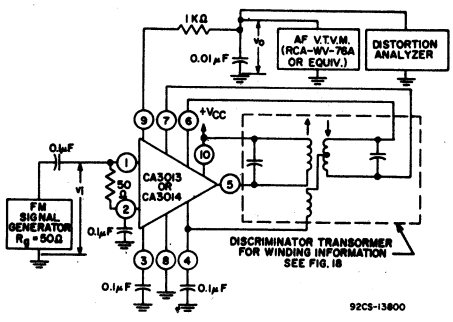
(b)

at 10.7 Mc/s



(c)

Fig. 13



PROCEDURE:

A - Recovered-AF Voltage Output:

1) Set input frequency = 4.5 Mc/s, v_i = 100 mV rms, modulating frequency = 1 kc/s, frequency deviation = ±25 kc/s.

2) Record v_o as Recovered-AF Voltage Output.

B - Input Limiting Voltage (Knee):

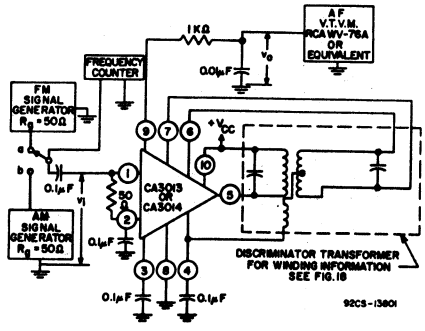
1) Repeat Steps A1 and A2, using v_i = 100 mV rms.

2) Decrease v_i to the level at which v_o is 3 dB below its value for v_i = 100 mV.

3) Record v_i as Input Limiting Voltage (Knee).

INPUT LIMITING VOLTAGE, RECOVERED AF VOLTAGE, AND TOTAL HARMONIC DISTORTION TEST SETUP

Fig. 14



PROCEDURE:

1) With Switch S in position "a", set input frequency = 4.5 Mc/s, v_i = 10 mV rms, modulating frequency = 1 kc/s, frequency deviation = ±25 kc/s.

2) Record v_o.

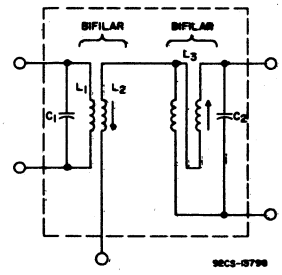
3) Place Switch S in position "b", and set input frequency = 4.5 Mc/s, v_i = 10 mV rms, modulating frequency = 1 kc/s, % modulation = 50.

4) Measure v_o, and record value in dB below value in Step 2 as AM Rejection.

AM-REJECTION TEST SETUP

Fig. 15

DISCRIMINATOR TRANSFORMER SCHEMATIC



(a)

CONSTRUCTION DETAILS OF DISCRIMINATOR TRANSFORMERS SHOWN IN FIGS. 2, 14 AND 15

Coil-Form Outside Diameter = 7/32 inch

Slugs: Radio Industries, Inc. Type "E" Material, or equivalent

Wire Type: "GRIPEZE"*, or equivalent

Operating Frequency Mc/s	Wire Size (AWG #)	Turns L_1▲	Turns L_2▲	Turns L_3	C_1 pF	C_2 pF
1.75	40	44	20	44 total (22 bifilar wound)	820	820
4.5	36	18	7	22 total (11 bifilar wound)	560	330
10.7	36	18	18	18 total (9 bifilar wound)	100	100

* Registered Trade Mark, Phelps-Dodge Copper Products.

▲ wound bifilar.

NOTE: The mutual coupling between L_1 and L_2 is adjusted for the desired degree of linearity.

(b)

Fig. 16

CA3018, CA3018A

General-Purpose Transistor Arrays

TWO ISOLATED TRANSISTORS AND A DARLINGTON-CONNECTED TRANSISTOR PAIR

For Low-Power Applications at Frequencies from DC Through the VHF Range

The CA3018 and CA3018A consist of four general purpose silicon n-p-n transistors on a common monolithic substrate.

Two of the four transistors are connected in the Darlington configuration. The substrate is connected to a separate terminal for maximum flexibility.

The transistors of the CA3018 and the CA3018A are well suited to a wide variety of applications in low-power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits but in addition they provide the advantages of close electrical and thermal matching inherent in integrated circuit construction.

The CA3018A is similar to the CA3018 but features tighter control of current gain, leakage, and offset parameters making it suitable for more critical applications requiring premium performance.

APPLICATIONS

- General use in signal processing systems in DC through VHF range
- Custom designed differential amplifiers
- Temperature compensated amplifiers
- See RCA Application Note, ICAN-5296 "Application of the RCA CA3018 Integrated-Circuit Transistor Array" for suggested Applications.

FEATURES

- Matched monolithic general purpose transistors
- H_{FE} matched ± 10%
- V_{BE} matched ± 2 mV CA3018A (± 5mV CA3018)
- Operation from DC to 120 MHz
- Wide operating current range
- CA3018A performance characteristics controlled from 10μ A to 10mA
- Low noise figure - - 3.2 dB typical at 1KHz
- Full military temperature range capability (-55 to + 125°C)
- The CA3018 is available in a sealed-junction Beam Lead version (CA3018L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".
- Supplied in the hermetic 12-lead TO-5 style package.

Maximum Ratings, Absolute-Maximum Values, at TA=25°C

	CA3018	CA3018A	
Power Dissipation, P:			
Any one transistor	300	300	mW
Total package	450	450	mW
Derate at 5 mW/°C for $T_A > 85°C$			
Temperature Range:			
Operating	-55 to + 125	-55 to + 125	°C
Storage	-65 to + 150	-65 to + 150	°C
LEAD TEMPERATURE (During Soldering)			
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265		°C

The following ratings apply for each transistor in the device:

	CA3018	CA3018A	
Collector-to-Emitter Voltage, V_{CEO}	15	15	V
Collector-to-Base Voltage, V_{CBO}	20	30	V
Collector-to-Substrate Voltage, V_{CIO}*	20	40	V
Emitter-to-Base Voltage, V_{EBO}	5	5	V
Collector Current, I_C	50	50	mA

*The collector of each transistor of the CA3018 and CA3018A is isolated from the substrate by an integral diode. *The substrate (terminal 10) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

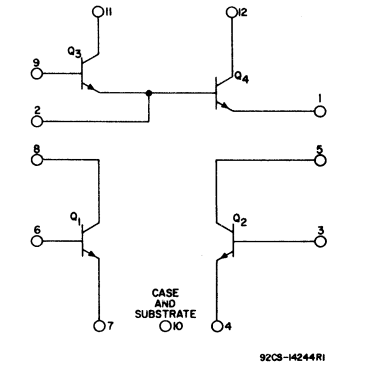


Fig. 1 - Schematic Diagram for CA3018 and CA3018A

STATIC CHARACTERISTICS

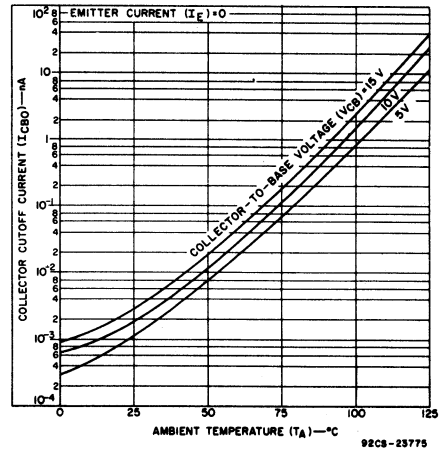


Fig.2 - Typical Collector-To-Base Cutoff Current vs Ambient Temperature for Each Transistor.

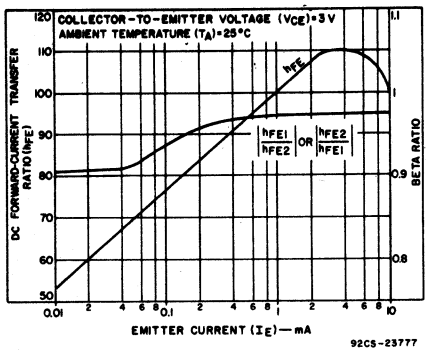


Fig. 3 - Typical Static Forward Current-Transfer Ratio and Beta Ratio for Transistors Q_1 and Q_2 vs Emitter Current.

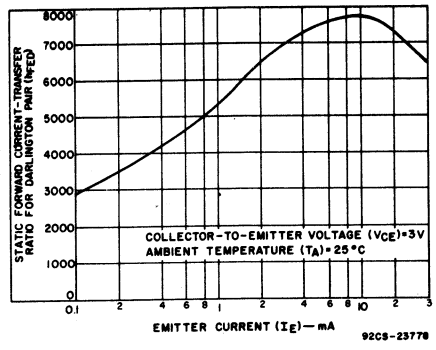


Fig. 4 - Typical Static Forward Current - Transfer Ratio for Darlington-connected Transisters Q_3 and Q_4 vs Emitter Current.

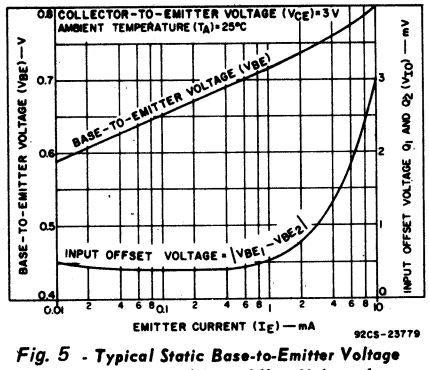


Fig. 5 - Typical Static Base-to-Emitter Voltage Characteristic and Input Offset Voltage for Q_1 and Q_2 vs Emitter Current.

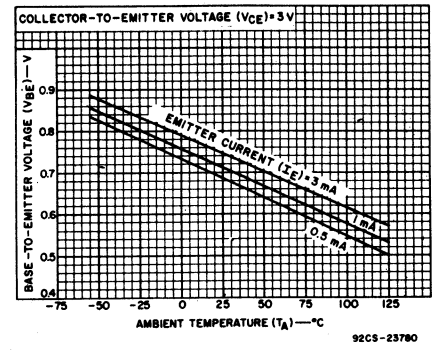


Fig. 6 - Typical Base-To-Emitter Voltage Characteristic for Each Transistor vs Ambient Temperature

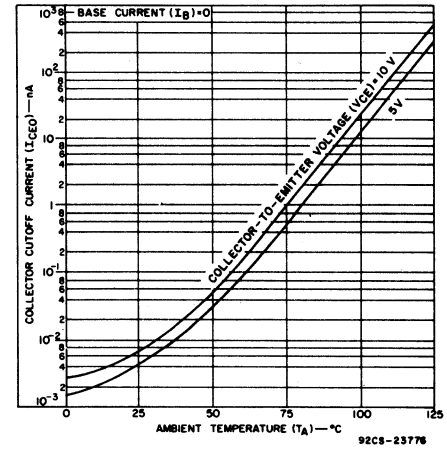


Fig. 7 - Typical Collector-To-Emmiter Cutoff Current vs Ambient Temperature for Each Transistor.

CA3018, CA3018A

Characteristics apply for each transistor in the CA3018 and CA3018A as specified.

ELECTRICAL CHARACTERISTICS at T_A = 25°C	SYMBOLS	SPECIAL TEST CONDITIONS	CA3018 LIMITS			CA3018A LIMITS			Units	CHARACTERISTICS CURVES
			Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
STATIC CHARACTERISTICS										
Collector-Cutoff Current	I_{CBO}	V_{CB}=10V, I_E=0	–	0.002	100	–	0.002	40	nA	2
Collector-Cutoff Current	I_{CEO}	V_{CE}=10V, I_B=0	–	See Curve	5	–	See Curve	0.5	μA	7
Collector-Cutoff Current Darlington Pair	I_{CEOD}	V_{CE}=10V, I_B=0	–	–	–	–	–	5	μA	–
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1mA, I_B=0	15	24	–	15	24	–	V	–
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=10μA, I_E=0	20	60	–	30	60	–	V	–
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E=10μA, I_C=0	5	7	–	5	7	–	V	–
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C=10μA, I_{CI}=0	20	60	–	40	60	–	V	–
Collector-to-Emitter Saturation Voltage	V_{CES}	I_B=1mA, I_C=10mA	–	0.23	–	–	0.23	0.5	V	–
Static Forward Current Transfer Ratio	h_{FE}	V_{CE}=3V, I_C=10mA I_C= 1mA I_C=10μA	– 30 –	100 100 54	– 200 –	50 60 30	100 100 54	– 200 –	– – –	3
Magnitude of Static-Beta Ratio (Isolated Transistors Q_1 and Q_2)		V_{CE}=3V, I_{C1}=I_{C2}=1mA	0.9	0.97	–	0.9	0.97	–	–	3
Static Forward Current Transfer Ratio Darlington Pair (Q_3 & Q_4)	h_{FED}	V_{CE}=3V I_C= 1mA I_C=100μA	1500 –	5400 –	– –	2000 1000	5400 2800	– –	–	4
Base-to-Emitter Voltage	V_{BE}	V_{CE}=3V I_E=1mA I_E=10mA	– –	0.715 0.800	– –	0.600 –	0.715 0.800	0.800 0.900	V	5
Input Offset Voltage	$\lvert V_{BE_1} - V_{BE_2} \rvert$	V_{CE}=3V, I_E=1mA	–	0.48	5	–	0.48	2	mV	5,8
Temperature Coefficient: Base-to-Emitter Voltage Q_1,Q_2	$\frac{\lvert \Delta V_{BE} \rvert}{\Delta T}$	V_{CE}=3V, I_E=1mA	–	1.9	–	–	1.9	–	mV/°C	6
Base (Q_3)-to-Emitter (Q_4) Voltage-Darlington Pair	V_{BED} (V_{9-1})	V_{CE}=3V I_E=10mA I_E= 1mA	– –	1.46 1.32	– –	– 1.10	1.46 1.32	1.60 1.50	V	9
Temperature Coefficient: Base-to-Emitter Voltage Darlington Pair-Q_3,Q_4	$\frac{\lvert \Delta V_{BED} \rvert}{\Delta T}$	V_{CE}=3V, I_E=1mA	–	4.4	–	–	4.4	–	mV/°C	10
Temperature Coefficient: Magnitude of Input-Offset Voltage	$\frac{\lvert V_{BE_1} - V_{BE_2} \rvert}{\Delta T}$	V_{CC}=+6V, V_{EE}=-6V, I_{C1}=I_{C2}=1mA	–	10	–	–	10	–	μV/°C	–

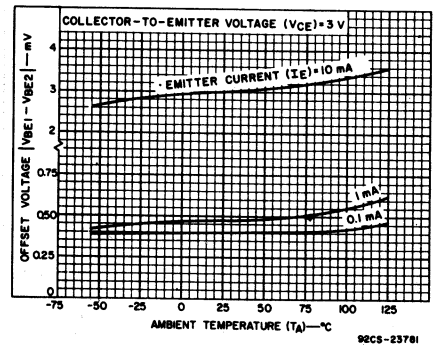


Fig.8 - Typical Offset Voltage Characteristic vs Ambient Temperature

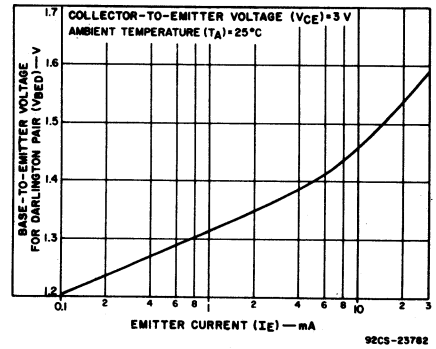


Fig.9 - Typical Static Input Voltage Characteristic for Darlington Pair (Q_3 and Q_4) vs Emitter Current

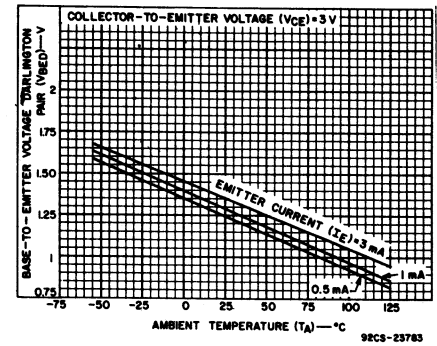


Fig.10 - Typical Static Input Voltage Characteristic for Darlington Pair (Q_3 and Q_4) vs Ambient Temperature.

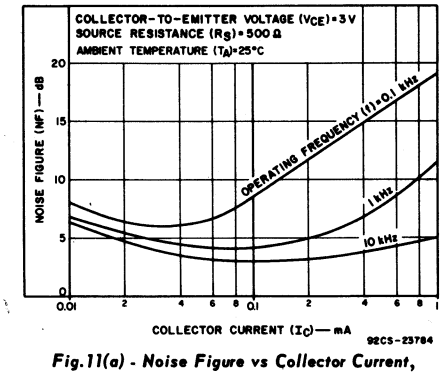


Fig.11(a) - Noise Figure vs Collector Current, R_S = 500 Ω.

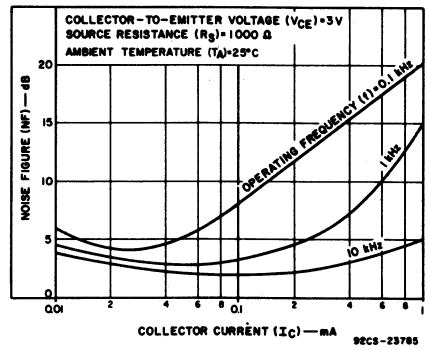


Fig.11(b) - Noise Figure vs Collector Current, R_S = 1 KΩ.

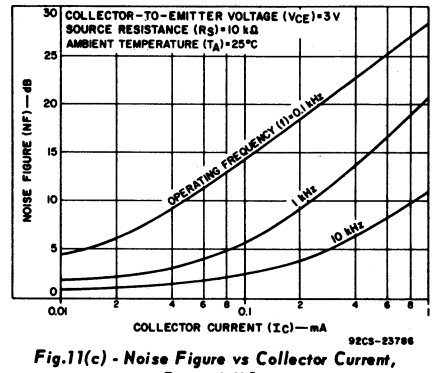


Fig.11(c) - Noise Figure vs Collector Current, R_S = 10 KΩ.

CA3018, CA3018A

ELECTRICAL CHARACTERISTICS, (CONT'D)

DYNAMIC CHARACTERISTICS			CA3018			CA3018A				
Low Frequency Noise Figure	NF	f=1 KHz, V_{CE}=3V, I_C=100μA Source resistance=1 KΩ	–	3.25	–	–	3.25	–	dB	11(b)
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:										
Forward Current-Transfer Ratio	h_{fe}	f=1kHz, V_{CE}=3V, I_C=1mA	–	110	–	–	110	–	–	12
Short-Circuit Input Impedance	h_{ie}		–	3.5	–	–	3.5	–	KΩ	12
Open-Circuit Output Impedance	h_{oe}		–	15.6	–	–	15.6	–	μmho	12
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		–	$1.8x10^{-4}$	–	–	$1.8x10^{-4}$	–	–	12
Admittance Characteristics:										
Forward Transfer Admittance	Y_{fe}	f=1MHz, V_{CE}=3V, I_C=1mA	–	31-j1.5	–	–	31-j1.5	–	mmho	13
Input Admittance	Y_{ie}		–	0.3+j0.04	–	–	0.3+j0.04	–	mmho	14
Output Admittance	Y_{oe}		–	0.001+j0.03	–	–	0.001+j0.03	–	mmho	15
Reverse Transfer Admittance	Y_{re}		See Curve			See Curve			mmho	16
Gain-Bandwidth Product	f_T	V_{CE}=3V, I_C=3mA	300	500	–	300	500	–	MHz	17
Emitter-to-Base Capacitance	C_{EB}	V_{EB}=3V, I_E=0	–	0.6	–	–	0.6	–	pF	–
Collector-to-Base Capacitance	C_{CB}	V_{CB}=3V, I_C=0	–	0.58	–	–	0.58	–	pF	–
Collector-to-Substrate Capacitance	C_{CI}	V_{CI}=3V, I_C=0	–	2.8	–	–	2.8	–	pF	–

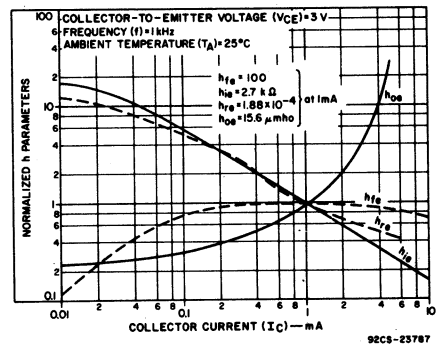


Fig.12 - Forward Current-Transfer Ratio (h_{fe}), Short-Circuit Input Impedance (h_{ie}), Open-Circuit Output Impedance (h_{oe}), and Open-Circuit Reverse Voltage-Transfer Ratio (h_{re}) vs Collector Current

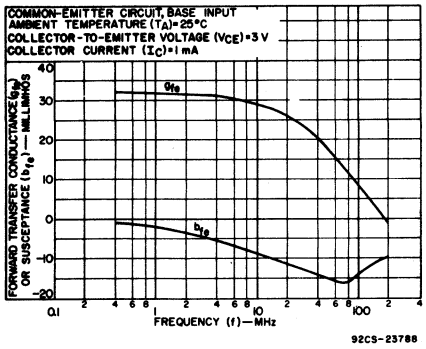


Fig.13 - Forward Transfer Admittance (Y_{fe})

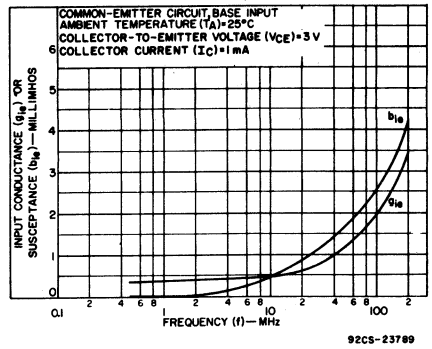


Fig.14 - Input Admittance (Y_{ie})

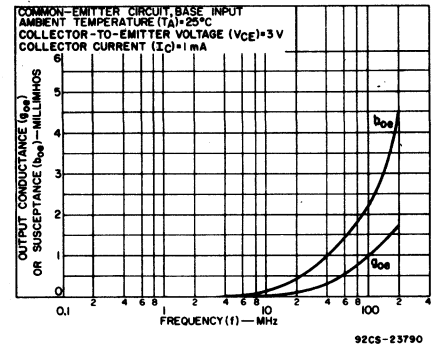


Fig.15 - Output Admittance (Y_{oe})

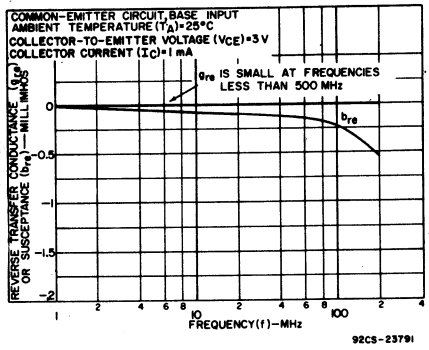


Fig.16 - Reverse Transfer Admittance (Y_{re})

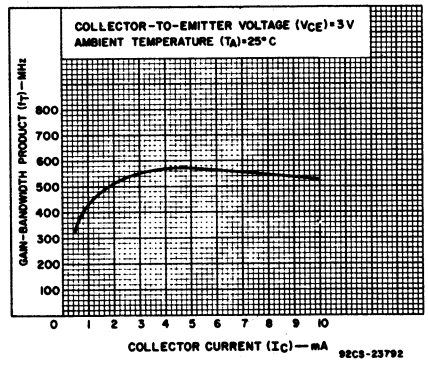


Fig.17 - Typical Gain-Bandwidth Product (f_T) vs Collector Current

CA3019

DIODE ARRAY

The CA3019 consists of one Diode "Quad" and two Isolated Diodes on a Common Substrate.

- **Designed for use in Telemetry, Data-Processing, Instrumentation, and Communication Equipment**
- **Built-in Temperature Stability for Operation from -55°C to +125°C**
- **10-Terminal TO-5 Package**
- **Hermetically Sealed**
- **Companion Application Note, ICAN-5299 "Application of the RCA CA3019 Integrated-Circuit Diode Array"**

HIGHLIGHTS

- **Excellent Diode Match**
- **Low Leakage Current**
- **Low Pedestal Voltage when Gating**

APPLICATIONS

- **Modulator**
- **Mixer**
- **Balanced Modulator**
- **Analog Switch**
- **Diode Gate for Chopper-Modulator Applications**

ABSOLUTE-MAXIMUM RATINGS:

DISSIPATION:
Any one diode unit . . . . . 20 max. mW
Total for device . . . . . 120 max. mW

TEMPERATURE RANGE:
Storage . . . . . -65 to +150 °C
Operating . . . . . -55 to +125 °C

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. . . . . +265°C

VOLTAGE: See Table

Absolute-Maximum Voltage Limits at $T_A = 25^0C$

TERMINAL	VOLTAGE LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	-3	+12	7	-6
2	-3	+12	7	-6
3	-3	+12	7	-6
4	-3	+12	7	-6
5	-3	+12	7	-6
6	-3	+12	7	-6
7	-18	0	1, 2, 3, 6, 8	0
8	-3	+12	7	-6
9	-3	+12	7	-6
10	NO CONNECTION			
CASE	INTERNALLY CONNECTED TO TERMINAL 7 **DO NOT GROUND**			

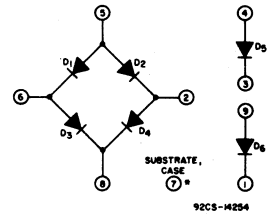


Fig.1 - Schematic Diagram for CA3019.

TYPICAL CHARACTERISTICS

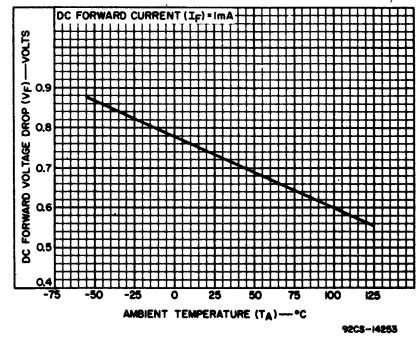


Fig.2 - DC Forward Voltage Drop (any Diode) vs Temperature for CA3019.

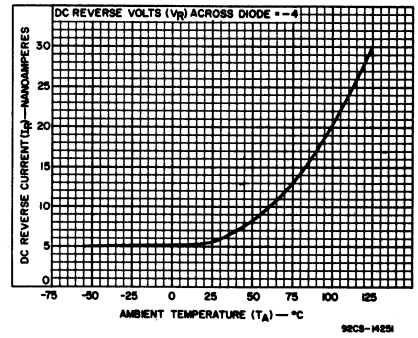


Fig.3 - Reverse (Leakage) Current (any Diode) vs Temperature for CA3019.

ELECTRICAL CHARACTERISTICS, at an Ambient Temperature, T_A, of 25°C
CHARACTERISTICS APPLY FOR EACH DIODE UNIT, UNLESS OTHERWISE SPECIFIED.

CHARACTERISTICS	SYMBOLS	TEST CIRCUITS	SPECIAL TEST CONDITIONS	LIMITS				TYPICAL CHARACTERISTICS CURVES
				TYPE CA3019				
		Fig.		Min.	Typ.	Max.	Units	Fig.
DC Forward Voltage Drop	V_F	-	DC Forward Current (I_F) = 1 mA	-	0.73	0.78	V	2
DC Reverse Breakdown Voltage	$V_{(BR)R}$	-	DC Reverse Current (I_R) = -10 μA	4	6	-	V	-
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	$V_{(BR)R}$	-	DC Reverse Current (I_R) = -10 μA	25	80	-	V	-
DC Reverse (Leakage) Current	I_R	-	DC Reverse Voltage (V_R) = -4 V	-	0.0055	10	μA	3
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	I_R	-	DC Reverse Voltage (V_R) = -4 V	-	0.010	10	μA	-
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	$\lvert V_{F1} - V_{F2} \rvert$	-	DC Forward Current (I_F) = 1 mA	-	1	5	mV	-
Single Diode Capacitance	C_D	-	Frequency (f) = 1 MHz DC Reverse Voltage (V_R) = -2 V	-	1.8	-	pF	4
Diode Quad-to-Substrate Capacitance	C_{DQ-I}		Frequency (f) = 1 MHz DC Reverse Voltage (V_R) between Terminal 2,5,6, or 8 of Diode Quad and Terminal 7 (Substrate) = -2 V					
			Terminal 2 or 6 to Terminal 7	-	4.4	-	pF	5
			Terminal 5 or 8 to Terminal 7	-	2.7	-	pF	6
Series Gate Switching Pedestal Voltage	V_S	7		-	10	-	mV	-

CA3019

TYPICAL CHARACTERISTICS (Cont'd)

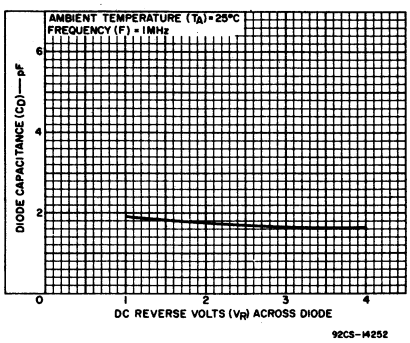


Fig.4 - Diode Capacitance (any Diode) vs Reverse Voltage for CA3019.

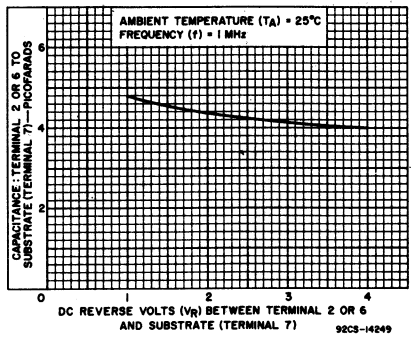


Fig.5 - Diode Quad-to-Substrate Capacitance vs Reverse Voltage for CA3019.

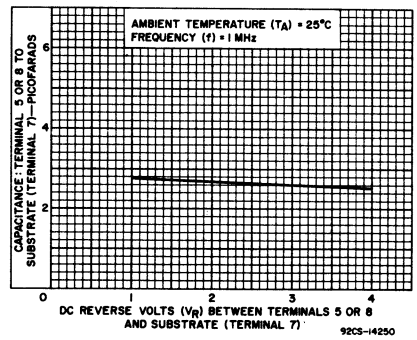


Fig.6 - Diode Quad-to-Substrate Capacitance vs Reverse Voltage for CA3019.

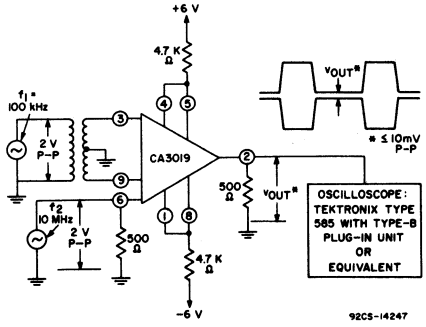


Fig.7 - Series Gate Switching Test Setup for CA3019.