

CA3026, CA3054

DUAL INDEPENDENT DIFFERENTIAL AMPLIFIERS

The CA3026 and CA3054 each consists of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six n-p-n transistors which comprise the amplifiers are general purpose devices which exhibit low 1/f noise and a value of f_T in excess of 300 MHz. These features make the CA3026 and CA3054 useful from dc to 120 MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

The monolithic construction of the CA3026 and CA3054 provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual channel applications where matched performance of the two channels is required.

For Low-Power Applications at Frequencies from DC to 120 MHz

APPLICATIONS

- Dual sense amplifiers
- Dual Schmitt triggers
- Multifunction combinations -- RF/Mixer, Oscillator; Converter/IF
- IF amplifiers (differential and/or cascode)
- Product detectors
- Doubly balanced modulators and demodulators
- Balanced quadrature detectors
- Cascade limiters
- Synchronous detectors
- Pairs of balanced mixers
- Synthesizer mixers
- Balanced (push-pull) cascode amplifiers

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES, AT $T_A = 25^\circ\text{C}$

Power Dissipation, P:	CA3026	CA3054	
Any one transistor	300	300	mW
Total package	600	750	mW
For $T_A > 55^\circ\text{C}$	Derate at 5		6.67 mW/ $^\circ\text{C}$
Temperature Range:			
Operating	-55 to +125		$^\circ\text{C}$
Storage	-65 to +150		$^\circ\text{C}$

Lead Temperature (During Soldering):

At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10 seconds max. $+265^\circ\text{C}$

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CISO}^*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

* The collector of each transistor of the CA3026 and CA3054 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide

for normal transistor action. The substrate should be maintained at signal (AC) ground by means of a suitable grounding capacitor, to avoid undesired coupling between transistors.

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 1[†] and horizontal terminal 3[†] is +15 to -5 volts.

† For CA3026; corresponding terminals for CA3054 are vertical terminal 2 and horizontal terminal 4.

CA3054 TERMINAL No. →	CA3026 TERMINAL No. →	13	14	1	2	3	4	6	7	8	9	11	12	5
13	10	0	-20	* +5	* -5	* +15	* -5	* *	* *	* *	* *	* *	* *	* *
14	11			* *	* *	* +20	* *	* *	* *	* *	* *	* *	* *	* +20
1	12			* +20	* 0	* +20	* *	* *	* *	* *	* *	* *	* *	* -20
2	1			* *	* *	* +15	* -5	* *	* *	* *	* *	* *	* *	* *
3	2			* *	* *	* +1	* -5	* *	* *	* *	* *	* *	* *	* *
4	3			* *	* *	* *	* *	* *	* *	* *	* *	* *	* *	* *
6	4							0	-20	* +5	* -5	* +15	* -5	* *
7	5									* *	* *	* *	* *	* +20
8	6									* +20	* 0	* *	* *	* +20
9	7									* *	* *	* +15	* -5	* *
11	8											* +1	* -5	* *
12	9													* *
5	9													Ref Substrate

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

Note 1: In the CA3026 terminal No.9 is connected to the emitter of Q_4 , the reference substrate, and the case; therefore, the case should not be grounded. Two terminal 9 columns (CA3026) appear in the voltage rating chart because it is a composite chart for both the CA3026 and the CA3054. Wherever an asterisk is shown in one column 9 and a rating is shown in the other column 9, the asterisk should be ignored.

Maximum Current Ratings

CA3054 TERMINAL No. #	CA3026 TERMINAL No.	I_{IN} mA	I_{OUT} mA
13	10	5	0.1
14	11	50	0.1
1	12	50	0.1
2	1	5	0.1
3	2	5	0.1
4	3	0.1	-50
6	4	5	0.1
7	5	50	0.1
8	6	50	0.1
9	7	5	0.1
11	8	5	0.1
12	9	0.1	50

• Terminal No.10 of CA3054 is not used

FEATURES

- Two differential amplifiers on a common substrate
- Independently accessible inputs and outputs
- Maximum input offset voltage -- ± 5 mV
- Full military temperature range capability -- -55°C to $+125^\circ\text{C}$
- Limited temperature range -- 0°C to 85°C for CA3054
- The CA3054 is available in a sealed-**junction Beam-Lead version (CA3054L)**. For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".
- CA3026—Hermetic 12-lead TO-5 package
- CA3054—14-lead dual-in-line plastic package

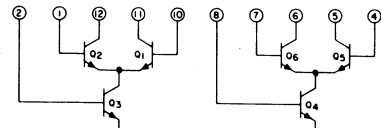


Fig. 1a - Schematic Diagram for CA3026.

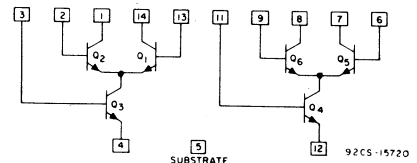
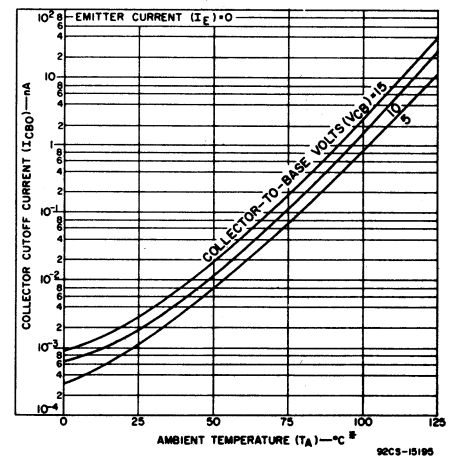


Fig. 1b - Schematic Diagram for CA3054.

CAUTION: Substrate MUST be maintained negative with respect to all collector terminals of this device. See Maximum Voltage Ratings chart.

TYPICAL STATIC CHARACTERISTICS



* For CA3054: use data from 0°C to 85°C only

Fig. 2 - Collector-to-base cutoff current vs ambient temperature for each transistor.

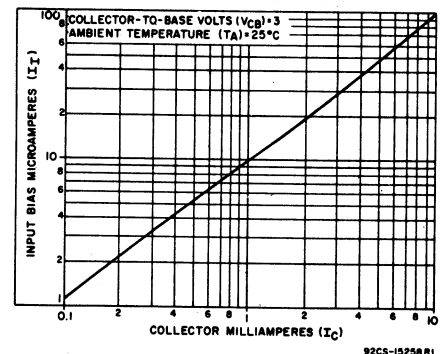


Fig. 3 - Input bias current characteristic vs collector current for each transistor.

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ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIRCUIT	CA3026 CA3054 LIMITS				TYPICAL CHARACTERISTICS CURVES	
				FIG.	MIN.	TYP.	MAX.		UNITS
STATIC CHARACTERISTICS									
For Each Differential Amplifier									
Input Offset Voltage	V_{IO}	$V_{CB} = 3\text{ V}$ $I_{E(Q3)} = I_{E(Q4)} = 2\text{ mA}$	-	-	0.45	5	mV	6	
Input Offset Current	I_{IO}		-	-	0.3	2	μA	7	
Input Bias Current	I_I		-	-	10	24	μA	3	
Quiescent Operating Current Ratio	$\frac{I_{C(Q1)} \text{ or } I_{C(Q2)}}{I_{C(Q3)} \text{ or } I_{C(Q4)}}$		-	-	0.98 to 1.02	-	-	-	3
Temperature Coefficient Magnitude of Input-Offset Voltage	$\frac{ \Delta V_{IO} }{\Delta T}$		-	-	1.1	-	$\mu\text{V}/^\circ\text{C}$	5	
For Each Transistor									
DC Forward Base-to-Emitter Voltage	V_{BE}	$V_{CB} = 3\text{ V}$	$I_C = 50\ \mu\text{A}$	-	-	0.630	0.700	V	6
			1 mA	-	-	0.715	0.800		
			3 mA	-	-	0.750	0.850		
			10 mA	-	-	0.800	0.900		
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	$V_{CB} = 3\text{ V}, I_C = 1\text{ mA}$	-	-	-1.9	-	$\mu\text{V}/^\circ\text{C}$	4	
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 10\text{ V}, I_E = 0$	-	-	0.002	100	nA	2	
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1\text{ mA}, I_B = 0$	-	15	24	-	V	-	
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\ \mu\text{A}, I_E = 0$	-	20	60	-	V	-	
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CSO}$	$I_C = 10\ \mu\text{A}, I_{C1} = 0$	-	20	60	-	V	-	
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\ \mu\text{A}, I_C = 0$	-	5	7	-	V	-	
DYNAMIC CHARACTERISTICS									
Common-Mode Rejection Ratio For Each Amplifier	CMR	$V_{CC} = 12\text{ V}$ $V_{EE} = -6\text{ V}$ $V_X = -3.3\text{ V}$ $f = 1\text{ kHz}$	8a	-	100	-	dB	8b	
AGC Range, One Stage	AGC		9a	-	75	-	dB	9b	
Voltage Gain, Single Stage Double-Ended Output	A		9a	-	32	-	dB	9b	
AGC Range, Two Stage	AGC		10a	-	105	-	dB	10b	
Voltage Gain, Two Stage Double-Ended Output	A		10a	-	60	-	dB	10b	
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics: (For Single Transistor)									
Forward Current-Transfer Ratio	h_{fe}	$f = 1\text{ kHz}, V_{CE} = 3\text{ V}, I_C = 1\text{ mA}$	-	-	110	-	-	11	
Short-Circuit Input Impedance	h_{ie}		-	-	3.5	-	k Ω	11	
Open-Circuit Output Impedance	h_{oe}		-	-	15.6	-	μmho	11	
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		-	-	1.8×10^{-4}	-	-	11	

DYNAMIC CHARACTERISTICS CONT'D

1/f Noise Figure (For Single Transistor)	NF	$f = 1\text{ kHz}, V_{CE} = 3\text{ V}$	-	-	3.25	-	dB	-
Gain-Bandwidth Product (For Single Transistor)	f_T	$V_{CE} = 3\text{ V}, I_C = 3\text{ mA}$	-	-	550	-	MHz	12
Admittance Characteristics; Differential Circuit Configuration: (For Each Amplifier)								
Forward Transfer Admittance	y_{21}	$V_{CB} = 3\text{ V}$ Each Collector $I_C \approx 1.25\text{ mA}$ $f = 1\text{ MHz}$	-	-	$-20 + j0$	-	mmho	13a
Input Admittance	y_{11}		-	-	$0.22 + j0.1$	-	mmho	13b
Output Admittance	y_{22}		-	-	$0.01 + j0$	-	mmho	13c
Reverse Transfer Admittance	y_{12}		-	-	$-0.003 + j0$	-	mmho	13d
Admittance Characteristics; Cascode Circuit Configuration: (For Each Amplifier)								
Forward Transfer Admittance	y_{21}	$V_{CB} = 3\text{ V}$ Total Stage $I_C \approx 2.5\text{ mA}$ $f = 1\text{ MHz}$	-	-	$68 - j0$	-	mmho	14a
Input Admittance	y_{11}		-	-	$0.55 + j0$	-	mmho	14b
Output Admittance	y_{22}		-	-	$0 + j0.02$	-	mmho	14c
Reverse Transfer Admittance	y_{12}		-	-	$0.004 - j0.005$	-	μmho	14d
Noise Figure	NF	$f = 100\text{ MHz}$	-	-	8	-	dB	-

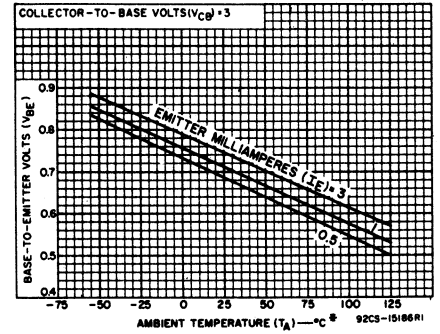


Fig. 4 - Base-to-emitter voltage characteristic for each transistor vs ambient temperature.

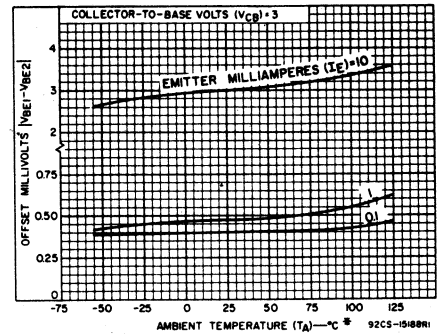


Fig. 5 - Offset voltage characteristic vs ambient temperature for differential pairs.

* For CA3054: use data from 0°C to 85°C only

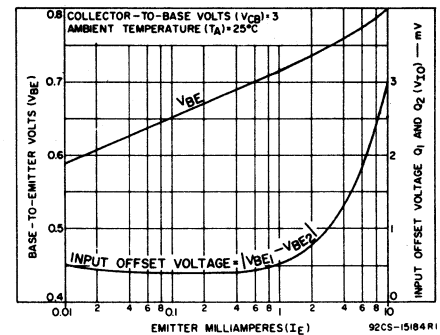


Fig. 6 - Static base-to-emitter voltage characteristic and input offset voltage for differential pairs vs emitter current.

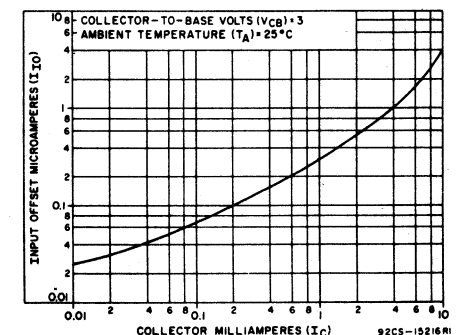


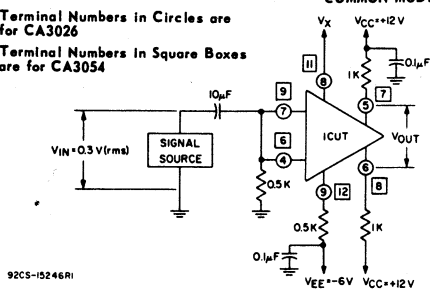
Fig. 7 - Input offset current for matched differential pairs vs collector current.

CA3026, CA3054

TYPICAL DYNAMIC CHARACTERISTICS

COMMON MODE REJECTION RATIO

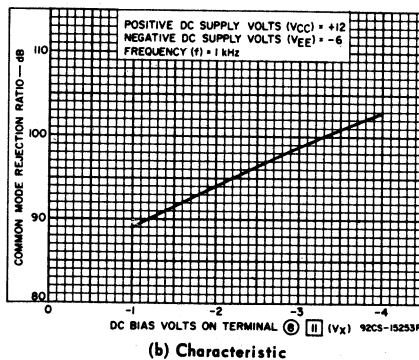
Terminal Numbers in Circles are for CA3026
Terminal Numbers in Square Boxes are for CA3054



92CS-15246R1

(a) Test setup

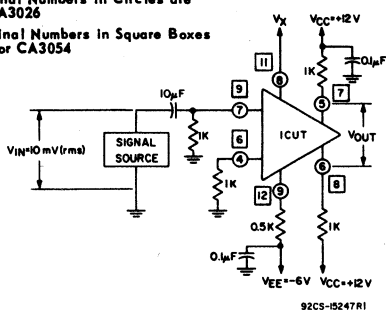
Fig.8



(b) Characteristic

SINGLE-STAGE VOLTAGE GAIN

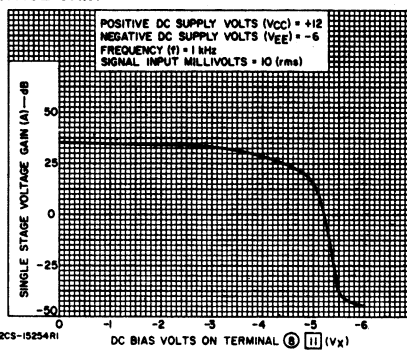
Terminal Numbers in Circles are for CA3026
Terminal Numbers in Square Boxes are for CA3054



92CS-15247R1

(a) Test setup

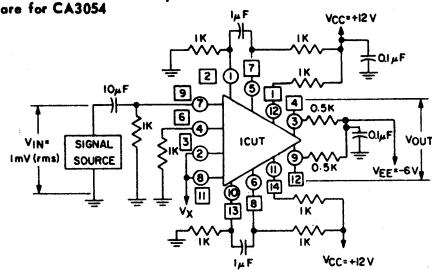
Fig.9



(b) Characteristic

TWO-STAGE VOLTAGE GAIN

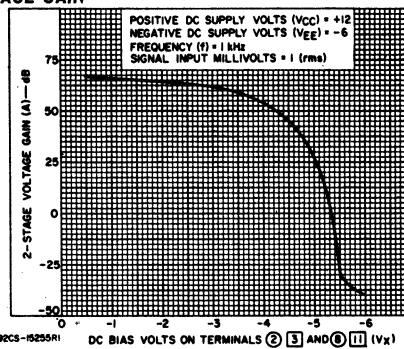
Terminal Numbers in Circles are for CA3026
Terminal Numbers in Square Boxes are for CA3054



92CS-15248R1

(a) Test setup

Fig.10



(b) Characteristic

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

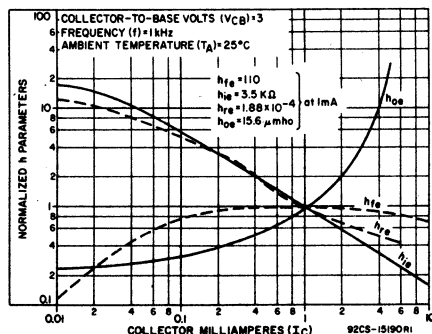


Fig.11 - Forward current-transfer ratio (h_{fe}), short-circuit input impedance (h_{ie}), open-circuit output impedance (h_{oe}), and open-circuit reverse voltage-transfer ratio (h_{re}) vs collector current for each transistor.

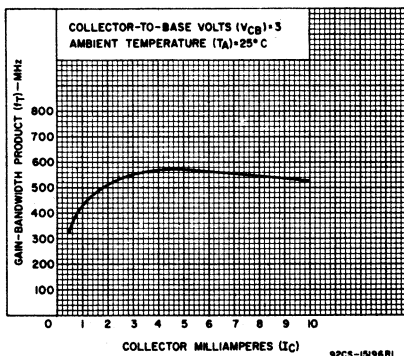


Fig.12 - Gain-bandwidth product (f_T) vs collector current.

CA3026, CA3054

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH DIFFERENTIAL AMPLIFIER

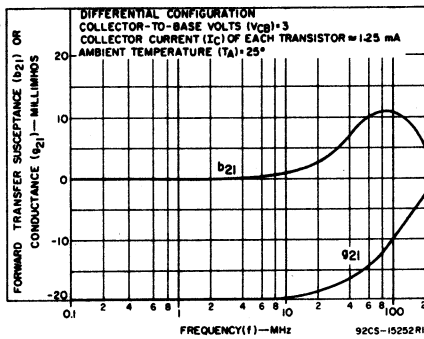


Fig.13(a) - Forward transfer admittance (Y_{21}) vs frequency.

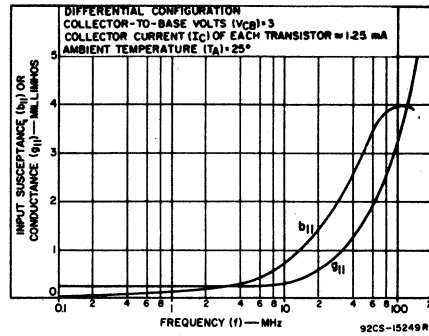


Fig.13(b) - Input admittance (Y_{11}).

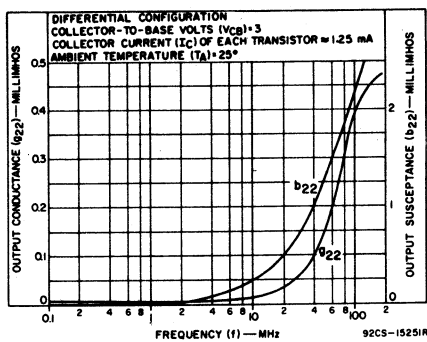


Fig.13(c) - Output admittance (Y_{22}) vs frequency.

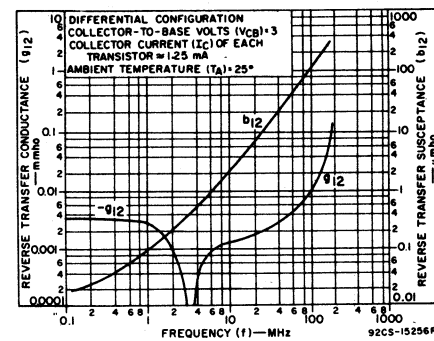


Fig.13(d) - Reverse transfer admittance (Y_{12}) vs frequency.

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH CASCODE AMPLIFIER

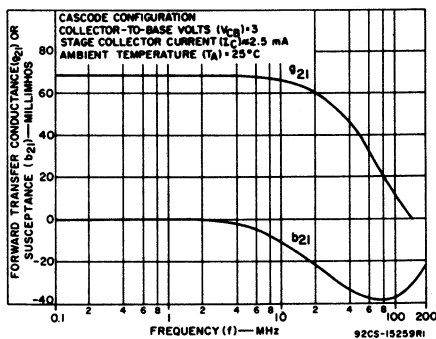


Fig.14(a) - Forward transfer admittance (Y_{21}) vs frequency.

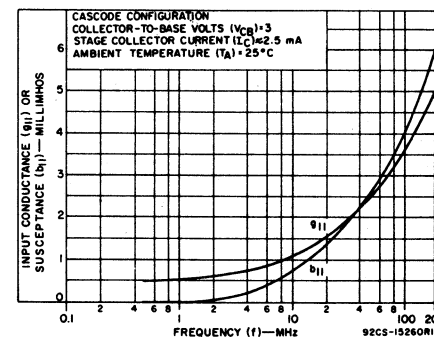


Fig.14(b) - Input admittance (Y_{11}) vs frequency.

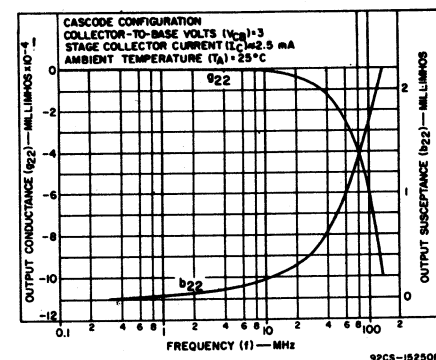


Fig.14(c) - Output admittance (Y_{22}) vs frequency.

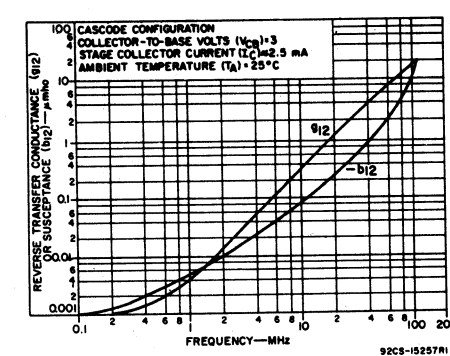


Fig.14(d) - Reverse transfer admittance (Y_{12}) vs frequency.

CA3028, CA3028A, CA3053

DIFFERENTIAL/CASCODE AMPLIFIERS

For Communications and Industrial Equipment at Frequencies from DC to 120 MHz

The CA3028A and CA3028B are differential/cascode amplifiers designed for use in communications and industrial equipment operating at frequencies from dc to 120 MHz.

The CA3028B is like the CA3028A but is capable of premium performance particularly in critical dc and differential amplifier applications requiring tight controls for input offset voltage, input offset current, and input bias current.

The CA3053 is similar to the CA3028A and CA3028B but is recommended for IF amplifier applications.

The CA3028A, CA3028B, and CA3053 are supplied in a hermetic 8-lead TO-5-style package. The "F" versions are supplied in a frit-seal package and the "S" versions in formed-lead (DIL-CAN) packages.

FEATURES

- Controlled for Input Offset Voltage, Input Offset Current, and Input Bias Current* (CA3028B)
- Balanced Differential Amplifier Configuration with Controlled Constant-Current Source to Provide
- The CA3028A is available in a sealed-junction Beam-Lead version (CA3028AL). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".

Unexcelled Versatility

- Single- and Dual-Ended Operation
- Operation from DC to 120 MHz
- Balanced-AGC Capability
- Wide Operating-Current Range

APPLICATIONS

- RF and IF Amplifiers (Differential or Cascode)
- DC, Audio, and Sense Amplifiers
- Converter in the Commercial FM Band
- Oscillator • Mixer • Limiter
- Companion Application Note, ICAN 5337 "Application of the RCA CA3028 Integrated Circuit Amplifier in the HF and VHF Ranges." This note covers characteristics of different operating modes, noise performance, mixer, limiter, and amplifier design considerations.

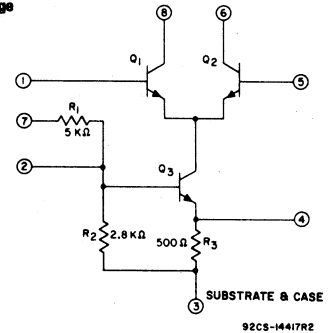


Fig. 1 - Schematic diagram for CA3028A, CA3028B and CA3053.

ABSOLUTE MAXIMUM RATINGS AT T_A = 25°C

DISSIPATION:

At T_A up to 55°C
(CA3028AF, CA3028BF, CA3053F) 750 mW

At T_A > 55°C
(CA3028AF, CA3028BF, CA3053F) Derate linearly 6.67 mW/°C

At T_A up to 85°C
(CA3028A, CA3028B, CA3053) 450 mW

At T_A > 85°C
(CA3028A, CA3028B, CA3053) Derate linearly 5 mW/°C

AMBIENT-TEMPERATURE RANGE:

Operating -55°C to +125°C
Storage -65°C to +150°C

LEAD TEMPERATURE (During Soldering):

At distance 1/16 ± 1/32" (1.59 ± 0.79 mm)
from case for 10 seconds max. +265°C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

TERMINAL No.	1	2	3	4	5	6	7	8
1		0 to -15 ^Δ	0 to -15 ^Δ	0 to -15 ^Δ	+5 to -5	*	*	+20 [⊕] to 0
2			+5 to -11	+5 to -1	+15 [⊕] to 0	*	+15 [⊕] to 0	*
3 [‡]				+10 to 0	+15 [⊕] to 0	+30 [⊕] to 0	+15 [⊕] to 0	+30 [⊕] to 0
4					+15 [⊕] to 0	*	*	*
5						+20 [⊕] to 0	*	*
6							*	*
7							*	*
8								

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of the horizontal terminal 4 with respect to terminal 2 is -1 to +5 volts.

‡ Terminal #3 is connected to the substrate and case.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe, if the specified voltage limits between all other terminals are not exceeded.

- ⊕ Limit is -12V for CA3053
- ⊕ Limit is +15V for CA3053
- ⊕ Limit is +12V for CA3053
- ⊕ Limit is +24V for CA3028A and +18V for CA3053

MAXIMUM CURRENT RATINGS

TERMINAL No.	I _{IN} mA	I _{OUT} mA
1	0.6	0.1
2	4	0.1
3	0.1	23
4	20	0.1
5	0.6	0.1
6	20	0.1
7	4	0.1
8	20	0.1

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CIRCUIT Fig.	SPECIAL TEST CONDITIONS		LIMITS TYPE CA3028A			LIMITS TYPE CA3028B			LIMITS TYPE CA3053			UNITS	TYPICAL CHARACTERISTICS CURVES Fig.
			+V _{CC}	-V _{EE}	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
STATIC CHARACTERISTICS															
Input Offset Voltage	V _{IO}	2	6V 12V	6V 12V	-	-	-	0.98 0.89	5 5	-	-	-	mV	4	
Input Offset Current	I _{IO}	3a	6V 12V	6V 12V	-	-	-	0.56 1.06	5 6	-	-	-	μA	4	
Input Bias Current	I _I	3a	6V 12V	6V 12V	-	16.6 36	70 106	-	16.6 36	40 80	-	-	-	μA	5a
		3b	9V 12V	-	-	-	-	-	-	-	29 36	85 125	-	μA	5b
Quiescent Operating Current	I ₆ or I ₈	3a	6V 12V	6V 12V	0.8 2	1.25 3.3	2 5	1 2.5	1.25 3.3	1.5 4	-	-	-	mA	6a 7
		3b	9V 12V	-	-	-	-	-	-	-	1.2 2.0	2.2 3.3	3.5 5.0	-	mA
AGC Bias Current (Into Constant-Current Source Terminal No.7)	I ₇	8a	12V 12V	V _{AGC} = +9 V _{AGC} = +12	-	1.28 1.65	-	-	1.28 1.65	-	-	-	-	mA	8b
Input Current (Terminal No.7)	I ₇	-	9V 12V	-	-	-	-	-	-	-	-	1.15 1.55	-	-	
		-	6V 12V	6V 12V	0.5 1	0.85 1.65	1 2.1	0.5 1	0.85 1.65	1 2.1	-	-	-	mA	-
Device Dissipation	P _T	3a	6V 12V	6V 12V	24 120	36 175	54 260	24 120	36 175	42 220	-	-	-	mW	9
		3b	9V 12V	-	-	-	-	-	-	-	-	50 100	80 150	-	mW

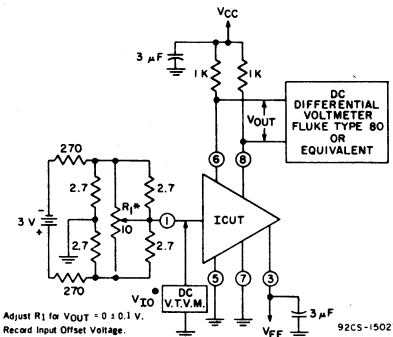


Fig. 2 - Input offset voltage test circuit for CA3028B.

CA3028, CA3028A, CA3053

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$ (cont'd)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	SPECIAL TEST CONDITIONS	LIMITS TYPE CA3028A			LIMITS TYPE CA3028B			UNITS	TYPICAL CHARACTERISTICS CURVE	
				Min.	Typ.	Max.	Min.	Typ.	Max.			
DYNAMIC CHARACTERISTICS												
Power Gain	G _P	10a	f = 100 MHz	Cascode	16	20	-	16	20	-	dB	10b
		11a,d	V _{CC} = +9V	Diff.-Amp.	14	17	-	14	17	-		
Noise Figure	NF	10a	f = 10.7 MHz	Cascode	35	39	-	35	39	-	dB	10c
		11a	V _{CC} = +9V	Diff.-Amp.	28	32	-	28	32	-		
Input Admittance	Y ₁₁	10a	f = 100 MHz	Cascode	-	7.2	9	-	7.2	9	mmho	12
		11a,d	V _{CC} = +9V	Diff.-Amp.	-	6.7	9	-	6.7	9		
Reverse Transfer Admittance	Y ₁₂	-	-	Cascode	-	-	-	-	0.6 + j 1.6	-	mmho	13
		-	-	Diff.-Amp.	-	-	-	-	0.5 + j 0.5	-		
Forward Transfer Admittance	Y ₂₁	-	f = 10.7 MHz	Cascode	-	-	-	-	0.0003 - j0	-	mmho	14
		-	V _{CC} = +9V	Diff.-Amp.	-	-	-	-	0.01 - j0.0002	-		
Output Admittance	Y ₂₂	-	-	Cascode	-	-	-	-	99 - j18	-	mmho	16
		-	-	Diff.-Amp.	-	-	-	-	-37 + j0.5	-		
Power Output (Untuned)	P _O	20a	f = 10.7 MHz	Diff.-Amp.	-	5.7	-	-	5.7	-	μW	20b
AGC Range (Max. Power Gain to Full Cutoff)	AGC	21a	V _{CC} = +9V	Diff.-Amp.	-	62	-	-	62	-	dB	21b
Voltage Gain	A	22a	f = 10.7 MHz	Cascode	-	40	-	-	40	-	dB	22b
		22c	V _{CC} = +0V R _L = 1 kΩ	Diff.-Amp.	-	30	-	-	30	-		
Max. Peak-to-Peak Output Voltage at f = 1 kHz	V _{O(P-P)}	23	V _{CC} = +6V, R _L = 2 kΩ	V _{EE} = -6V	-	-	-	-	35	38	42	V _{P-P}
		23	V _{CC} = +12V, R _L = 1.6 kΩ	V _{EE} = -12V	-	-	-	-	40	42.5	45	
Bandwidth at -3 dB point	BW	23	V _{CC} = +6V, R _L = 2 kΩ	V _{EE} = -6V	-	-	-	-	7.3	-	MHz	-
		23	V _{CC} = +12V, R _L = 1.6 kΩ	V _{EE} = -12V	-	-	-	-	8	-		
Common-Mode Input-Voltage Range	V _{CMR}	24	V _{CC} = +6V, V _{CC} = +12V	V _{EE} = -6V, V _{EE} = -12V	-	-	-2.5 -5	(-3.2 - 4.5) (-7 - 9)	4 7	-	V	-
Common-Mode Rejection Ratio	CMR	24	V _{CC} = +6V, V _{CC} = +12V	V _{EE} = -6V, V _{EE} = -12V	-	-	60 60	110 90	-	-	dB	-
Input Impedance at f = 1 kHz	Z _{IN}	-	V _{CC} = +6V, V _{CC} = +12V	V _{EE} = -6V, V _{EE} = -12V	-	-	-	5.5 3	-	-	kΩ	-
Peak-to-Peak Output Current	I _{P-P}	-	V _{CC} = +9V	f = 10.7 MHz e _{in} = 400 mV Diff.-Amp.	2	4	7	2.5	4	6	mA	-
		-	V _{CC} = +12V	-	3.5	6	10	4.5	6	8		

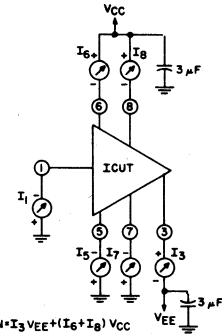


Fig. 3a - Input offset current, input bias current, device dissipation, and quiescent operating current test circuit for CA3028A and CA3028B.

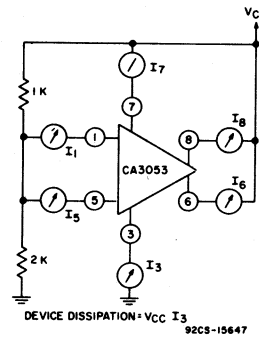


Fig. 3b - Input bias current, device dissipation, and quiescent operating current test circuit for CA3053.

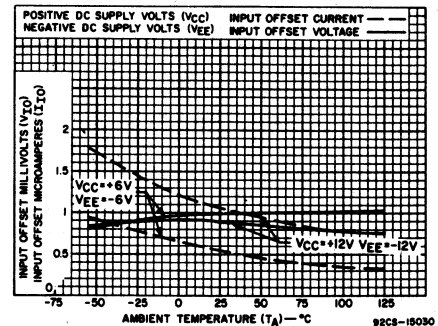


Fig. 4 - Input offset voltage and input offset current for CA3028B.

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$ (cont'd)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	SPECIAL TEST CONDITIONS	LIMITS TYPE CA3053			UNITS	TYPICAL CHARACTERISTICS CURVE
				Min.	Typ.	Max.		
DYNAMIC CHARACTERISTICS								
Power Gain	G _P	10a	f = 10.7 MHz	Cascode	35	39	-	dB
Input Admittance	Y ₁₁	11a	V _{CC} = +9V	Diff.-Amp.	28	32	-	mmho
		-	-	Cascode	-	0.6 + j 1.6	-	12
Reverse Transfer Admittance	Y ₁₂	-	-	Diff.-Amp.	-	0.5 + j 0.5	-	mmho
		-	-	Cascode	-	0.0003 - j0	-	14
Forward Transfer Admittance	Y ₂₁	-	f = 10.7 MHz	Diff.-Amp.	-	0.01 - j0.0002	-	mmho
		-	V _{CC} = +9V	Cascode	-	99 - j18	-	16
Output Admittance	Y ₂₂	-	-	Diff.-Amp.	-	-37 + j0.5	-	mmho
		-	-	Cascode	-	0. + j0.08	-	18
Voltage Gain	A	22a	f = 10.7 MHz	Cascode	-	40	-	dB
		22c	V _{CC} = +0V R _L = 1 kΩ	Diff.-Amp.	-	30	-	22d
Peak-to-Peak Output Current	P-P	-	V _{CC} = +9V V _{CC} = +12V	f = 10.7 MHz e _{in} = 400 mV Diff.-Amp.	2 3.5	4 6	7 10	mA

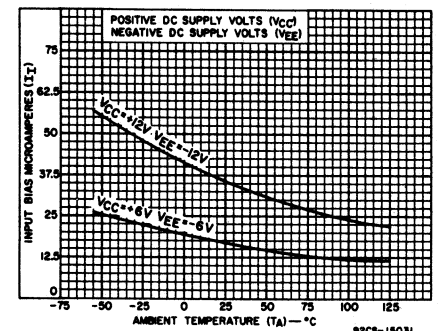


Fig. 5a - Input bias current vs. ambient temperature for CA3028A and CA3028B.

CA3028, CA3028A, CA3053

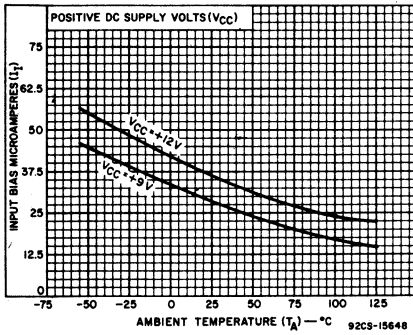


Fig.5b - Input bias current vs. ambient temperature for CA3053.

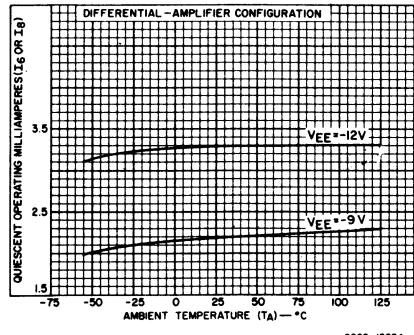


Fig.6a - Quiescent operating current vs. ambient temperature for CA3028A and CA3028B.

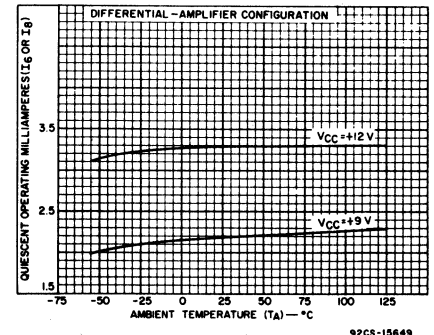


Fig.6b - Quiescent operating current vs. ambient temperature for CA3053.

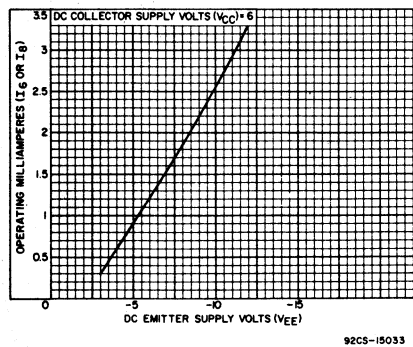


Fig.7 - Operating current vs. VEE voltage for CA3028A and CA3028B.

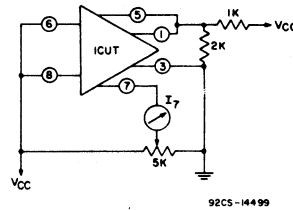


Fig.8a - AGC bias current test circuit (differential-amplifier configuration) for CA3028A and CA3028B.

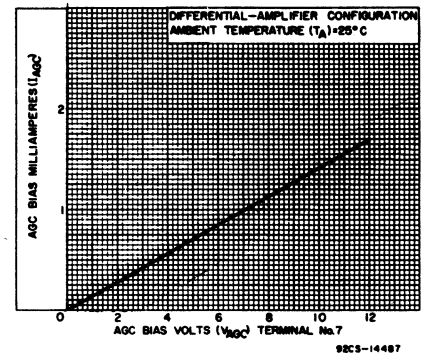


Fig.8b - AGC bias current vs. bias volts (terminal No.7) for CA3028A and CA3028B.

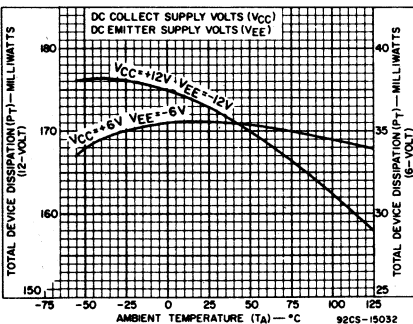


Fig.9 - Device dissipation vs. temperature for CA3028A and CA3028B.

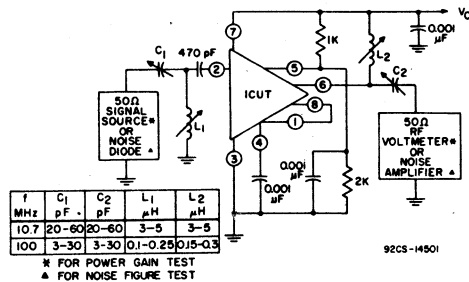


Fig.10a - Power gain and noise figure test circuit (cascode configuration) for CA3028A, CA3028B and CA3053*.

* 10.7 MHz Power Gain Test Only.

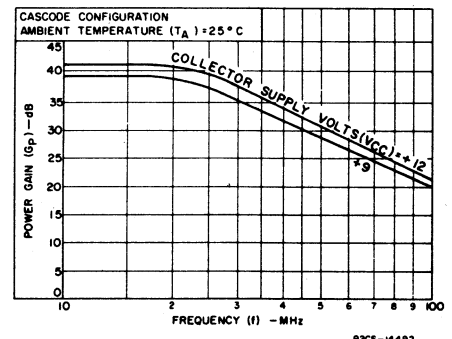


Fig.10b - Power gain vs. frequency (cascode configuration) for CA3028A and CA3028B.

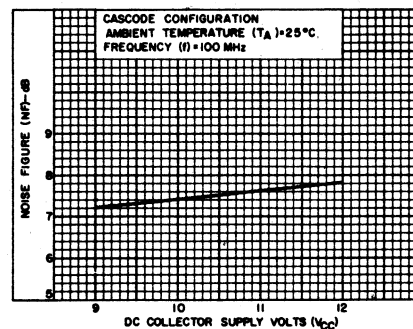


Fig.10c - 100 MHz noise figure vs. collector supply volts (cascode configuration) for CA3028A and CA3028B.

TYPICAL NOISE FIGURE AND POWER GAIN TEST CIRCUITS AND CHARACTERISTICS

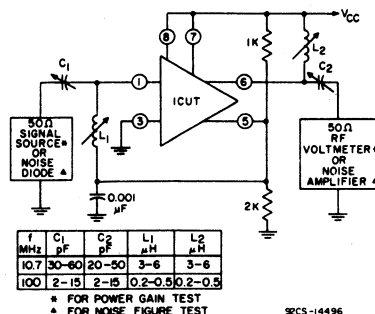


Fig.11a - Power gain and noise figure test circuit (differential-amplifier configuration and terminal No.7 connected to VCC) for CA3028A, CA3028B and CA3053*.

* 10.7 MHz Power Gain Test Only.

CA3028, CA3028A, CA3053

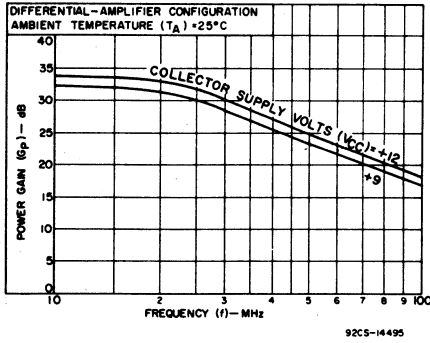


Fig. 11b - Power gain vs. frequency (differential-amplifier configuration) for CA3028A and CA3028B.

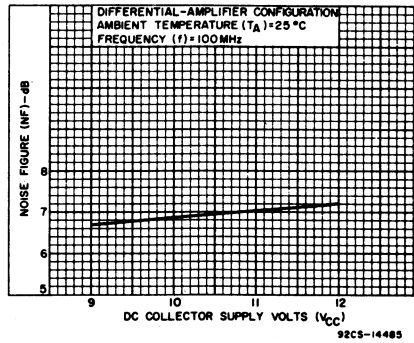


Fig. 11c - 100 MHz noise figure vs. collector supply voltage (differential-amplifier configuration) for CA3028A and CA3028B.

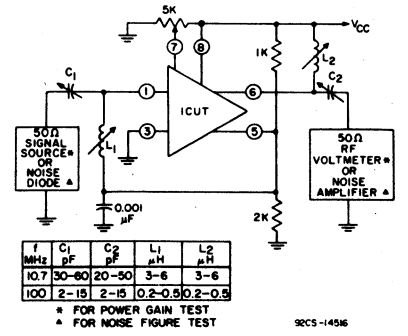


Fig. 11d - Power gain and noise figure test circuit (differential-amplifier configuration) for CA3028A and CA3028B.

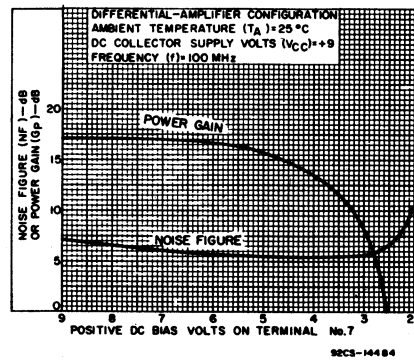


Fig. 11e - 100 MHz noise figure and power gain vs. base-to-emitter bias (terminal No. 7) for CA3028A and CA3028B.

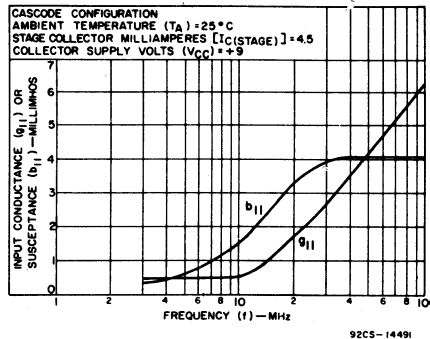


Fig. 12 - Input admittance (Y11) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

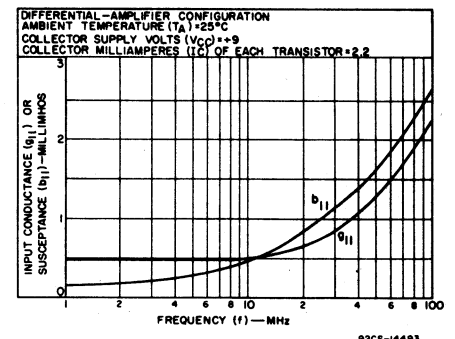


Fig. 13 - Input admittance (Y11) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

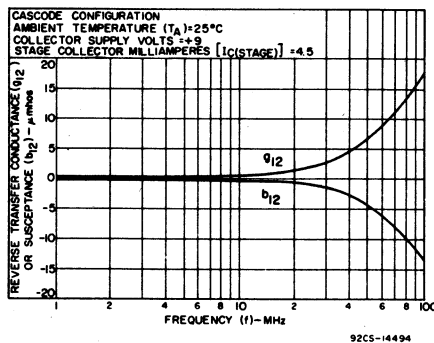


Fig. 14 - Reverse transadmittance (Y12) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

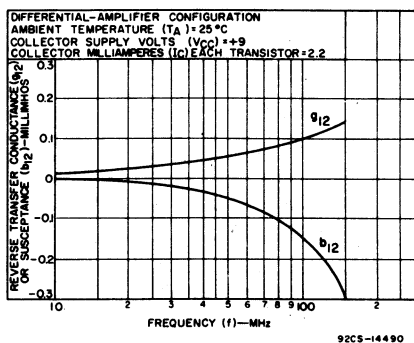


Fig. 15 - Reverse transadmittance (Y12) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

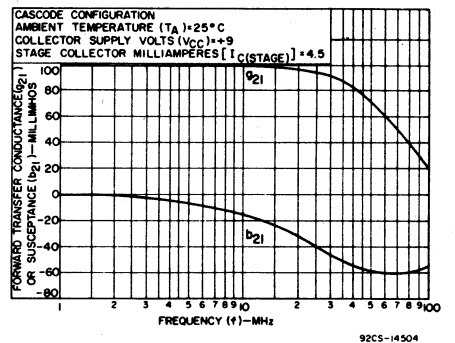


Fig. 16 - Forward transadmittance (Y21) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

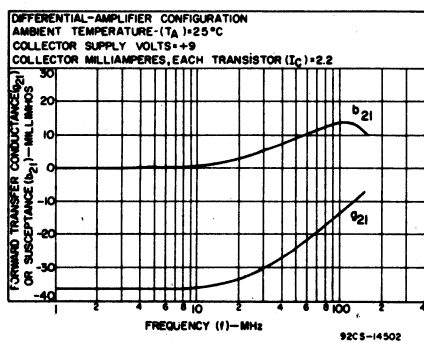


Fig. 17 - Forward transadmittance (Y21) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

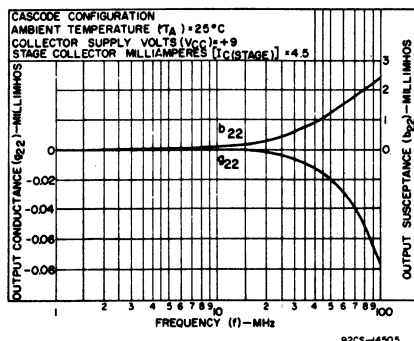


Fig. 18 - Output admittance (Y22) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

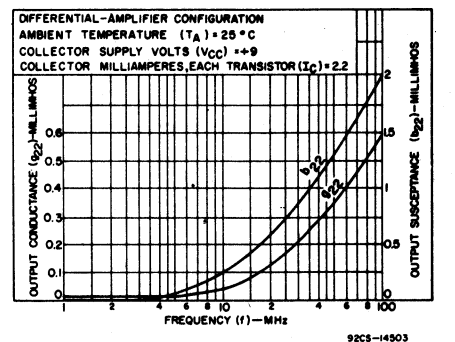


Fig. 19 - Output admittance (Y22) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

CA3028, CA3028A, CA3053

TYPICAL TEST CIRCUITS AND CHARACTERISTICS

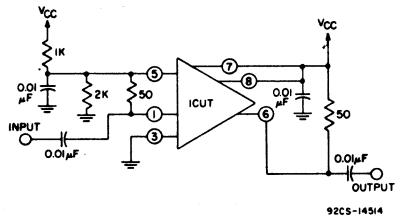


Fig. 20a - Output power test circuit for CA3028A and CA3028B.

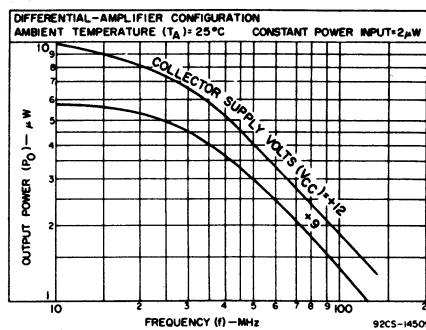


Fig. 20b - Output power vs. frequency - 50 ohm input and 50 ohm output (differential-amplifier configuration) for CA3028A and CA3028B.

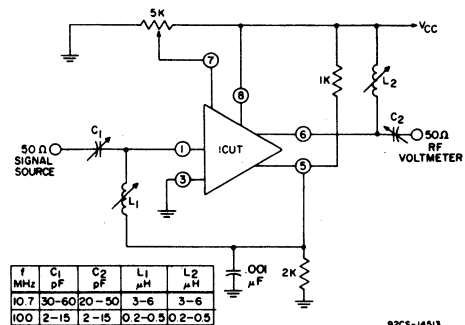


Fig. 21a - AGC range test circuit (differential amplifier) for CA3028A and CA3028B.

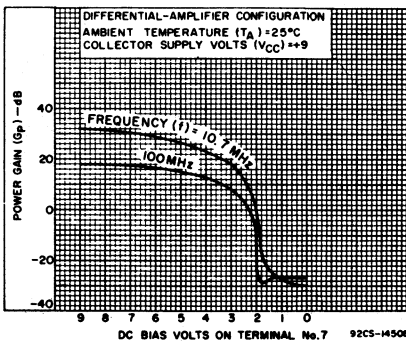


Fig. 21b - AGC characteristics for CA3028A and CA3028B.

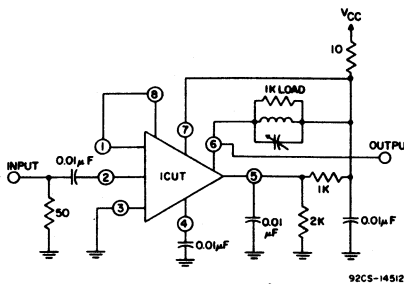


Fig. 22a - Transfer characteristic (voltage gain) test circuit (10.7 MHz) cascode configuration for CA3028A, CA3028B and CA3053.

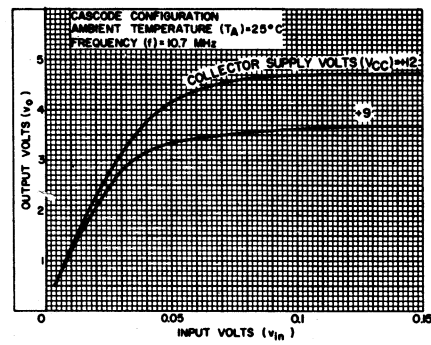


Fig. 22b - Transfer characteristics (cascode configuration) for CA3028A, CA3028B and CA3053.

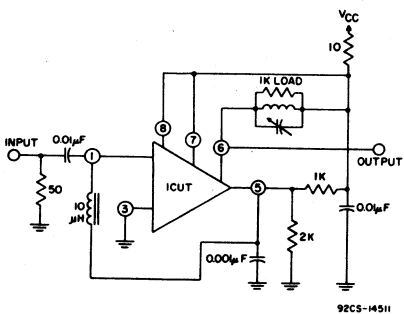


Fig. 22c - Transfer characteristic (voltage gain) test circuit (10.7 MHz) differential-amplifier configuration for CA3028A, CA3028B and CA3053.

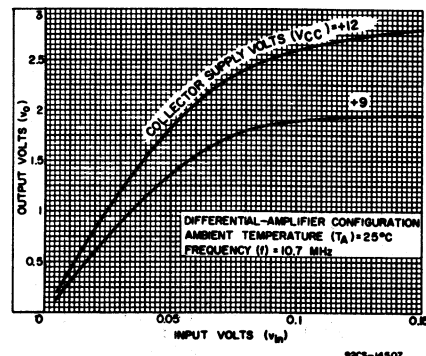


Fig. 22d - Transfer characteristics (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

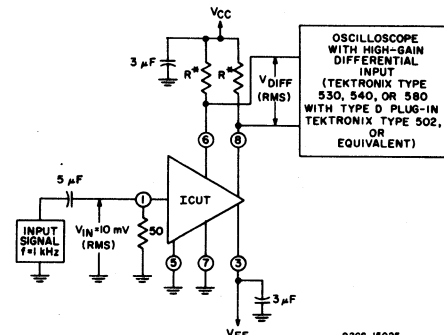


Fig. 23 - Differential voltage gain, maximum peak-to-peak output voltage, and bandwidth test circuit for CA3028B.

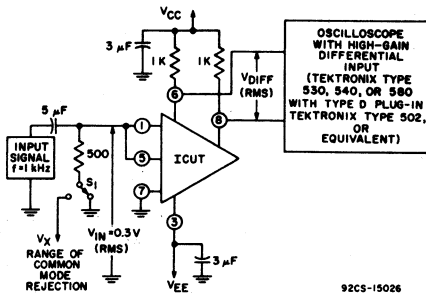


Fig. 24 - Common-mode rejection ratio and common-mode input-voltage range test circuit for CA3028B.