CA3033, CA3047 Types
Operational Amplifiers

For High-Output-Current Applications

RCA-CA3033 is a high-performance integrated circuit operational amplifier featuring high input impedance, high gain, high power output, and low input-offset voltage and current. The device consists of two differential amplifiers in cascade and a single-ended class-B power output stage on a single monolithic silicon chip.

RCA-CA3033A has all the superior features and characteristics of the CA3033 but, in addition, can be operated at higher supply voltages to provide higher gain, higher common mode rejection, greater maximum output voltage swing, and more than double the power output.

RCA-CA3033 and CA3033A are hermetically sealed in 14-lead "dual-in-line" ceramic packages and are designed for operation over the full military temperature range of −55 °C to +125 °C.

The RCA-CA3047 and CA3047A are supplied in 14-lead "dual-in-line" plastic packages and are designed to operate over the temperature range of 0°C to +70 °C, ambient.

Companion Application Note, ICAN-5641 "Application of RCA CA3033 and CA3033A High Performance Integrated-Circuit Operational Amplifiers."

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ±30%.

RCA reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

The RCA-CA3047 and CA3047A are electrically identical to the CA3033 and CA3033A, respectively, but are limited in operating and storage temperature range.

FEATURES

	CA3033 CA3047 V⁺ = +12 V V⁻ = −12 V	CA3033A CA3047A V⁺ = 15 V V⁻ = −15 V	
■ Output Current	36	76	mA min.
■ Input Offset Current	35	25	nA max.
■ Open Loop Differential Gain	84	87	dB min.
■ Output Voltage Swing	18	23	V_{p-p} min.
■ Input Bias Current	350	180	nA max.
■ Power Output	80	220	mW min.
■ Common Mode Rejection Ratio	84	93	dB min.

APPLICATIONS

- Comparator
- Integrator
- Differentiator
- Audio Amplifier
- Summing Amplifier
- Servo Driver
- DC Amplifier
- Multivibrator
- Narrow Band and Band Pass Amplifier

ABSOLUTE-MAXIMUM RATINGS

	CA3033	CA3033A	CA3047	CA3047A
INPUT SIGNAL VOLTAGE	±10 V	−13 V, +10 V	±10 V	−13V, +10 V
DEVICE DISSIPATION:				
Up to T_A = 25 °C	1.2 W	1.2 W	750 mW	750 mW
Above T_A = 25 °C	Derate at 8 mW/°C		Derate at 6.67 mW/°C	
TEMPERATURE RANGE:				
Operating	−55 °C to +125 °C		0 °C to +70 °C	
Storage	−65 °C to +150 °C		−65 °C to +150 °C	
LEAD TEMPERATURE (During Soldering):				
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265 °C			

MAXIMUM VOLTAGE RATINGS at T_A = 25° C — CA3033, CA3047

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 1 with respect to the horizontal terminal 14 is 0 to +4 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1		*	*	*	*	*	*	*	*	*	*	*	*	+4 0
2			*	*	*	*	*	*	*	*	*	*	*	+26 0
3				*	*	0 -26	*	*	*	*	*	*	*	+26 0
4					+5 -1	0 -15	*	*	*	*	*	*	*	+26 0
5						0 -26	*	+20 -1 Note 1	*	*	*	*	+20 -1 Note 1	*
6							+26 0	+26 0	+26 0	+26 0	+26 0	+26 0	+26 0	+26 0
7								+20 -2 Note 1	*	*	*	*	+20 -2 Note 1	+26 0
8									+20 -1 Note 2	+20 -2 Note 3	+20 -2 Note 3	+20 -1 Note 2	*	+26 0
9										+1 -5	*	+5 -5	+1 -20 Note 2	+26 -5
10											+10 -10	*	+2 -20 Note 3	+26 -10
11												+1 -5	+2 -20 Note 3	+26 -10
12													+1 -20 Note 2	+26 -5
13														*
14														Substrate

MAXIMUM CURRENT RATINGS

CA3033 CA3047
CA3033A CA3047A

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	5	5
2	20	-
3	50	50
4	10	10
5	5	5
6	-	-
7	5	5
8	1	1
9	1	0.1
10	1	0.1
11	1	0.1
12	1	0.1
13	1	1
14	-	-

Notes: 1. This rating applies to the more positive terminal of terminals 8 and 13.
2. This rating applies to the more positive terminal of terminals 9 and 12.
3. This rating applies to the more positive terminal of terminals 10 and 11.

*Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

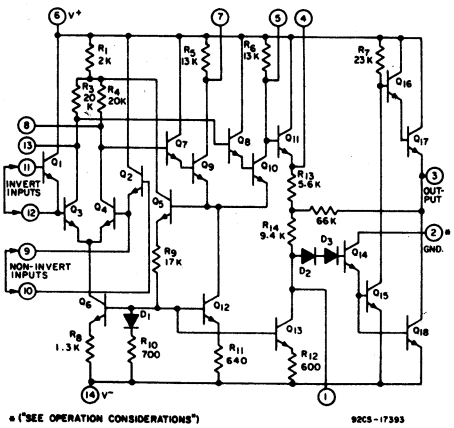


Fig. 1 - Schematic diagram of operational amplifiers, CA3033, CA3033A, CA3047, CA3047A.

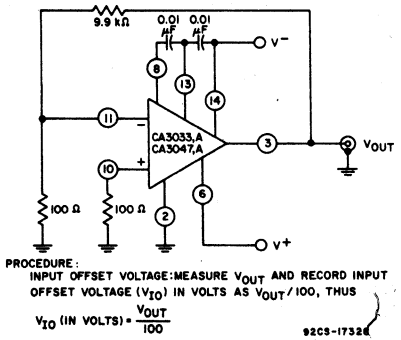


Fig. 2a - Input offset voltage, input offset voltage sensitivity, and device dissipation test circuit.

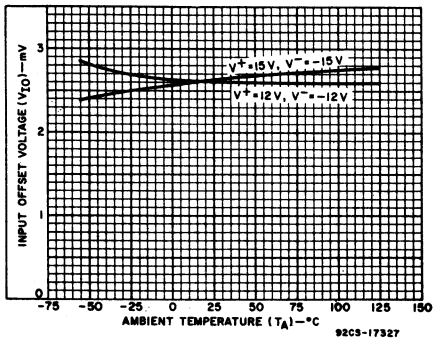


Fig. 2b - Typical input offset voltage vs. ambient temperature.

CA3033, CA3047 Types

MAXIMUM VOLTAGE RATINGS at T_A = 25° C — **CA3033A, CA3047A**

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 1 with respect to the horizontal terminal 14 is 0 to +4 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1		*	*	*	*	*	*	*	*	*	*	*	*	+4 0
2			*	*	*	*	*	*	*	*	*	*	*	+38 0
3				*	*	0 -38	*	*	*	*	*	*	*	+38 0
4					+5 -1	0 -22	*	*	*	*	*	*	*	+38 0
5						0 -38	*	+30 -1 Note 1	*	*	*	*	+30 -2 Note 1	*
6							+38 0	+38 0	+38 0	+38 0	+38 0	+38 0	+38 0	+38 0
7								+30 -2 Note 1	*	*	*	*	+20 -2 Note 1	+38 0
8									+30 -1 Note 2	+30 -2 Note 3	+30 -2 Note 3	+30 -1 Note 2	*	+38 0
9										+1 -5	*	+5 -5	+1 -30 Note 2	+38 -5
10											+10 -10	*	+2 -20 Note 3	+38 -10
11												+1 -5	+2 -30 Note 3	+38 -10
12													+1 -30 Note 2	+38 -5
13														*
14														Sub-strate

Notes: See CA3033, CA3047 Rating Chart Notes.

MAXIMUM CURRENT RATINGS are identical for all four types (See CA3033, CA3047 chart)

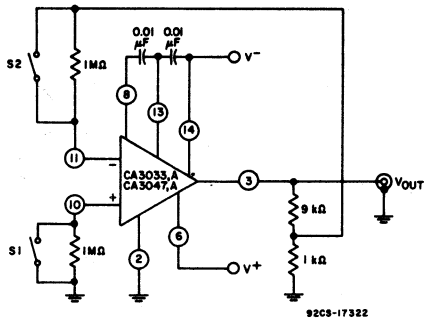


Fig. 3a - Input offset current and input bias current test circuit.

PROCEDURES:

A. Inverting Input Current
Set switch, S_1 in closed position and set switch, S_2 in open position.
Measure output voltage and convert this reading to inverting input current using the following relation:

$$I_I \text{ inverting (in } \mu A) = \frac{V_{OUT} \text{ (in volts)}}{10}$$

B. Non-inverting Input Current
Set switch, S_1 in open position and set switch, S_2 in closed position.
Measure output voltage and convert this reading to non-inverting input current using the following relation:

$$I_I \text{ non-inverting (in } \mu A) = \frac{-V_{OUT} \text{ (in volts)}}{10}$$

C. Input Offset Current
Set switches, S_1 and S_2 in open positions.
Measure output voltage and convert this reading to input offset current using the following relation:

$$I_{IO} \text{ (in } \mu A) = \frac{V_{OUT} \text{ (in volts)}}{10}$$

ELECTRICAL CHARACTERISTICS
For Equipment Design

Characteristics	Symbols	Test Conditions: Circuit Fig.	Test Conditions: T_A = 25° C		Test Conditions: Typical Characteristics Curves Fig.	LIMITS: CA3033 CA3047 (DC Supply Voltage V^+ = 12 V, V^- = −12 V) Min.	Typ.	Max.	LIMITS: CA3033A CA3047A (V^+ = 15 V, V^- = −15 V) Min.	Typ.	Max.	Units
Input Offset Voltage	V_{IO}	2a			2b	–	2.6	5	–	2.9	5	mV
Input Offset Current	I_{IO}	3a			3b	–	5	35	–	9	25	nA
Input Bias Current	I_I	3a			3c	–	70	350	–	100	180	nA
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V^+$	2a			–	–	0.3	0.5	–	0.2	0.5	mV/V
Negative	$\Delta V_{IO}/\Delta V^-$	2a			–	–	0.3	0.5	–	0.2	0.5	mV/V
Device Dissipation	P_T	2a			–	60	120	180	80	170	300	mW
Open-Loop Differential Voltage Gain	A_{OL}	–	f = 1 kHz		4	84	90	–	87	93	–	dB
Common-Mode Rejection Ratio	CMRR	–			5	84	100	–	93	105	–	dB
Common-Mode Input-Voltage Range	V_{ICR}	–	f = 1 kHz		–	−7.5	+5,−9	+3.5	−9.7	6,−11	4.7	V
Maximum Output-Voltage Swing	$V_{O(P-P)}$	–		R_L = 500 Ω	–	18	22	–	–	–	–	Vp-p
				R_L = 300 Ω		–	–	–	23	25	–	
Input Impedance	Z_I	–			–	0.25	1.5	–	0.6	1	–	MΩ
Output Current	I_O	–		R_L = 500 Ω	6	35	44	–	–	–	–	mA-(P-P)
				R_L = 300 Ω		–	–	–	76	83	–	
Power Output THD <5%	P_o	–		R_L = 500 Ω	7	80	122	–	–	–	–	mW
				R_L = 300 Ω		–	–	–	220	255	–	

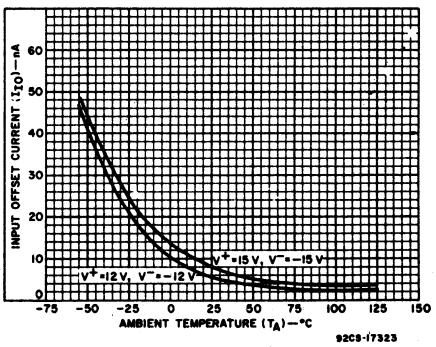


Fig. 3b - Typical input offset current vs. ambient temperature.

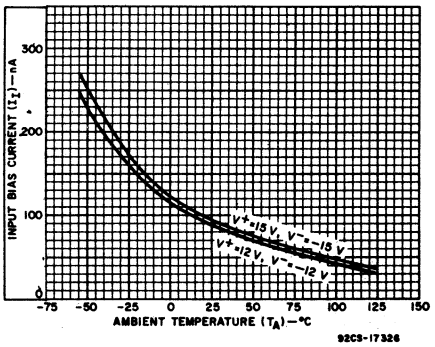


Fig. 3c - Typical input bias current vs. ambient temperature.

CA3033, CA3047 Types

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

Input Offset Voltage Drift −55°C to 125°C	$V_{IO}/\Delta T$	2a		2b	–	6.6	–	–	6.6	–	μV/°C
Input Offset Current Drift											
−55°C to 25°C	$I_{IO}/\Delta T$	3a		3b	–	1	–	–	1	–	nA/°C
25°C to 125°C					–	0.08	–	–	0.08	–	
60-dB Amplifier Bandwidth	BW	8a	C_x, C_y = 0.001 μF	8b,c	–	230	–	–	350	–	kHz
Slew Rate	SR	9	(amplifier circuit only)	–	–	2.7	–	–	3	–	V/μs

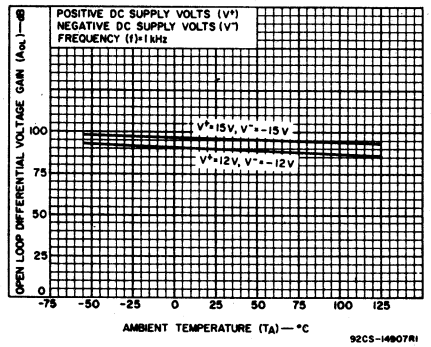


Fig. 4 - Typical open-loop differential voltage gain vs. ambient temperature.

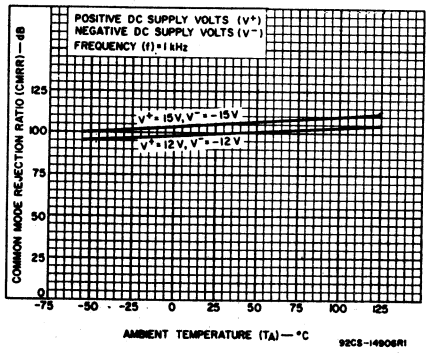


Fig. 5 - Typical common mode rejection ratio vs. ambient temperature.

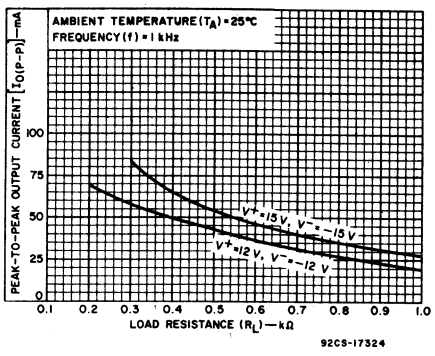


Fig. 6 - Typical peak-to-peak output current vs. load resistance.

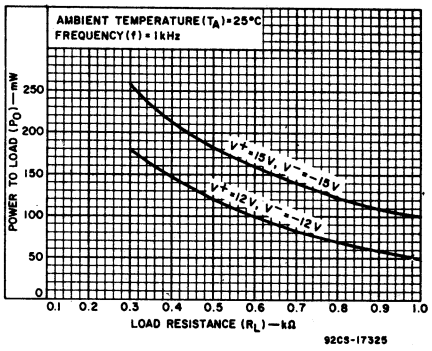


Fig. 7 - Typical power output vs. load resistance.

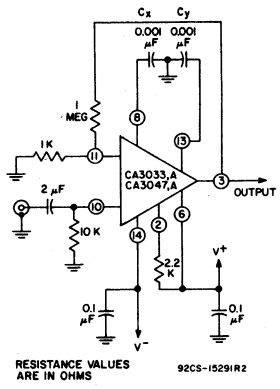


Fig. 8a - Typical 60-dB amplifier.

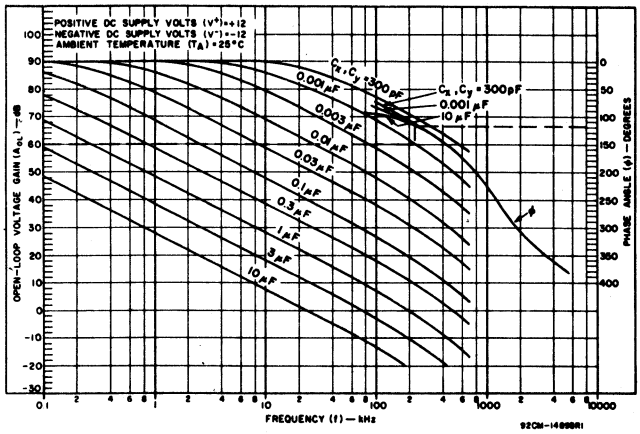


Fig. 8b - Typical phase compensation characteristics for CA3033, CA3047 (V^+ = +12 V, V^- = −12 V)

For any desired closed loop gain (in decibels), read horizontally along the gain line to the attenuation curve which provides the desired closed loop bandwidth. The required values for the compensation capacitors is shown on the curve. Move vertically from the intersection of the gain and attenuation lines until the phase angle curve (ϕ) is reached and read the phase angle between the input and output on the right-hand scale. The difference between the indicated phase angle and 180° is the typical phase margin. (A minimum phase margin of 45° is recommended to allow for component variations and differences among amplifiers.) If the phase margin is smaller than required, the desired bandwidth can be stably achieved through the use of a more complex feedback network. As the closed loop gain approaches unity, the compensating capacitors required (0.3 μF to 1.0 μF) are bulky and costly. A capacitor one-half the value shown on the chart, connected between terminals 8 and 13, and a 0.001 μF capacitor from either terminals 8 or 13 to ground or V^- is an acceptable alternative method. This arrangement provides the same gain-phase roll-off shown on the curves and permits the use of more readily available, lower-voltage disc capacitors which are smaller and cost less. For linear operation, the maximum expected difference voltage between the two collectors is less than 1 volt.

Figure 8a shows the phase compensating capacitors (C_x, C_y) returned to ground. In some systems with large parasitic impedances in the power supply system, returning these capacitors to the negative (V^-) supply may result in more stable operation.

CA3033, CA3047 Types

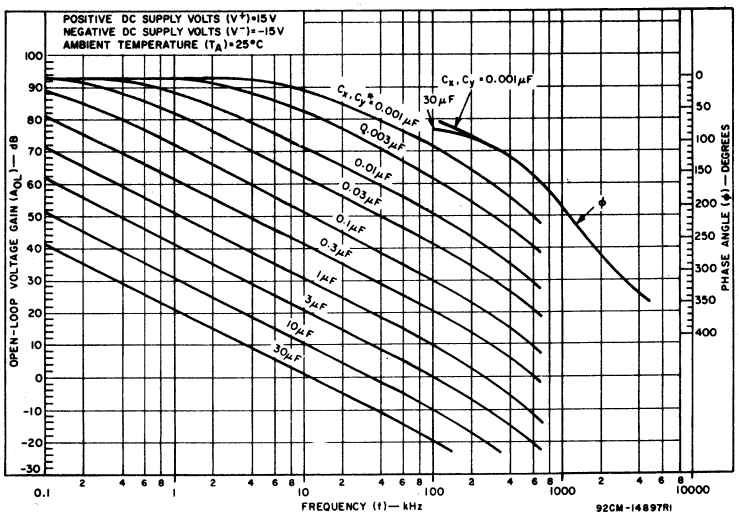
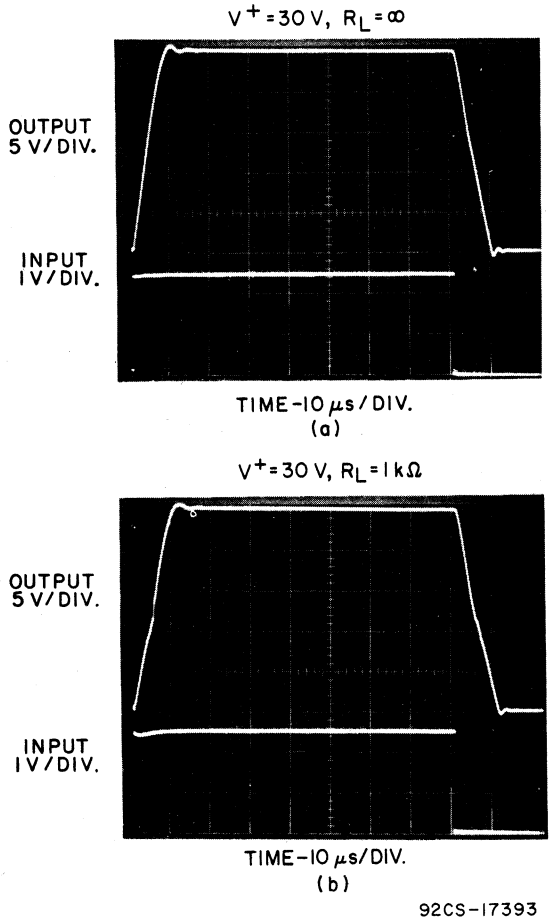
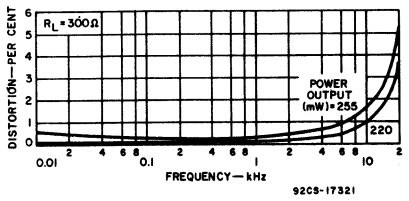


Fig. 8c - Typical phase compensation characteristics for CA3033A, CA3047A (V^+ = 15 V, V^- = −15 V).





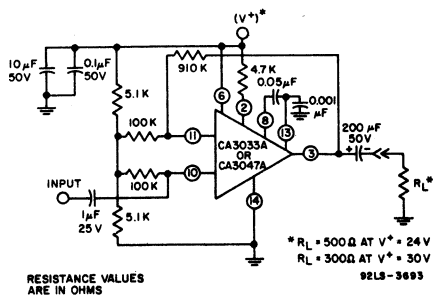


Fig. 9 - Amplifier with single voltage supply and associated pulse response waveforms and distortion curves.

OPERATING CONSIDERATIONS

The CA3033, CA3033A, CA3047, and CA3047A operational amplifiers have very high peak-pulse current capability. The open-loop output impedance is typically less than 30 ohms at 10 kHz and the peak short-circuit output current may exceed 100 milliamperes. To prevent possible damage to the chip because of excessive dissipation it is important that the output stage is not subjected to sustained high peak currents. To minimize the possibility of damage from accidental shorts, it is recommended that a 51-ohm resistor be placed in series with the output circuit.

When high peak output currents are required of the amplifier, it is desirable to provide a current-limiting resistor of about 2200 ohms in series with the collector of transistor Q_{14}. This resistor may be returned to ground, or, if its value is increased to 4700 ohms; it may be returned to the V^+ terminal.

CA3035, CA3035V1

Ultra-High-Gain Wide-Band Amplifier Array

Monolithic Silicon

- Three Individual General-Purpose Amplifiers
- Ideal for service in Remote-Control Amplifiers — — e.g., TV Receivers
- Available in two electrically identical versions: CA3035 with straight leads; CA3035V1 with formed leads

HIGHLIGHTS

- Three separate amplifiers — gain and bandwidth for each amplifier can be adjusted with suitable external circuitry
- Amplifiers operable independently or in cascade
- Exceptionally high cascade voltage gain — 129 dB typ. at 40 kHz
- Low noise performance
- Wide-band response
- All amplifiers single-ended — only one power supply required
- Wide operating temperature range — -55°C to +125°C
- Built-in temperature compensation
- Hermetically sealed, all-welded 10-lead TO-5-style metal package with straight or formed leads

ABSOLUTE-MAXIMUM RATINGS:

Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Device Dissipation ..... 300 mW
Input Voltage ..... 1 V p-p
Supply Voltage ..... +15V
Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. ..... +265°C

ELECTRICAL CHARACTERISTICS AT T_A = 25°C

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	TEST CIRCUITS AND CHARACTERISTICS CURVES	LIMITS CA3035, CA3035V1 Min.	Typ.	Max.	UNITS
STATIC CHARACTERISTICS							
Quiescent Operating Voltage	V3 V5 V7	V_{CC} = +9V	Fig.3	– – –	2 1.9 4.9	– – –	V V V
Total Current Drain	I_d	V_{CC} = +9V, R_{L3} = 5KΩ	Fig.3	3.5	5	7.5	mA
DYNAMIC CHARACTERISTICS							
Voltage Gain: Amplifier No.1 Amplifier No.2 Amplifier No.3	 A_1 A_2 A_3	f = 40 kHz, V_{CC} = +9V		 40 40 38	 44 46 42	 – – –	 dB dB dB
Output Voltage Swing	V_{out} V_{1out} V_{2out} V_{3out}	R_{L1} = 10KΩ R_{L2} = 10KΩ R_{L3} = 5KΩ Sinusoidal Output, V_{CC} = +9V		 – – –	 2 2.6 8	 – – –	 Vp-p Vp-p Vp-p
Input Resistance: Amplifier No.1 Amplifier No.2 Amplifier No.3	 R_1in R_2in R_3in	f = 40 kHz		 – – –	 50K 2K 670	 – – –	 Ω Ω Ω
Output Resistance	R_1out R_2out R_3out	f = 40 kHz		– – –	270 170 100K	– – –	Ω Ω Ω
Bandwidth at -3dB point: Amplifier No.1 Amplifier No.2 Amplifier No.3	 BW_1 BW_2 BW_3	V_{CC} = +9V	 Fig.5 Fig.6 Fig.7	 – – –	 500 2.5 2.5	 – – –	 kHz MHz MHz
Noise Figure Amplifier No.1	NF_1	f = 1 kHz, R_S = 1 KΩ	Fig.4	–	6	7	dB
Sensitivity		V_{CC} = +13 V Relay (K_1) Current = 7.5 mA	Fig.2	–	100	150	μV

SCHEMATIC DIAGRAM FOR CA3035 AND CA3035V1

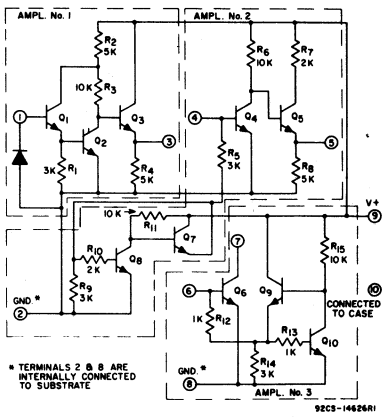


Fig. 1

TYPICAL REMOTE CONTROL SYSTEM

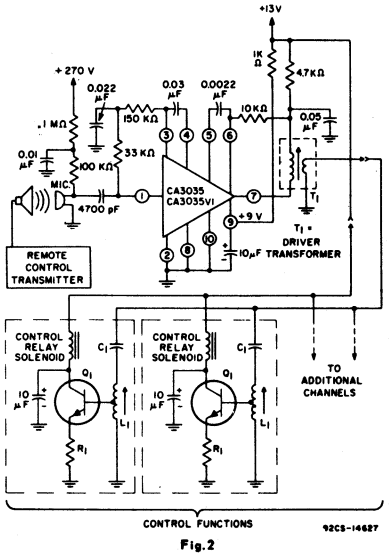


Fig. 2

STATIC CHARACTERISTICS TEST CIRCUIT

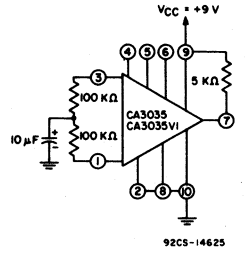
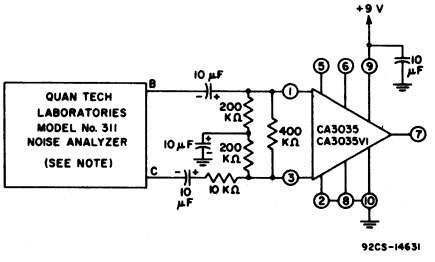


Fig. 3

NOISE FIGURE TEST CIRCUIT

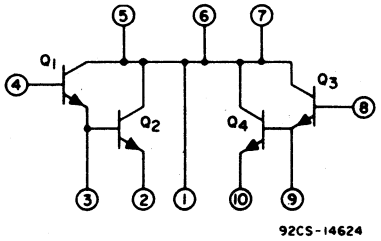


NOTE: SET ALL INTERNAL POWER SUPPLIES ON QUAN TECH NOISE ANALYZER TO ZERO VOLTS.

Fig. 4

CA3036
DUAL DARLINGTON ARRAY

- Two independent low-noise wide-band amplifier channels
- Particularly useful for preamplifier and low-level amplifier applications in single-channel and stereo systems
- Wide application in low-noise industrial instrumentation amplifiers



92CS-14624

Fig.1 – Schematic Diagram for CA3036.

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

CHARACTERISTICS		SYMBOLS	TEST CONDITIONS	LIMITS TYPE CA3036 Min.	Typ.	Max.	UNITS
For Each Transistor (Q_1, Q_2, Q_3, Q_4)	Collector-Cutoff Current	I_{CBO}	V_{CB} = 5V, I_E = 0	–	–	0.5	μA
	Collector-Cutoff Current	I_{CEO}	V_{CE} = 10 V, I_B = 0	–	–	5	μA
	Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	15	20	–	V
	Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	30	44	–	V
	Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	5	6	–	V
For Either Input Transistor (Q_1 or Q_3)	Static Forward Current-Transfer Ratio	h_{FE}	I_{C1} or I_{C3} = 1 mA	30	82	–	–
For Either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)	Emitter-to-Base Breadkown Voltage	$V_{(BR)EBO(D)}$	I_{E2} or I_{E4} = 10 μA	10	12.6	–	V
	Static Forward Current-Transfer Ratio	$h_{FE(D)}$	$I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ = 1 mA	1000	4540	–	–
For Each Input Transistor (Q_1 or Q_3)	Short-Circuit Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, I_{C1} or I_{C3} = 1 mA	–	82	–	–
	Short-Circuit Input Impedance	h_{ie}		–	2.6K	–	Ω
	Open-Circuit Output Admittance	h_{oe}		–	7	–	μmho
	Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		–	9.8 x 10-5	–	–
For Either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)	Short-Circuit Forward Current-Transfer Ratio	$h_{fe(D)}$	f = 1 kHz, $I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ = 1 mA	–	1300	–	–
	Short-Circuit Input Impedance	$h_{ie(D)}$		–	82K	–	Ω
	Open-Circuit Output Admittance	$h_{oe(D)}$		–	108	–	μmho
	Open-Circuit Reverse Voltage-Transfer Ratio	$h_{re(D)}$		–	2.7 x 10-3	–	–
	Voltage Gain	$A_{(D)}$		–	26	–	dB
	Power Gain	$G_{p(D)}$		–	47	–	dB
	Noise Voltage See Fig.3 for Test Circuit	E_N	f = 100 Hz	–	0.2	3	$\mu V(rms)/\sqrt{f(Hz)}$
			f = 1 kHz	–	0.05	0.3	
			f = 10 kHz	–	0.012	0.1	
For Either Input Transistor (Q_1 or Q_3)	Forward Transfer Admittance	y_{fe}	f = 50 MHz, I_{C1} or I_{C3} = 2 mA	–	0.68 + j 7.9	–	mmho
	Input Admittance (Output Short-Circuited)	y_{ie}		–	4.14 + j 5.95	–	mmho
	Output Admittance (Input Short-Circuited)	y_{oe}		–	1.94 + j 2.64	–	mmho
	Reverse Transfer Admittance (Input Short-Circuited)	y_{re}		–	Negligible	–	mmho
For either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)	Input Admittance (Output Short-Circuited)	$y_{ie(D)}$	f = 50 MHz, $I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ = 2 mA	–	1.71 + j 2.8	–	mmho
	Output Admittance (Input Short-Circuited)	$y_{oe(D)}$		–	3.96 + j 2.6	–	mmho
	Gain-Bandwidth Product	$f_T(D)$		150	200	–	MHz

HIGHLIGHTS

- Matched transistors with emitter-follower outputs
- Low-noise performance
- 200-MHz gain-bandwidth product
- Operation from -55°C to +125°C
- Hermetically sealed, all-welded 10-lead TO-5-style metal package

APPLICATIONS

- Stereo phonograph preamplifiers
- Low-level stereo and single channel amplifier stages
- Low-noise, emitter-follower differential amplifiers
- Operational amplifier drivers

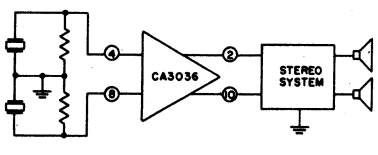
MAXIMUM RATINGS, Absolute-Maximum Values:

POWER DISSIPATION, P:
- Any one transistor . . . . . 300 max. mW
- Total for array . . . . . 600 max. mW

TEMPERATURE RANGE:
- Operating . . . . . –55 to +125 °C
- Storage . . . . . –65 to +150 °C

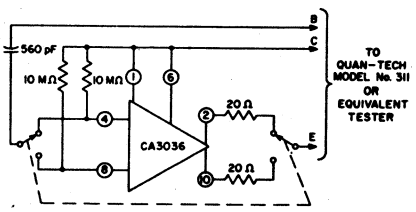
LEAD TEMPERATURE (During Soldering):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . . +265 °C

The following ratings apply for each transistor in the array:
- Collector-to-Emitter Voltage, V_{CEO} . . . . 15 max. V
- Collector-to-Base Voltage, V_{CBO} . . . . . 30 max. V
- Emitter-to-Base Voltage, V_{EBO} . . . . . 5 max. V
- Collector Current, I_C . . . . . 50 max. mA



92CS-14633R1

Fig.2 - Block Diagram of Stereo System using CA3036 as Phono Preamplifier.



92CS-14628

Fig.3 - Noise Voltage Test Circuit for CA3036.

CA3039

Diode Array

Six Matched Diodes on a Common Substrate

ULTRA-FAST LOW-CAPACITANCE MATCHED DIODES

For Applications in Communications and Switching Systems

The RCA-CA3039 consists of six ultra-fast, low capacitance diodes on a common monolithic substrate. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the array extremely useful for a wide variety of applications in communication and switching systems.

Five of the diodes are independently accessible, the sixth shares a common terminal with the substrate.

For applications such as balanced modulators or ring modulators where capacitive balance is important, the substrate should be returned to a DC potential which is significantly more negative (with respect to the active diodes) than the peak signal applied.

APPLICATIONS

- Balanced modulators or demodulators
- Ring modulators
- High speed diode gates
- Analog switches

FEATURES

- Excellent reverse recovery time – 1 ns typ.
- Matched monolithic construction – V_F matched within 5 mV
- Low diode capacitance – C_D = 0.65 pF typical at V_R = –2 V
- The CA3039 is available in a sealed-junction Beam-Lead version (CA3039L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".
- Supplied in the hermetic 12-lead TO-5 style package

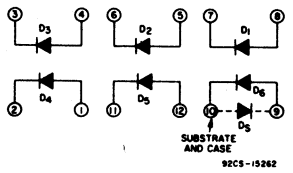


Fig. 1 - Schematic Diagram for CA3039

ABSOLUTE MAXIMUM RATINGS AT T_A = 25°C

DISSIPATION:	
Any one diode unit	100 mW
Total for device	600 mW
For T_A > 55°C	derate linearly 5.7 mW/°C
TEMPERATURE RANGE:	
Operating	–55 to +125°C
Storage	–65 to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C
PEAK INVERSE VOLTAGE, PIV for: D_1–D_5	5 V
D_6	0.5 V
PEAK DIODE-TO-SUBSTRATE VOLTAGE, V_{DI} for D_1–D_5 (term. 1,4,5,8 or 12 to term. 10)	+20, –1 V
DC FORWARD CURRENT, I_F	25 mA
PEAK RECURRENT FORWARD CURRENT, I_f	100 mA
PEAK FORWARD SURGE CURRENT, $I_{f(surge)}$	100 mA

ELECTRICAL CHARACTERISTICS, at T_A = 25° C

Characteristics apply for each diode unit, unless otherwise specified.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS			UNITS	CHARACTERISTIC CURVES
			MIN.	TYP.	MAX.		FIG.
DC Forward Voltage Drop	V_F	I_F = 50 μA	–	0.65	0.69	V	2
		1 mA	–	0.73	0.78	V	
		3 mA	–	0.76	0.80	V	
		10 mA	–	0.81	0.90	V	
DC Reverse Breakdown Voltage	$V_{(BR)R}$	I_R = –10 μA	5	7	–	V	–
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	$V_{(BR)R}$	I_R = –10 μA	20	–	–	V	–
DC Reverse (Leakage) Current	I_R	V_R = –4 V	–	0.016	100	nA	3
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	I_R	V_R = –10 V	–	0.022	100	nA	4
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	$\lvert V_{F_1} - V_{F_2} \rvert$	I_F = 1 mA	–	0.5	5	mV	2
Temperature Coefficient of $\lvert V_{F_1} - V_{F_2} \rvert$	$\frac{\Delta \lvert V_{F_1} - V_{F_2} \rvert}{\Delta T}$	I_F = 1 mA	–	1	–	μV/°C	5
Temperature Coefficient of Forward Drop	$\frac{\Delta V_F}{\Delta T}$	I_F = 1 mA	–	–1.9	–	mV/°C	6
DC Forward Voltage Drop for Anode-to-Substrate Diode (D_S)	V_F	I_F = 1 mA	–	0.65	–	V	–
Reverse Recovery Time	t_{rr}	I_F = 10 mA, I_R = 10 mA	–	1	–	ns	–
Diode Resistance	R_D	f = 1 kHz, I_F = 1 mA	25	30	45	Ω	7
Diode Capacitance	C_D	V_R = –2 V, I_F = 0	–	0.65	–	pF	8
Diode-to-Substrate Capacitance	C_{DI}	V_{DI} = +4 V, I_F = 0	–	3.2	–	pF	9

TYPICAL CHARACTERISTICS

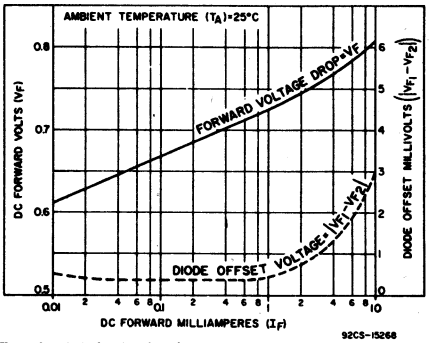


Fig. 2 - DC forward voltage drop (any diode) and diode offset voltage vs DC forward current

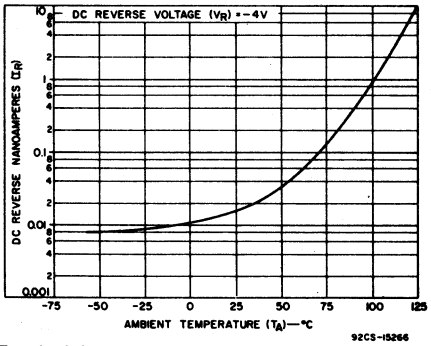


Fig. 3 - DC reverse (leakage) current (diodes 1,2,3,4,5) vs temperature

CA3039

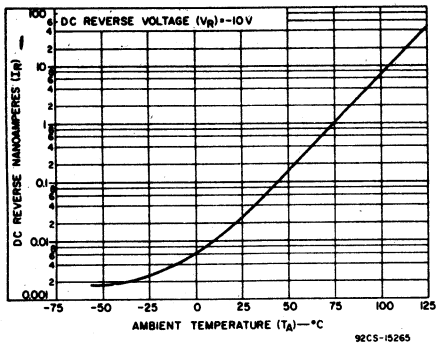


Fig. 4 - DC reverse (leakage) current between diodes (1,2,3,4,5) and substrate vs temperature

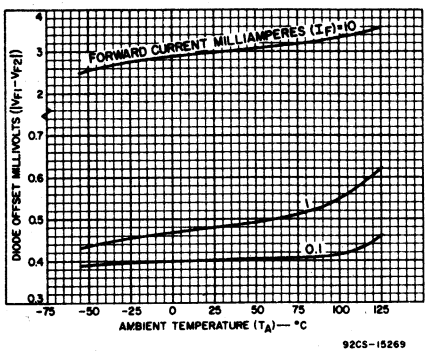


Fig. 5 - Diode offset voltage (any diode) vs temperature

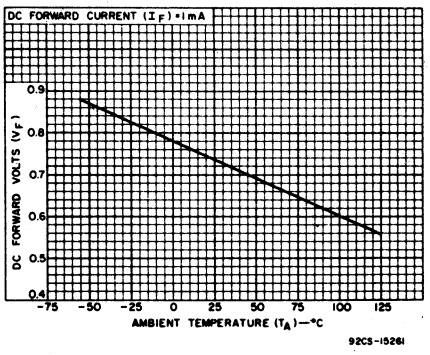


Fig. 6 - DC forward voltage drop (any diode) vs temperature

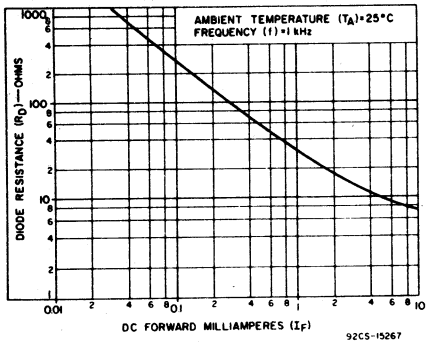


Fig. 7 - Diode resistance (any diode) vs DC forward current

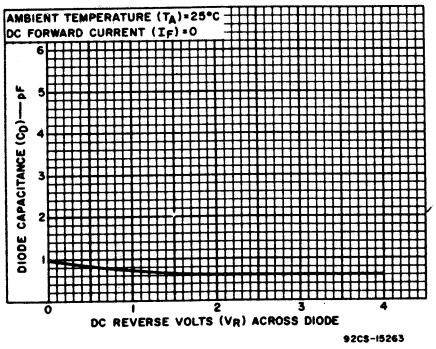


Fig. 8 - Diode capacitance (diodes 1,2,3,4,5) vs reverse voltage

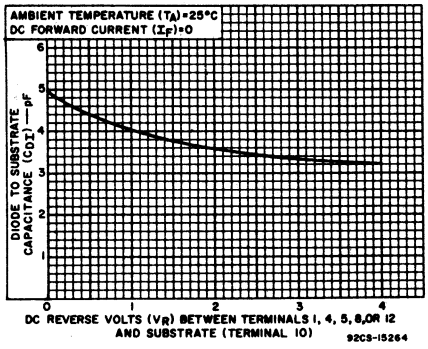


Fig. 9 - Diode-to-substrate capacitance vs reverse voltage