13.-

RCA linear integrated circuits

High-Frequency Wide-Band Amplifier/Phase Detector

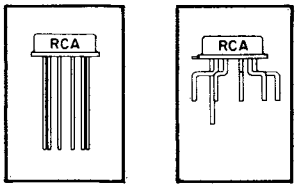
Monolithic Silicon

CA3034
CA3034V1

File No. 273

- Primarily intended for AFC (automatic-frequency-control) applications
- Available in two electrically identical versions: CA3034 with straight leads; CA3034V1 with formed leads

CA3034 CA3034V1



10-LEAD TO-5 — FORMED 10-LEAD TO-5

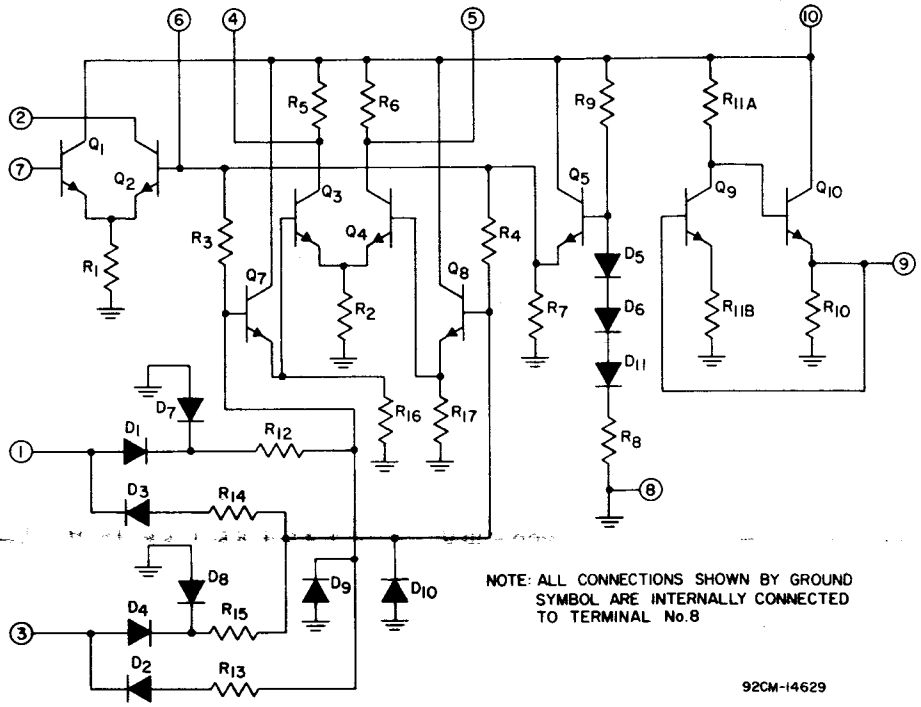


Fig.1 - Schematic Diagram for CA3034 and CA3034V1.

HIGHLIGHTS

- Differential Input Amplifier
- Dual phase detector with differential output amplifier
- Compensated reference voltage supply
- Hermetically sealed all-welded lead TO-5-style metal with straight or formed
- Wide operating-temperature range -55°C to +125°C

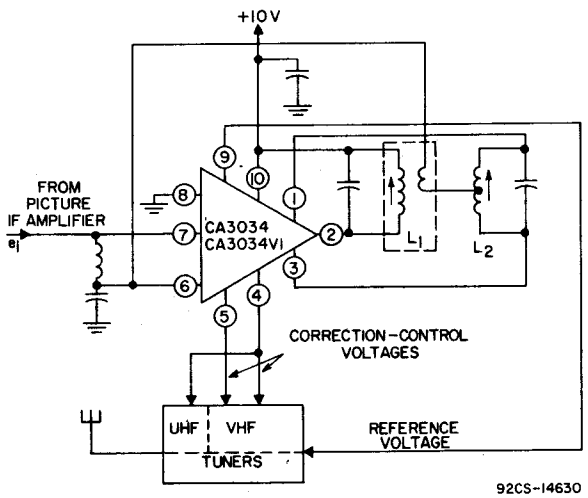


Fig.2 - Block Diagram of Typical AFC Application Using CA3034 or CA3034V1 in Color-TV Receiver.

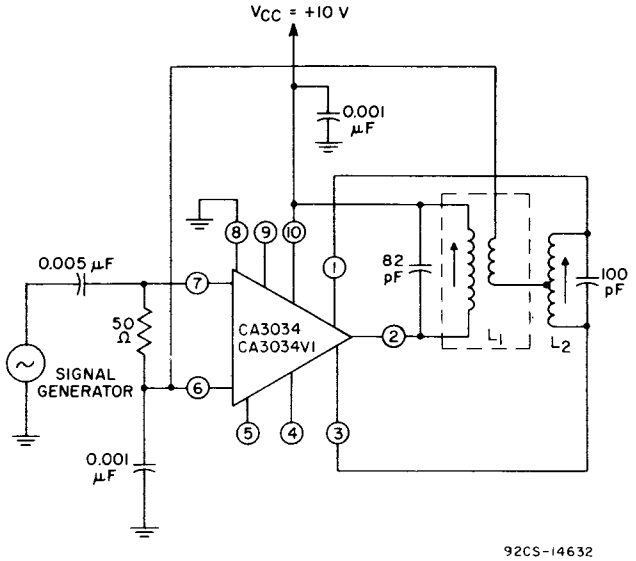
L_1 and L_2 = Phase Detector Transformers

ABSOLUTE MAXIMUM RATINGS:

Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +200°C
Device Dissipation	300 mW
Input Voltage	12 V p-p
Supply Voltage	15 V

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CIRCUIT Fig.	SPECIAL TEST CONDITIONS	LIMITS CA3034, CA3034V1 Min.	Typ.	Max.	UNITS
STATIC CHARACTERISTICS							
Total Current Drain	I_d	--	V_{CC} = 10 V	6.5	9	13	mA
Quiescent Operating Current into Terminal 2	I_2	--	V_{CC} = 10 V	1.3	1.9	2.6	mA
Reference Voltage at Terminal 9	V_9	2	V_{CC} = 10 V	5.3	5.5	5.7	V
Quiescent Operating Voltage at Terminal 4	V_4	--	V_{CC} = 10 V	4.5	5.5	6.5	V
Quiescent Operating Voltage at Terminal 5	V_5	--	V_{CC} = 10 V	4.5	5.5	6.5	V
Output Offset Voltage between Terminals 4&5	V_{4-5}	--	V_{CC} = 10 V	--	0	1.5	V
DYNAMIC CHARACTERISTICS							
Input Impedance (Terminal 7)	Z_{in}	--		--	2K	--	Ω
Correction-Control Voltage at terminal 4	$V_{corr(4)}$	3	V_{CC} = 10 V, V_{in} = 100 mV RMS, f_o in MHz				V
			45.750 -0.025	9.0	--	--	
			45.750 + 0.025	--	--	1.5	
			45.750 -0.500	9.6	--	--	
			45.750 + 0.500	--	--	1.5	
			45.750 -1.15	8.0	--	--	
			45.750 + 1.15	--	--	3.0	
			45.750 -1.55	--	--	8.0	
			45.750 + 1.55	3.0	--	--	
Correction-Control Voltage at terminal 5	$V_{corr(5)}$	3	V_{CC} = 10 V, V_{in} = 100 mV RMS, f_o in MHz				V
			45.750 -0.025	--	--	1.50	
			45.750 + 0.025	9.0	--	--	
			45.750 -0.500	--	--	1.50	
			45.750 + 0.500	9.6	--	--	
			45.750 -1.15	--	--	3.0	
			45.750 + 1.15	8.0	--	--	
			45.750 -1.55	3.0	--	--	
			45.750 + 1.55	--	--	8.0	



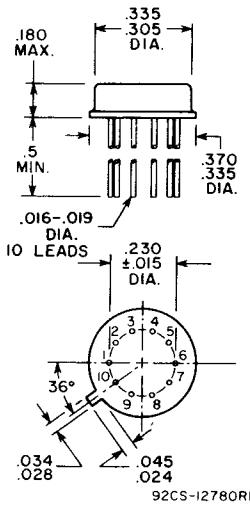
L_1 IS ALIGNED FOR SYMMETRICAL BANDWIDTH ON EITHER SIDE OF 45.750 MHz.

L_2 IS ALIGNED FOR ZERO DIFFERENTIAL OUTPUT BETWEEN TERMINALS 4 AND 5 AT f_0 = 45.750 MHz.

Fig.3 - Correction Voltage Test Circuit for CA3034 and CA3034V1.

DIMENSIONAL OUTLINES

CA3034



CA3034V1