CA3040

VIDEO and WIDE-BAND AMPLIFIER

For Industrial and Commercial Equipment at Frequencies up to 200 MHz

The RCA CA3040 is a monolithic silicon integrated circuit designed to meet the requirements of a wide variety of applications requiring high gain and wide bandwidth. The cascode-connected differential amplifier achieves a double-ended gain of 37 dB with a typical 3 dB bandwidth of 55 MHz. Emitter-Follower input and output stages provide the desirable high input impedance and low output impedance for coupling to other circuits.

The CA3040 includes two biasing options, allowing the user to optimize his design over the entire military temperature range of -55 to +125°C. **Bias Mode A** yields a substantially constant voltage at the output terminals for applications using DC coupling to succeeding stages or requiring maximum dynamic range over the temperature range. DC output voltage varies less than 0.1 volt (typically) over the entire temperature range while gain varies ±2 dB. **Bias Mode B** provides extremely stable gain over the temperature range. Gain variation is 0 dB (typically) in this Bias Mode. DC variation is ±0.8 volt.

Provisions are also made for stabilizing the operating point for either single or split power supplies.

FEATURES

- High Differential Push-Pull Voltage Gain ..... 37 dB typ.
  Single-Ended Voltage Gain ..... 31 dB typ.
- Wide (3dB) Bandwidth ..... 55 MHz typ.
- Balanced Input and Output
- High Input Resistance ..... 150 kΩ typ.
- Low Output Resistance ..... 125 Ω typ.
- Bias Options for Temperature Compensation:
  Bias Mode A: "Constant" Voltage
  Bias Mode B: "Constant" Gain
- **Supplied in the hermetic 12-lead TO-5 style package**

APPLICATIONS

- Video Amplifier
- Modulator
- Mixer
- Schmitt Trigger
- IF Amplifier
- DC Amplifier
- Sense Amplifier

ABSOLUTE-MAXIMUM RATINGS

DISSIPATION * ..... 450 mW
Derating factor for T_A > 85°C ..... 5 mW/°C
TEMPERATURE RANGE:
Operating ..... -55°C to +125°C
Storage ..... -65°C to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. ..... +265°C

* Limitation imposed by the thermal resistance of package.

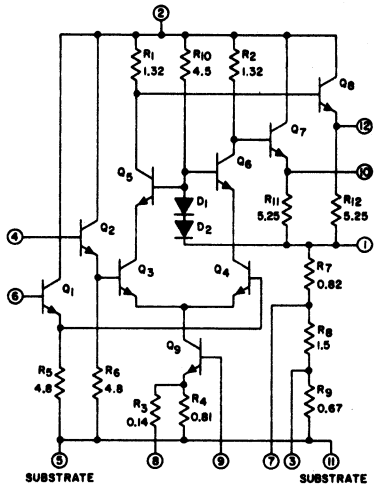


Fig.1 - Schematic Diagram for CA3040

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 2 with respect to terminal 11 is 0 to +14 volts.

TERMINAL No.	1	2	3	4	5▲	6	7	8	9	10	11▲	12
1		0 -14	*	*	+14 0	*	+10 -10	*	*	*	+14 0	*
2			*	+14 0	+14 0	+14 0	*	*	*	+14 0	+14 0	+14 0
3				*	+5 -3	*	*	*	*	*	+5 -3	*
4					*	+3 -3	*	*	*	*	*	*
5▲					▲	*	+10 -3	*	+3 -7	*	0 Note 1	*
6							*	*	*	*	*	*
7								*	*	*	+10 -3	*
8									+3 -3	*	*	*
9										*	+7 -3	*
10											*	*
11▲											▲	*
12												

▲ Reference Substrate

Note 1: External connection required for proper operation.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	5	5
2	-	-
3	5	5
4	1	0.1
5	-	-
6	1	0.1
7	5	5
8	5	5
9	1	0.1
10	-	10
11	-	-
12	-	10

STATIC CHARACTERISTICS TEST CIRCUITS

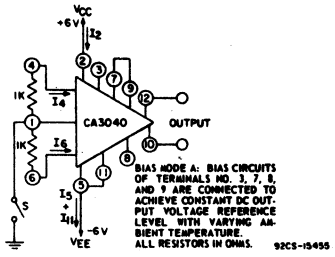


Fig.2(a) - Bias Mode A

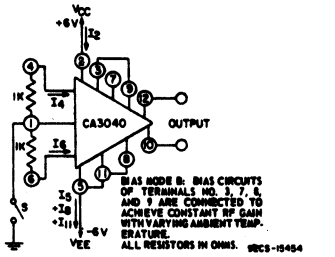


Fig.2(b) - Bias Mode B

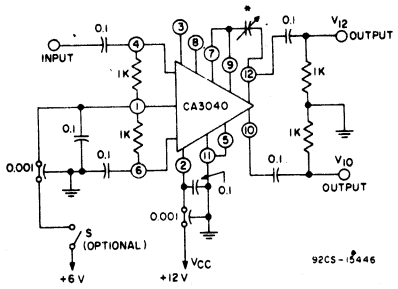
CA3040

ELECTRICAL CHARACTERISTICS AT T_A = 25°C Unless Otherwise Specified

Characteristics	Symbols	Test Circuits Fig.	Special Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
STATIC CHARACTERISTICS	V_{CC} = +6V, V_{EE} = -6V						
Output Voltage	V_{10} or V_{12}	2(a) 2(b)	Bias Mode Switch A or B: Closed	1.4	2.7	3.7	V
Base Bias Voltage	V_9	2(a)	Bias Mode A Switch Closed	-	-1.7	-	V
		2(b)	Bias Mode B Switch Closed	-	-1.7	-	V
Input Bias Reference Voltage	V_1	2(a) 2(b)	Bias Mode Switch A or B: Open	-1	-	+1	V
Input Bias Current	I_4, I_6	2(a) 2(b)	Bias Mode Switch A or B: Closed	-	15	45	μA
Input Unbalance Current	$\lvert I_6 - I_4 \rvert$	2(a) 2(b)	Bias Mode Switch A or B: Closed	-	-	6	μA
Power Supply Current Drain	I_2 or $I_5 + I_{11}$	2(a)	Mode A Switch open or closed	4.7	8.5	15.5	mA
	I_2 or $I_5 + I_8 + I_{11}$	2(b)	Mode B Switch open or closed				
DYNAMIC CHARACTERISTICS	V_{CC} = +12V, V_{EE} = 0, Split Voltage Supply (Optional) = +6V						
Differential Voltage Gain							
Single-Ended Input Differential Output	$A_{DIFF(DE)}$	3(a)	f = 1 MHz, R_S = 50 Ω	34	37	-	dB
Single-Ended Input and Output	$A_{DIFF(SE)}$	3(a)	f = 1 MHz, R_S = 50 Ω	28	31	-	dB
-3 dB Bandwidth	BW	3(a)	R_S = 50 Ω	40	55	-	MHz
Differential Voltage Gain Balance	$A_{DIFF(SE)10} - A_{DIFF(SE)12}$	3(a)	f = 1 MHz	-1	0	+1	dB
Output Voltage Swing	V_8 or V_{10} RMS	3(a)	f = 1 MHz, R_S = 50 Ω	-	0.5	-	VRMS
Noise Figure	NF	3(a)	(Note 1) f = 30 MHz, R_S = 400 Ω	-	7.5	9	dB
Parallel Input Resistance	R_I	3(a)	f = 1 MHz	-	150	-	kΩ
Parallel Input Capacitance	C_I	3(a)		-	2.2	-	pF
Output Resistance	R_O	3(a)		-	125	-	Ω
TEMPERATURE DEPENDENT CHARACTERISTICS Temperature coefficients for ambient temperature: -55°C ≤ T_A ≤ + 125°C							
Output Voltage	$\frac{\Delta V_{10} \text{ or } \Delta V_{12}}{°C}$	3(a)	Bias Mode A	-	0	-	mV/°C
		3(b)	Bias Mode B	-	6.4	-	mV/°C
Power Supply Current Drain	$\Delta I_2/°C$	3(a)	Bias Mode A	-	5	-	μA/°C
Differential Voltage Gain	$A_{DIFF}/°C$	3(a)	Bias Mode A	-	0.0166	-	dB/°C
		3(b)	Bias Mode B	-	0	-	

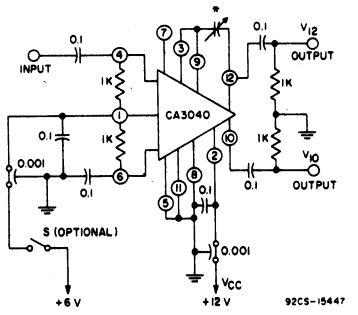
Note 1: Replace 1-kΩ resistors between Term. 1 and 4 and Term. 1 and 6 with suitable chokes so that reactance at 30 MHz exceeds 5kΩ

DYNAMIC CHARACTERISTICS TEST CIRCUITS



* VARIABLE CAPACITANCE (0.5-1.0 μF) ADJUSTMENT FOR EQUAL 3dB BANDWIDTH AT AMPLIFIER OUTPUTS, TERMINALS 10 AND 12.
ALL RESISTORS IN OHMS.
ALL CAPACITORS IN MICROFARADS (UNLESS OTHERWISE INDICATED).
BIAS MODE A IS AS DEFINED IN FIG 2(a)

Fig.3(a) - Bias Mode A



* SEE FIG 3(a)
BIAS MODE B IS AS DEFINED IN FIG 2(b)
ALL RESISTORS IN OHMS.
ALL CAPACITORS IN MICROFARADS (UNLESS OTHERWISE INDICATED).

Fig.3(b) - Bias Mode B

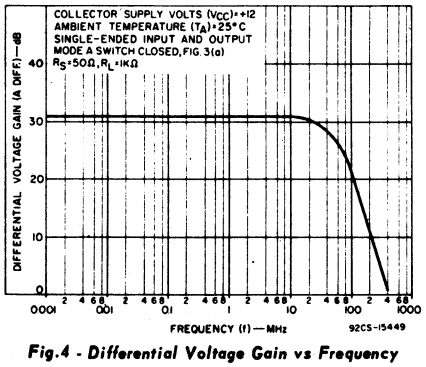


Fig.4 - Differential Voltage Gain vs Frequency

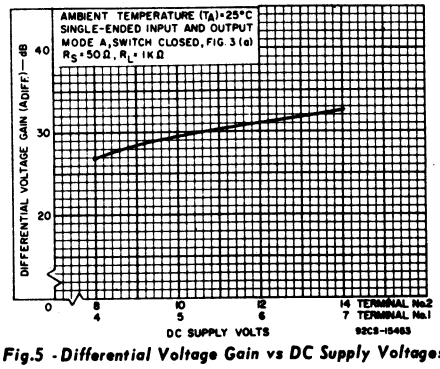


Fig.5 - Differential Voltage Gain vs DC Supply Voltages

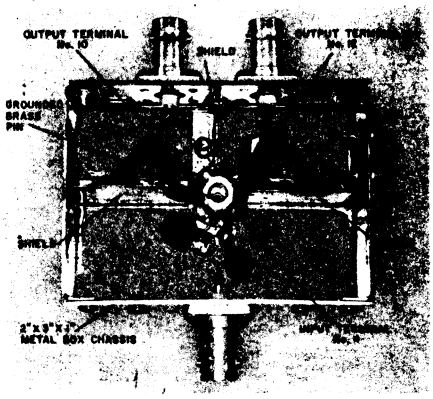


Fig.6 - Test Circuit Layout

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OPERATING CONSIDERATIONS

General

The CA3040 is designed to provide flexibility in the selection of power supply configurations and to provide the circuit designer the choice between two modes of temperature-compensated performance. Mode A, which provides constant DC output voltage, is recommended for most applications. The control of the operating point provided by this mode maintains the dynamic range of the device while gain variation over most of the range is less than ±1 dB. Mode B provides constant gain for applications where this consideration is critical, but will exhibit a reduction of dynamic range at the temperature extremes.

Power Supply Considerations

Figures 2 and 3 illustrate the use of the CA3040 with balanced dual supplies and single power supplies, respectively. Both figures demonstrate that the inputs may be directly referenced to the center point of the supply (ground in Fig.2) by closing the included switch. This is the natural connection in Fig.2. This connection is optional, however, and need not be made. Use of this connection in Fig.3 implies the presence of another DC supply or a "stiff" bleeder. If such a source is present its use is suggested in order to maintain maximum common mode range. Dynamic performance and dynamic range of the output circuit are unaffected by the choice of biasing scheme used so that in most cases direct connection of Terminal No.1 to the center point of the supply is not required. Where direct connection is not used, Terminals No.4 and No.6 must be biased from Terminal No.1 for proper operation.

High-Frequency Considerations

Stable high-frequency operation requires that proper high-frequency construction techniques be followed. The photograph of Fig.6 illustrates the precautions taken in the construction of the test circuit of Fig.3.

Extreme caution is required because of the extended gain bandwidth capability of the device. Oscillations have been observed in the 400-to-800 MHz range when precautions were not taken. In addition to normal considerations of shielding, parts layout, and isolation, the following specific suggestions are made:

1. Use sockets only when necessary. Sockets, when used, must provide shielding within the pin circle. The socket shown in the chassis of Fig.6 is a Barnes MG-1201, or equivalent, modified by drilling a 1/8" hole in the center and inserting a grounded brass pin.
2. Do not bypass Terminal No.9 in normal operation. Fig.3 shows the use of neutralization between Terminal No.9 and one output to balance the amplifier at high frequencies. Experience shows that stable operation, while possible, is difficult to achieve if Terminal No.9 is bypassed to ground.
3. In DC testing, 1 kΩ, 1/4 W carbon resistors should be soldered directly to the socket Terminals No.4 and No.6 to suppress parasitic oscillations. All current carrying connections are made at the other end of the resistors. Direct sensing of Terminal No.4 or No.6 voltage should not be attempted.

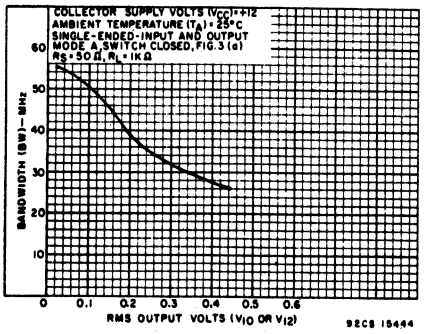

Fig.7 - 3dB Bandwidth vs Single-Ended Output Voltage

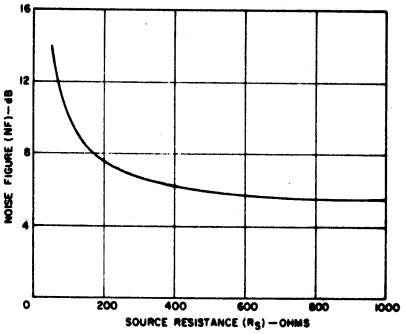

Fig.8 - Noise Figure (NF) vs Source Impedance

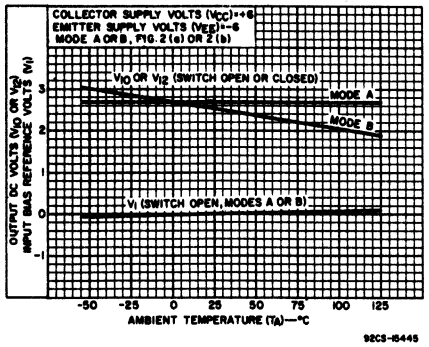

Fig.9 - Output Volts or Input Bias Reference Volts vs Ambient Temperature

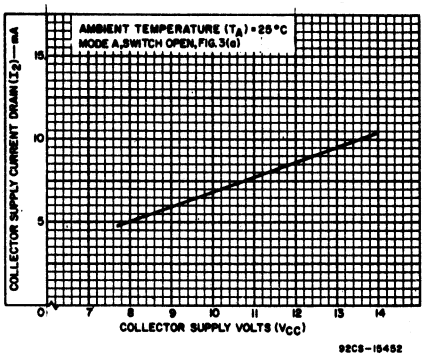

Fig.10 - Collector Supply Current Drain (I_2) vs Collector Supply Voltage (V_{CC})

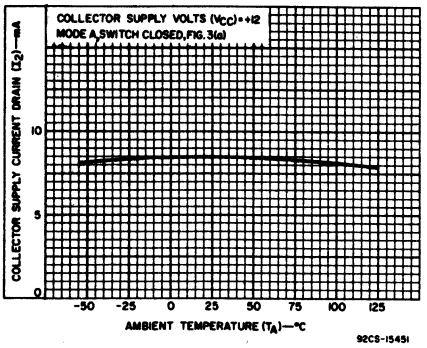

Fig.11 - Collector Supply Current Drain (I_2) vs Ambient Temperature

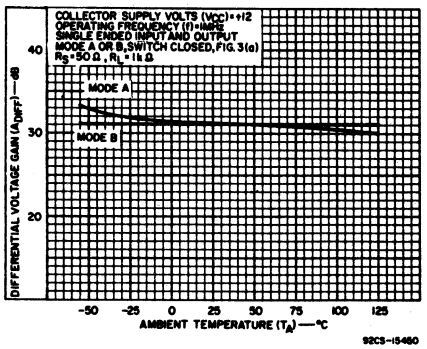

Fig.12 - Single-Ended Differential Voltage Gain vs Ambient Temperature

CA3041

WIDE-BAND AMPLIFIER, FM DETECTOR AF. PREAMPLIFIER/DRIVER

For Sound Sections of TV Receivers Using Tube-Type AF Output Amplifiers

FEATURES

- high-sensitivity – input limiting voltage (knee) = 150 μV typ. at 4.5 MHz
- large audio drive voltage capability
- excellent AM rejection – 58 dB typ. at 4.5 MHz
- inherent high stability – internally shielded
- internal Zener-diode-regulated voltage supply
- low harmonic radiation
- wide frequency capability – <100 kHz to > 20 MHz
- low harmonic distortion

RCA Integrated Circuit Type CA3041 provides, in a single monolithic silicon chip, a major subsystem for the sound sections of TV receivers. As shown in the Schematic Diagram (Fig. 1) and the TV Receiver Block Diagrams (Fig. 12)| the CA3041 contains a multistage wide-band if-amplifier/limiter section, an FM-detector stage, a Zener-diode-regulated power-supply section, and an af-amplifier section specifically designed to drive directly a 6AQ5 beam power tube or other audio output tube of similar characteristics.

In FM receivers, the CA3041 can be used to provide if amplification and limiting, FM detection, and af preamplification.

The CA3041 provides exceptional versatility of circuit design because the if-amplifier/limiter section, FM detector section, and af-preamplifier/driver section can be used independently of each other.

The CA3041 utilizes a 14-lead dual-in-line plastic package with leads specially formed to facilitate automatic insertion of the device in suitably punched printed-circuit boards.

MAXIMUM RATINGS, *Absolute Maximum Values:*

OPERATING-TEMPERATURE RANGE ..... –40° to +85°C
STORAGE-TEMPERATURE RANGE ..... –65° to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C
MAXIMUM INPUT-SIGNAL VOLTAGE:
Between Terminals 1 and 3 ..... ±3 V
MAXIMUM DEVICE DISSIPATION:
At Ambient Temperatures up to +25°C ..... 950 mW
At Ambient Temperatures above +25°C ..... Derate at 10.8 mW/°C

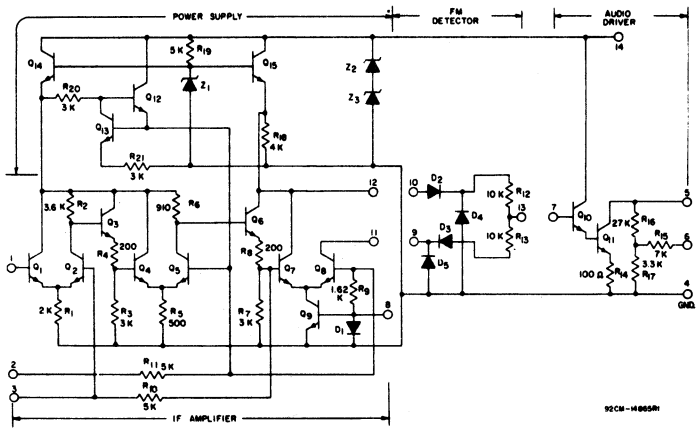

Fig. 1 - Schematic diagram.

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS AT T_A = 25°C

Indicated voltage or current limits for each terminal may be applied under the specified voltage conditions for other terminals. All voltages are with respect to ground (Terminal 4).

TERMINAL	VOLTAGE OR CURRENT LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS													
			1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	-3 V	+3 V	–	AT SAME DC VOLTAGE AS TERMINAL 1	EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL	GROUND (VOLTAGE REFERENCE TERMINAL)	CONNECTED TO +140 V THROUGH 47 kΩ RESISTOR*	CONNECTED TO TERMINAL 7 THROUGH 100 kΩ RESISTOR*	AF-INPUT TERMINAL (EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL)	DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL	AT SAME DC VOLTAGE AS TERMINAL 12 (EXCEPT TERMINAL 9)	AT SAME DC VOLTAGE AS TERMINAL 12 (EXCEPT TERMINAL 10)	AT SAME DC VOLTAGE AS TERMINAL 12 (EXCEPT TERMINAL 11)	EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL	AT SAME DC VOLTAGE AT TERMINAL 12 (EXCEPT TERMINAL 13)	CONNECTED TO +140 V DC THROUGH 6.2-kΩ RESISTOR*
2	-3 V	+3 V	-3 to +3													
3	-3 V	+3 V	-3 to +3													
4	GROUND (VOLTAGE REFERENCE TERMINAL)		-3 to +3													
5	20 mA		-3 to +3													
6	0 V	+10 V	-3 to +3													
7	10 mA		-3 to +3													
8	10 mA		-3 to +3													
9	10 mA		-3 to +3													
10	10 mA		-3 to +3													
11	+2.5 V	+5 V	-3 to +3													
12	+2.5 V	+5 V	-3 to +3													
13	+2.5 V	+5 V	-3 to +3													
14	50 mA		-3 to +3													

* Any other combination of DC Supply Voltage and Series Resistance which will not cause the Maximum Device Dissipation Limit or any of the Maximum Voltage or Current Limits for the CA3041 to be exceeded may be used.

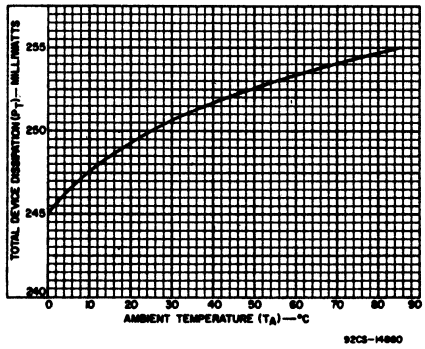

Fig. 2 - Typical dissipation characteristic for CA3041.

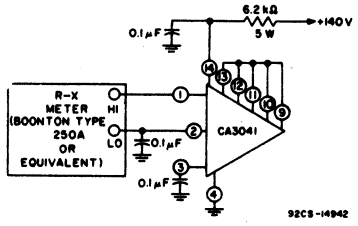

Fig. 3 - Test setup for measurement of input-impedance components.

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ELECTRICAL CHARACTERISTICS, *at an Ambient Temperature, T_A, of 25°C, and a DC Supply Voltage, V_{CC}, of +140 Volts applied to Terminal 14 through a resistance of 6.2 kΩ, unless otherwise indicated. Any other combination of DC Supply Voltage and Series Resistance which will not cause the Maximum Dissipation Limit or any of the Maximum Voltage or Current Limits for the CA3041 to be exceeded may be used.*

CHARACTERISTICS (See Page 7 for Definitions of Terms)	SYMBOLS	TEST CONDITIONS: SETUP AND PROCEDURE Fig.	TEST CONDITIONS: SPECIAL CONDITIONS	LIMITS: TYPE CA3041 Min.	Typ.	Max.	Units	TYPICAL CHARACTERISTICS CURVES Fig.
Total Device Dissipation	P_T	11	T_A = 0°C	220	245	270	mW	2
			T_A = +25°C	225	250	275	mW	
			T_A = +85°C	230	255	280	mW	
Zener Regulating Voltage (DC Supply Voltage at Terminal 14)	V_{14}	-		10.5	11.2	12.3	V	-
Quiescent Operating Current (into Terminal 11)	I_{11}	11		0.25	0.63	1	mA	-
9-Volt Current Drain (Quiescent Operating Current into Terminal 14)	I_{14}	11	V_{CC} = +9 V applied directly to Terminal 14	7	11	16	mA	-
Input-Impedance Components: Parallel Input Resistance	R_i	3	f = 4.5 MHz	-	11	-	kΩ	-
Parallel Input Capacitance	C_i	3		-	5	-	pF	-
Output-Impedance Components: Parallel Output Resistance	R_o	-		-	100	-	kΩ	-
Parallel Output Capacitance	C_o	-		-	4	-	pF	-
Input Limiting Voltage (Knee)	$V_{i(lim)}$	7		-	150	200	μV (rms)	4
Amplitude-Modulation Rejection	AMR	10		45	58	-	dB	9
IF-Amplifier Voltage Gain	$A_{(IF)}$	5		-	67	-	dB	4
Recovered AF Voltage: 1. At FM-Detector Output	V_o(af)	-	R_L = 50 kΩ, Δf = ±25 kHz THD = 0.7% (typ.)	-	250	-	mV (rms)	-
2. At AF-Driver Output in Test Setup		-	THD < 5%	8	9	-	V (rms)	-
Total Harmonic Distortion	THD	7	$V_{o(af)}$ = 8 V(rms)	-	1.5	5	%	-
Discriminator Output Resistance	$R_{o(dis)}$	-	f = 1 kHz	-	10	-	kΩ	-
AF-Amplifier Input Resistance	$R_{i(af)}$	-		-	100	-	kΩ	-
AF-Amplifier Output Resistance	$R_{o(af)}$	-		-	30	-	kΩ	-
AF-Driver Voltage Gain	A_{af}	6		-	41	-	dB	8

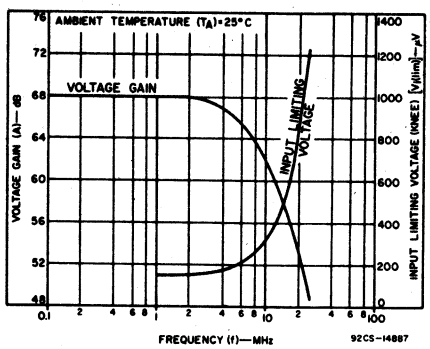
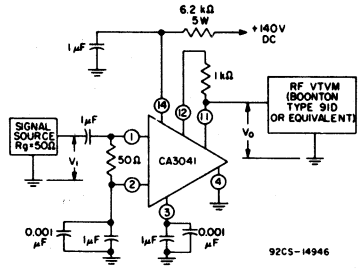


Fig.4 - Typical IF-amplifier voltage gain and input-limiting voltage (knee) characteristics.



PROCEDURE:

A - Voltage Gain:

1) Set input frequency at desired value, v_i = 100 μV rms.
2) Record v_o.
3) Calculate Voltage Gain A from A = 20 $\log_{10} v_o/v_i$
4) Repeat Steps 1, 2, and 3 for each frequency and/or for temperature desired.

Fig.5 - Test setup for measurement of IF-amplifier voltage gain.

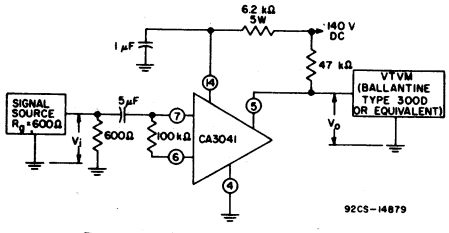
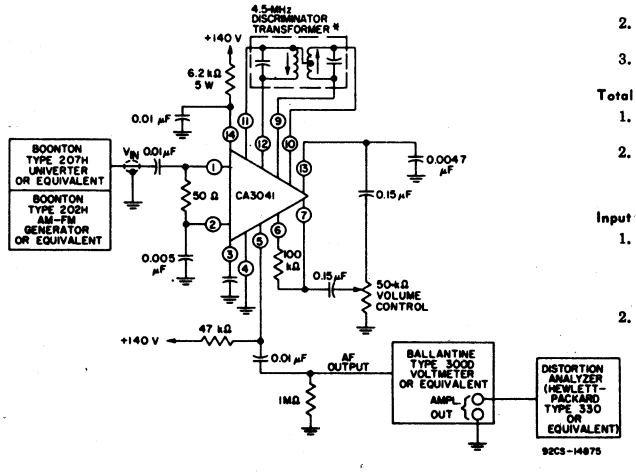


Fig.6 - Test setup for measurement of AF-amplifier voltage gain.



* TRW Electronics, Des Plaines, Illinois. Part No. EO23874, or equivalent.

Fig.7 - Test setup for measurement of input limiting voltage (Knee), recovered AF voltage, and total harmonic distortion.

PROCEDURES:

Recovered AF Voltage:

1. Set Input Signal Generator as follows:
   Output frequency = 4.5 MHz
   Modulating frequency = 1 kHz
   Deviation = ± 25 kHz
   Output level for V_{in} = 100 mV rms
2. Set volume control for maximum af output.
3. Measure af output voltage and record as Recovered AF Voltage.

Total Harmonic Distortion:

1. Adjust volume control for an af output voltage of 300 mV rms.
2. Measure Total Harmonic Distortion of the output signal in accordance with the Operating Instructions for the Distortion Analyzer.

Input Limiting Voltage (Knee):

1. Decrease V_{in} until the af output voltage is 3 dB less than the value set in Step 1 of the procedure for measurement of Total Harmonic Distortion (300 mV - 3 dB = 210 mV)
2. Measure resulting value of V_{in} and record as Input Limiting Voltage (Knee).

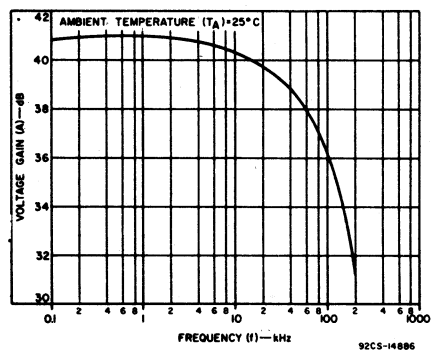


Fig.8 - Typical AF-driver voltage-gain characteristic

CA3041

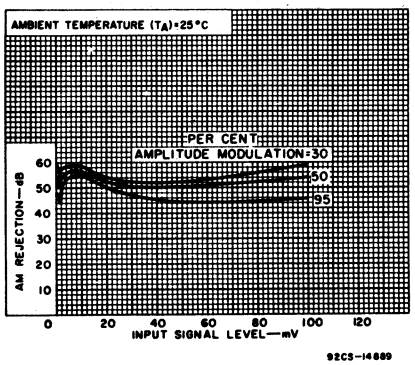
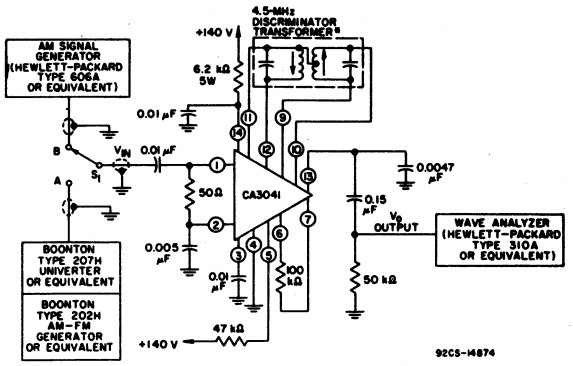


Fig.9 - Typical AM rejection characteristics for CA3041.

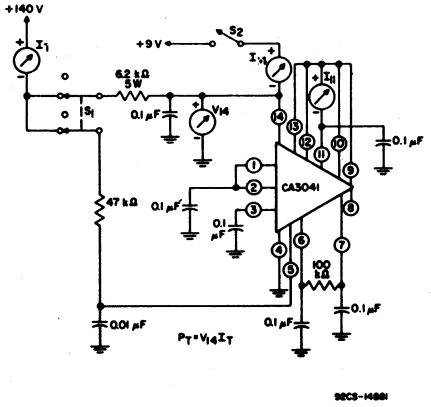


PROCEDURES:

1. Set FM Signal Generator as follows:
   Output frequency = 4.5 MHz
   Modulating frequency = 1000 Hz
   Deviation = ± 25 kHz
   Output level for V_{in} = 100 mV rms
2. Set AM Signal Generator as follows:
   Output frequency = 4.5 MHz
   Modulating frequency = 1000 Hz
   Per cent modulation = 30
   Output level for V_{in} = 10 mV rms
3. With S_1 in Position A measure AF Output Voltage and record as $V_{o(FM)}$.
4. With S_1 in Position B measure AF Output Voltage and record as $V_{o(AM)}$.
5. Determine AM Rejection from AMR = $V_{o(FM)}/V_{o(AM)}$

* TRW Electronics, Des Plaines, Illinois. Part No. EO23874, or equivalent.

Fig.10 - Test setup for measurement of AM rejection.



PROCEDURES:

Total Device Dissipation:

1. Close S_1, open S_2.
2. Measure and record V_{14} and I_T.
3. Determine Total Device Dissipation from $P_T = V_{14}I_T$.

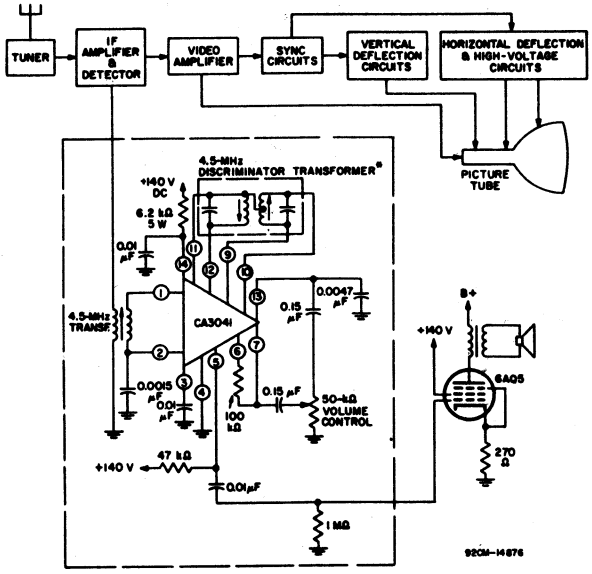
Quiescent Operating Current into Terminal 11:

1. Close S_1, open S_2.
2. Measure I_{11} and record as Quiescent Operating Current into Terminal 11.

9-Volt Current Drain:

1. Open S_1, close S_2.
2. Measure I_{14} and record as 9-Volt Current Drain.

Fig.11 - Test setup for total dissipation, quiescent operating current into terminal No.11, and 9-volt current drain.



* TRW Electronics, Des Plaines, Illinois. Part No. EO23874, or equivalent.

Fig.12 - Block diagram of typical TV receiver using CA3041.

CA3042

WIDE-BAND AMPLIFIER, FM DETECTOR AF PREAMPLIFIER/DRIVER

For Sound Sections of TV Receivers Using Transistor-Type AF Output Amplifiers

FEATURES

- high sensitivity – input limiting voltage (knee) = 150 μV typ. at 4.5 MHz
- 6-mA audio drive capability
- excellent AM rejection – 58 dB typ. at 4.5 MHz
- inherent high stability – internally shielded
- internally Zener-diode-regulated voltage supply
- low harmonic radiation
- wide frequency capability – <100 kHz to >20 MHz
- low harmonic distortion

RCA Integrated Circuit Type CA3042 provides, in a single monolithic silicon chip, a major sub-system for the sound sections of TV receivers. As shown in the Schematic Diagram (Fig.1) and the TV Receiver Block Diagrams (Figs.2A and 2B) the CA3042 contains a multistage wide-band if-amplifier section, an FM-detector stage, a Zener-diode-regulated power-supply section, and an af-amplifier section specifically designed to drive directly an n-p-n audio output transistor or a high-gain audio output pentode tube.

In FM receivers, the CA3042 can be used to provide if amplification and limiting, FM detection, and af preamplification.

The CA3042 provides exceptional versatility of circuit design because the if-amplifier/limiter section, FM detector section, and af-preamplifier/driver section can be used independently of each other.

The CA3042 utilizes a 14-lead dual-in-line plastic package with leads specially formed to facilitate automatic insertion of the device in suitably punched printed-circuit boards.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

OPERATING-TEMPERATURE RANGE	−40° to +85°C
STORAGE-TEMPERATURE RANGE	−65° to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C
MAXIMUM INPUT-SIGNAL VOLTAGE:	
Between Terminals 1 and 3	±3 V
MAXIMUM DEVICE DISSIPATION:	
At Ambient Temperatures up to +25°C	950 mW
At Ambient Temperatures above +25°C	Derate at 10.8 mW/°C

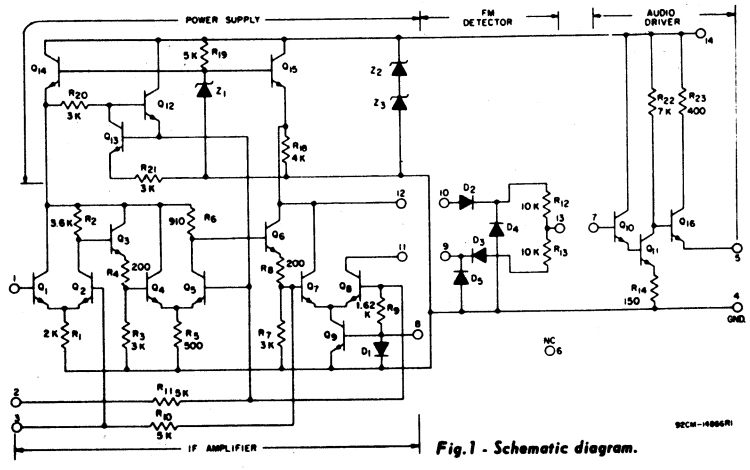


Fig.1 - Schematic diagram.

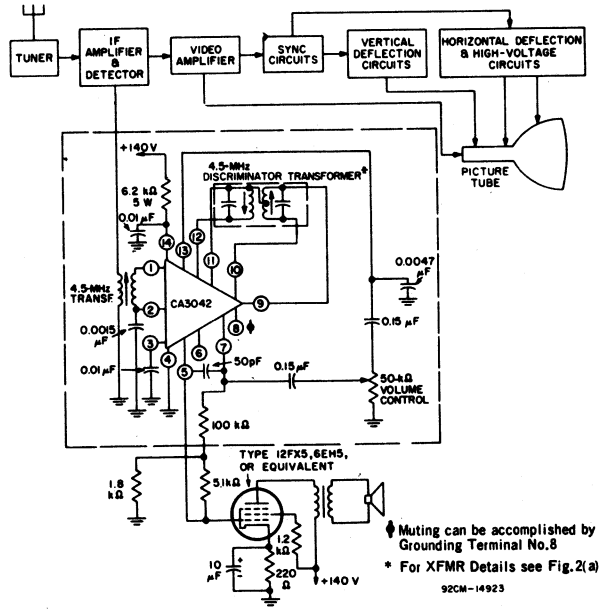


Fig.2(b) - Block diagram of typical TV receiver utilizing the CA3042 and a 12FX5, 6EH5, or equivalent.

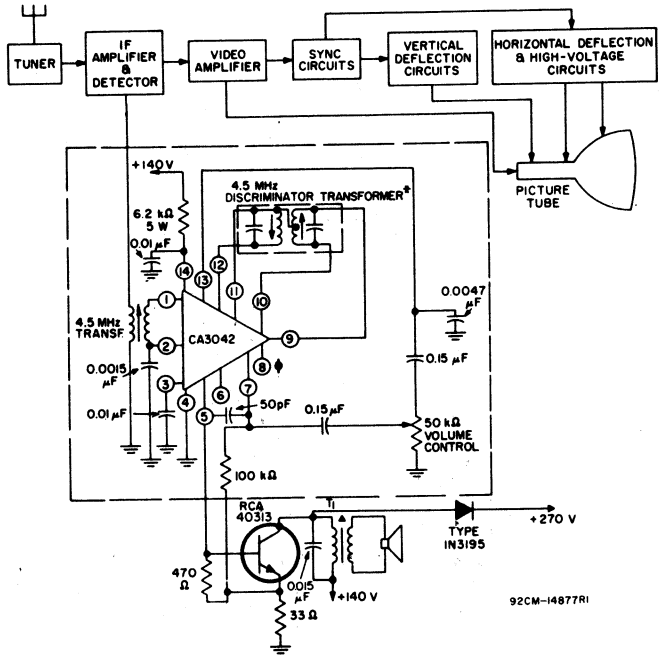
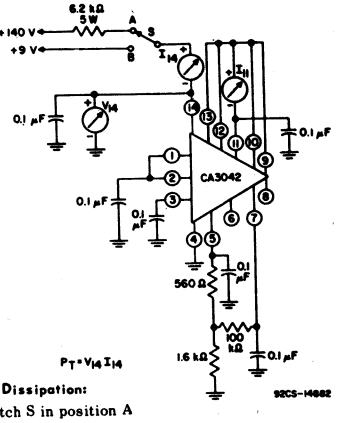


Fig. 2(a) - Block diagram of typical TV receiver utilizing transistor RCA-40313.



PROCEDURES: $P_T = V_{14} I_{14}$

Total Device Dissipation:

1. Set switch S in position A
2. Measure and record V_{14} and I_{14}.
3. Determine Total Device Dissipation from $P_T = V_{14} I_{14}$

Quiescent Operating Current into Terminal 11:

1. Turn switch S to position B
2. Measure I_{11} and record as Quiescent Operating Current into Terminal 11.

9-Volt Current Drain:

1. Set switch S in position B
2. Measure I_{14} and record as 9-Volt Current Drain.

Fig.3 - Test setup for measurement of total device dissipation, quiescent current into terminal No.11, and 9-volt current drain.

CA3042

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS AT T_A = 25°C

Indicated voltage or current limits for each terminal may be applied under the specified voltage conditions for other terminals. All voltages are with respect to ground (Terminal 4).

TERMINAL	VOLTAGE OR CURRENT LIMITS		VOLTAGE CONDITIONS AT OTHER TERMINALS													
			1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	-3 V	+3 V	–	AT SAME DC VOLTAGE AS TERMINAL 1	EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL	GROUND (VOLTAGE REFERENCE TERMINAL)	AF-DRIVER OUTPUT TERMINAL (EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL)	NO CONNECTION	AF-INPUT TERMINAL (EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL)	MUTING TERMINAL (EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL EXCEPT THAT TERMINAL MAY BE GROUNDED TO OBTAIN MUTING ACTION)	AT SAME DC VOLTAGE AS TERMINAL 12 (EXCEPT TERMINAL 9)	AT SAME DC VOLTAGE AS TERMINAL 12 (EXCEPT TERMINAL 10)	AT SAME DC VOLTAGE AS TERMINAL 12 (EXCEPT TERMINAL 11)	EXTERNAL DC VOLTAGE IS NOT NORMALLY APPLIED TO THIS TERMINAL	AT SAME DC VOLTAGE AT TERMINAL 12 (EXCEPT TERMINAL 13)	CONNECTED TO +140 V DC THROUGH 6.2-kΩ RESISTOR*
2	-3 V	+3 V	-3 to +3													
3	-3 V	+3 V	-3 to +3													
4	GROUND (VOLTAGE REFERENCE TERMINAL)		-3 to +3													
5	20 mA		-3 to +3													
6	NO CONNECTION		-3 to +3													
7	10 mA		-3 to +3													
8	10 mA		-3 to +3													
9	10 mA		-3 to +3													
10	10 mA		-3 to +3													
11	+2 V	+10 V	-3 to +3													
12	+2.5 V	+10 V	-3 to +3													
13	0 V	+10 V	-3 to +3													
14	50 mA		-3 to +3													

* Any other combination of DC Supply Voltage and Series Resistance which will not cause the Maximum Device Dissipation Limit or any of the Maximum Voltage or Current Limits for the CA3042 to be exceeded may be used.

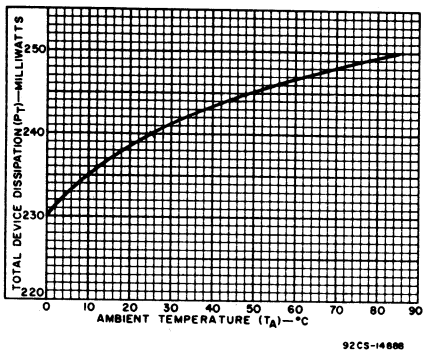


Fig.4 - Typical dissipation characteristic.

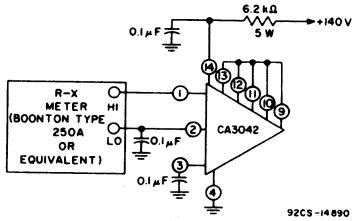
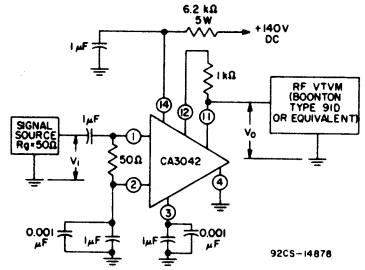


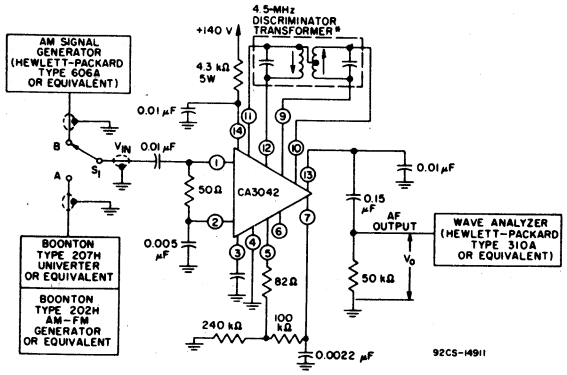
Fig.5 - Test setup for measurement of input-impedance components.



PROCEDURE Voltage Gain:

1. Set input frequency at desired value, v_i = 100 μV rms.
2. Record v_o.
3. Calculate Voltage Gain A from A = 20 $\log_{10} v_o/v_i$.
4. Repeat Steps 1, 2, and 3 for each frequency and/or for temperature desired.

Fig.6 - Test setup for measurement of IF amplifier voltage gain.



PROCEDURES:

1. Set FM Signal Generator as follows:
   Output Frequency = 4.5 MHz
   Modulating frequency = 1000 Hz
   Deviation = ±25 kHz
   Output level for V_{in} = 100 mV rms
2. Set AM Signal Generator as follows:
   Output frequency = 4.5 MHz
   Modulating frequency = 1000 Hz
   Per cent modulation = 30
   Output level for V_{in} = 10 mV rms
3. With S_1 in Position A measure AF Output Voltage and record as $V_{o(FM)}$.
4. With S_1 in Position B measure AF Output Voltage and record as $V_{o(AM)}$.
5. Determine AM Rejection from AMR = $\frac{V_{o(FM)}}{V_{o(AM)}}$

* TRW Electronics, Des Plaines, Illinois. Part No. EO23874, or equivalent.

Fig.7 - Test setup for measurement of AM rejection.

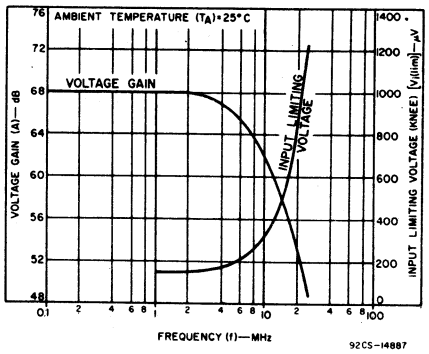


Fig.8 - Typical IF amplifier voltage gain and input limiting voltage (knee) characteristics.

CA3042

ELECTRICAL CHARACTERISTICS, *at an Ambient Temperature, T_A, of 25°C, and a DC Supply Voltage, V_{CC}, of +140 Volts applied to Terminal 14 through a resistance of 6.2 kΩ, unless otherwise indicated. Any other combination of DC Supply Voltage and Series Resistance which will not cause the Maximum Dissipation Limit or any of the Maximum Voltage or Current Limits for the CA3042 to be exceeded may be used.*

CHARACTERISTICS (See Page 7 for Definitions of Terms)	SYMBOLS	TEST CONDITIONS: SETUP AND PROCEDURE Fig.	TEST CONDITIONS: SPECIAL CONDITIONS	LIMITS: TYPE CA3042 Min.	Typ.	Max.	Units	TYPICAL CHARACTERISTICS CURVES Fig.
Total Device Dissipation	P_T	3	T_A = 0°C	200	230	260	mW	4
			T_A = +25°C	210	240	270	mW	
			T_A = +85°C	220	250	280	mW	
Zener Regulating Voltage (DC Supply Voltage at Terminal 14)	V_{14}	–		10.5	11.2	12.3	V	–
Quiescent Operating Current (into Terminal 11)	I_{11}	3		0.25	0.63	1	mA	–
9-Volt Current Drain (Quiescent Operating Current into Terminal 14)	I_{14}	3	V_{CC} = +9 V applied directly to Terminal 14	8	12	18	mA	–
Input-Impedance Components: Parallel Input Resistance	R_I	5	f = 4.5 MHz	–	11	–	kΩ	–
Parallel Input Capacitance	C_I	5	f = 4.5 MHz	–	5	–	pF	–
Output-Impedance Components: Parallel Output Resistance	R_O	–	f = 4.5 MHz	–	100	–	kΩ	–
Parallel Output Capacitance	C_O	–	f = 4.5 MHz	–	4	–	pF	–
Input Limiting Voltage (Knee)	$V_{I(lim)}$	11	f = 4.5 MHz	–	150	200	μV (rms)	8
Amplitude-Modulation Rejection	AMR	7	f = 4.5 MHz	45	58	–	dB	
IF-Amplifier Voltage Gain	$A_{(IF)}$	6	f = 4.5 MHz	–	67	–	dB	8
Recovered AF Voltage: 1. At FM-Detector Output	$V_{O(af)}$	11	f = 4.5 MHz, Δf = ±25 kHz, R_L = 50 kΩ THD = 0.7% (typ.)	–	250	–	mV (rms)	–
2. At AF-Driver Output in Test Setup		11	f = 4.5 MHz, Δf = ±25 kHz, R_L = 322 Ω THD < 5%	500	800	–	mV (rms)	–
3. At AF-Driver Output in TV-Receiver Sound System		2A or 2B	f = 4.5 MHz, Δf = ±25 kHz, R_L = 150 kΩ THD = 1.5% (typ.)	–	3	–	V (rms)	–
Total Harmonic Distortion: 1. In Test Setup	THD	11	f = 4.5 MHz, Δf = ±25 kHz, $V_{O(af)}$ = 500 mV (rms)	–	1.5	5	%	–
2. In TV Receiver Sound System		2A or 2B	f = 4.5 MHz, Δf = ±25 kHz, $V_{O(af)}$ = 1.3 V (rms)	–	1	–	%	–
FM-Detector Output Resistance	$R_{O(det)}$	–	f = 1 kHz	–	10	–	kΩ	–
AF-Driver Input Resistance	$R_{I(af)}$	–	f = 1 kHz	–	100	–	kΩ	–
AF-Driver Output Resistance	$R_{O(af)}$	–	f = 1 kHz	–	250	–	Ω	–
AF-Driver Voltage Gain	A_{af}	9	f = 1 kHz, R_S = 50 Ω, C_1 = 0	–	30	–	dB	10

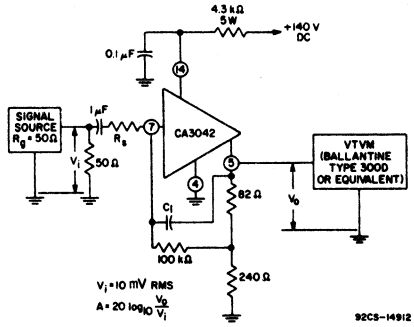


Fig.9 - Test setup for measurement of AF amplifier voltage gain.

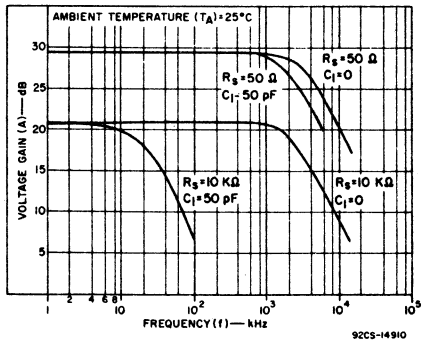
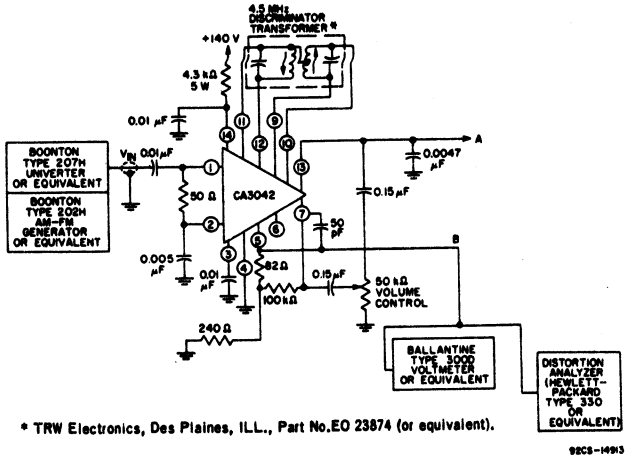


Fig.10 - Typical AF amplifier voltage gain characteristics.



* TRW Electronics, Des Plaines, ILL., Part No.EO 23874 (or equivalent).

PROCEDURES:

Recovered AF Voltage:

1. Set Input Signal Generator as follows:
   - Output frequency = 4.5 MHz
   - Modulating frequency = 1 kHz
   - Deviation = ±25 kHz
   - Output level for V_{in} = 100 mV rms
2. Set volume control for maximum af output
3. Measure af output voltage and record as Recovered AF Voltage.

Total Harmonic Distortion:

1. Adjust volume control for an af output voltage of 500 mV rms.
2. Measure Total Harmonic Distortion of the output signal in accordance with the Operating Instructions for the Distortion Analyzer.

Input Limiting Voltage (Knee):

1. Decrease V_{in} until the af output voltage is 3 dB less than the value set in Step 1 of the procedure for measurement of Total Harmonic Distortion (500mV - 3 dB = 350 mV)
2. Measure resulting value of V_{in} and record as Input Limiting Voltage (Knee).

Fig.11 - Test setup for measurement of input limiting voltage (knee), recovered AF voltage, and total harmonic distortion.

CA3043

Special-Function Sub-System

HIGH-GAIN IF AMPLIFIER, LIMITER, FM DETECTOR, AND AF PREAMPLIFIER/DRIVER

For FM IF Amplifier Applications in Communications Receivers and High-Fidelity FM Receivers up to 20 MHz

FEATURES

- high sensitivity - - input limiting voltage (knee) 50 μV typ. at 10.7 MHz
- excellent AM rejection - - 58 dB typ. at 10.7 MHz
- inherent high stability - - internally shielded
- internal Zener-diode regulated voltage supply
- low harmonic radiation
- wide frequency capability - - <100 kHz to >20 MHz
- low harmonic distortion
- hermetic 12-lead TO-5 style package

RCA Integrated Circuit Type CA3043 provides in a single monolithic silicon chip, a major sub-system for the IF sections of Communications and high-fidelity FM receivers. As shown in the Schematic Diagram (Fig.2) and the FM Receiver Block Diagram (Fig.1), the CA3043 contains a multistage if-amplifier/limiter section, an FM-detector stage, a Zener-diode regulated power-supply section, and an af-amplifier section. In FM receivers, the CA3043 can be used to provide if amplification and limiting, FM detection, and af preamplification. The CA3043 provides exceptional versatility of circuit design because the if-amplifier/limiter section, FM detector section, and af-preamplifier/driver section can be used independently of each other.

The four stage emitter-follower-coupled if amplifier section provides 80-dB voltage gain at 10.7 MHz, and features an output stage with exceptionally good limiting characteristics because of its transistor constant-current sink.

The FM detector section is distinguished by circuitry which provides forward bias to the detector diodes, D2 and D3, and also provides a reference voltage for AFC.

The audio amplifier provides a low-impedance drive for subsequent audio amplifiers.

The power supply section provides zener-regulated, decoupled voltages for the IF amplifier, detector, and audio amplifier sections.

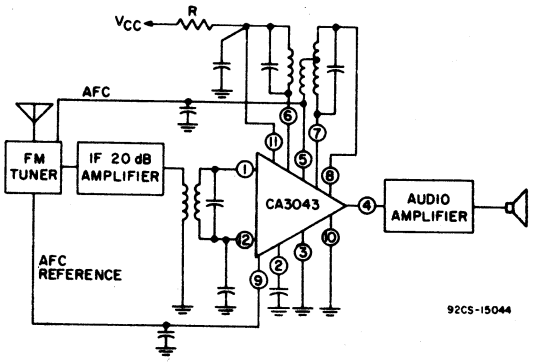


Fig.1 - Typical application of the CA3043 as a high-gain limiter, amplifier-detector in an FM receiver.

ABSOLUTE-MAXIMUM RATINGS at T_A = 25°C

DISSIPATION:
At T_A = 25°C to T_A = 85°C . . . . . 450 mW
Above T_A = 85°C . . . . . Derate linearly 5 mW/°C

LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 min) from case for 10 seconds max . . . . . + 265°C

TEMPERATURE RANGE:
Operating . . . . . -55°C to + 125°C
Storage . . . . . -65°C to + 150°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	TEST CIRCUIT AND PROCEDURE	LIMITS TYPE CA3043			UNITS
			Fig.	Min.	Typ.	Max.	
STATIC CHARACTERISTICS							
Current Drain at 6V into Pin No.11	I_{11}	V_{CC} = +6V	3	10	16	20	mA
Regulator Voltage Pin No.11	V_{11}	V_{CC} = +30V, R_S = 750 Ω	3	6.9	7.4	8	V
Total Device Dissipation	P_T		3	200	225	260	mW
Quiescent Operating Current into Pin No.6	I_6		3	-	0.65	-	mA
DYNAMIC CHARACTERISTICS at V_{CC} = +30V, R_S = 750 Ω, f = 10.7 MHz							
Voltage Gain	A_v		4	72	80	-	dB
Input Limiting Voltage (knee)	v_i(lim)	v_o(af) at -3 dB point	6	-	50	-	μV (RMS)
Limiting Current from Pin No.6	I_6(lim)		4	-	0.42	-	mA (RMS)
Recovered AF Voltage	v_o(af)	v_i = 1 mV (RMS), f (modulating) = 1 kHz, Deviation = ± 75 kHz	6	75	110	150	mV (RMS)
Amplitude-Modulation Rejection	AMR	v_i = 10 mV, f (modulating) = 1 kHz, % modulation = 50%	8	-	58	-	dB
Total Harmonic Distortion	THD	v_i = 1 mV (RMS)	6	-	0.3	-	%
Input Impedance Components:							
Parallel Input Resistance	R_I		-	-	7	-	kΩ
Parallel Input Capacitance	C_I		-	-	5	-	pF

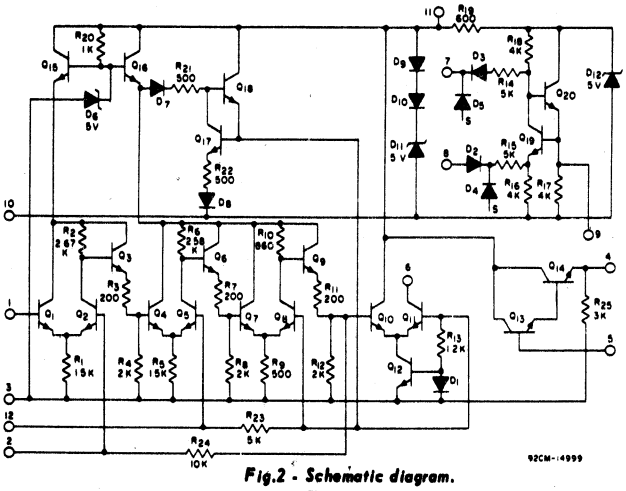
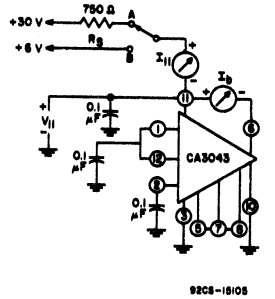


Fig.2 - Schematic diagram.

Notes:
S = Substrate
Terminal No.3 wire-connected to the case.
Terminal No.10 connected to the case through the substrate
Terminals No.3 and 10 which are connected to the substrate should be connected to the most negative point in the circuit.
Diodes D_4 and D_5, act as capacitors and are used to balance the detector substrate capacitances.



Switch in Position A for:
Regulator-Voltage, Quiescent-Operating-Current, and Device Dissipation Test
Switch in Position B for Current into Pin No.11

Fig.3 - Regulator voltage, device dissipation, quiescent operating current, and current at 6 volts into Pin No. 11.

CA3043

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range between horizontal terminal 5 and vertical terminal 3 is +6 to 0 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12
1		+4 -4	0 -5	*	*	*	*	*	*	0 -5	*	Note(1)
2			0 -3	*	*	*	*	*	*	0 -3	*	*
3				+6 0	+6 0	+15 +2	+6 0	+6 0	+6 0	0	Note(2)	+3 0
4					+2 -4	*	*	*	*	0 -6	*	*
5						*	*	*	*	0 -6	+6 0	*
6							*	*	*	-2 -15	*	*
7								Note(1)	*	0 -6	*	*
8									*	0 -6	*	*
9										0 -6	*	*
10											Note(2) 0	+3 0
11												*
12												

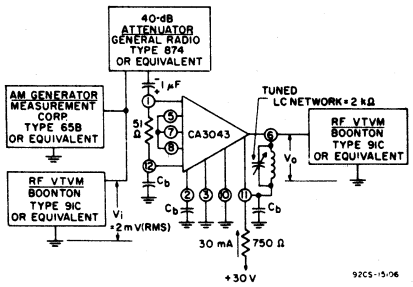
MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	-	-
2	-	-
3	0.1	40
4	-	20
5	-	-
6	-	-
7	-	-
8	-	-
9	-	20
10	0.1	40
11	40	0.1
12	-	-

Note 1: These terminals should be connected through a dc resistance to any terminal which does not exceed 100 ohms.

Note 2: Pin 11 may be connected to any positive voltage source through a suitable resistor provided its current rating is not exceeded.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.



Voltage Gain = $20 \log_{10} 100 \frac{V_o}{V_i}$

C_b - Bypass Capacitor, 0.1 μF electrolytic in parallel with 0.01 μF

$I_6(lim) = \frac{V_o}{2K\Omega}$, V_i = 100 mV(RMS)

* Output circuit should be completely shielded from the input circuit at the socket.

Fig.4 - Voltage gain test circuit.

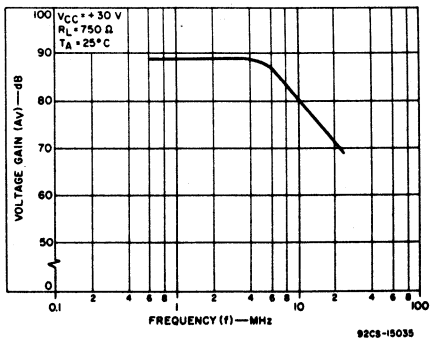
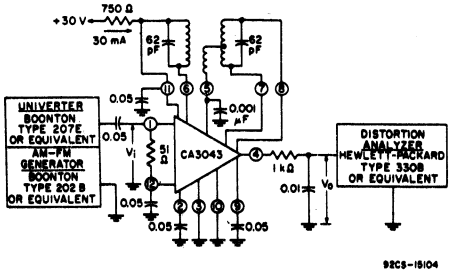


Fig.5 - Voltage gain vs frequency.



PROCEDURE:

1. Recovered Audio Voltage $v_{o(af)}$ –
   Set input frequency to 10.7 MHz,
   v_i = 1 mV(RMS), modulating frequency = 1 kHz
   Deviation = ±75 kHz
   Record v_o as measured on the Distortion Analyzer meter scale.
   This is the recovered Audio Voltage $v_{o(af)}$
2. 3 dB Limiting Sensitivity $v_{i(lim)}$ –
   Reduce v_i until $v_{o(af)}$ drops 3 dB.
   Record this value of v_i as $v_{i(lim)}$
3. Total Harmonic Distortion THD –
   Reset v_i to 1 mV(RMS) and operate Distortion Analyzer per manufacturer's instructions to measure THD.

* See Fig.9 for details on Discriminator Transformer.

Fig.6 - Input limiting voltage (knee), recovered AF voltage, and total harmonic distortion test circuit.

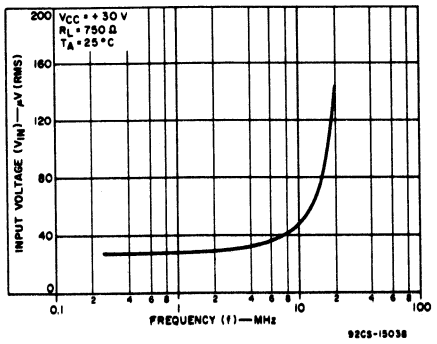
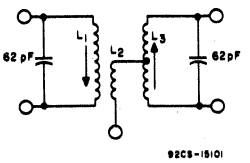
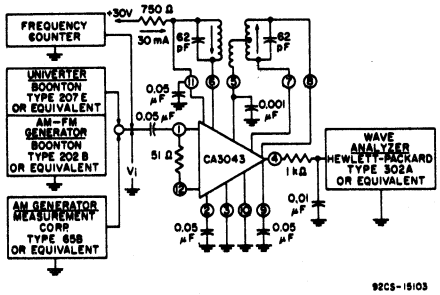


Fig.7 - Input limiting voltage (knee) at -3 dB point vs frequency.



Coil Form, Outside Diameter = 7/32"
Can = 1/2" square X 1-1/8" long
Slugs - Radio Industries Type MP34/MP100 Material
L_1 & L_3 = 20 Turns 5-44 litz wire universal wound
L_2 = 10 Turns 5-44 litz wire wound bifilar with L_1
L_1 & L_3 coupling adjusted to 520 kHz peak to peak separation on S curve when operated in circuit shown in Fig.6.

Fig.9 - 10.7-MHz discriminator transformer for CA3043.



PROCEDURE:

A. Connect FM Generator to CA3043 input.
   Set frequency to 10.7 MHz, v_i = 10 mV, modulating frequency = 1 kHz
   Deviation = ±75 kHz.
   Tune Wave Analyzer to peak reading at 1 kHz and record recovered Audio Voltage $v_{o(af)FM}$.

B. Disconnect FM Generator and Connect AM Generator to CA3043 input.
   Set frequency to 10.7 MHz, v_i = 10 mV, modulating frequency = 1 kHz, percent modulation = 50%.
   Tune Wave Analyzer to peak reading and record recovered audio voltage $v_{o(af)AM}$
   Amplitude Modulation Rejection Ratio = $20 \log_{10} \frac{v_{o(af)FM}}{v_{o(af)AM}}$

Fig.8 - Amplitude modulation rejection test circuit.

CA3044, CA3044V1

Special-Function Sub-System

WIDE-BAND AMPLIFIER/PHASE DETECTOR WITH ZENER DIODE VOLTAGE REGULATOR

For AFC (Automatic Frequency Control) Applications

The RCA CA3044 and CA3044V1 represent a second generation of integrated circuits designed primarily for AFC (Automatic-Frequency-Control) applications.

The CA3044V1 is electrically identical to the CA3044 but is supplied with formed leads for easier PC board design and construction.

FEATURES

- Primarily intended for AFC (automatic frequency control) Applications
- Internal Zener Diode Voltage Regulator
- Differential Input Amplifier/Limiter
- Full-Wave Diode Bridge Detector
- Differential Output Voltage Amplifier
- Available in Two Electrically Identical Versions of the 10-lead TO-5 style package,

  CA3044 With Straight Leads;

  CA3044V1 With Formed Leads
- Wide Operating Temperature Range; -55 to +125°C

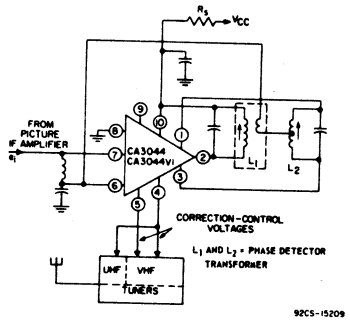


Fig.1 - Block diagram of Typical Automatic Fine Tuning (AFT) Application using CA3044 or CA3044V1 in Color-TV Receiver.

ABSOLUTE-MAXIMUM RATINGS

DISSIPATION:
- At T_A = 25°C ..... 830 mW
- Above T_A = 25°C ..... Derate linearly 5.6 mW/°C

TEMPERATURE RANGE:
- Operating ..... -55°C to +125°C
- Storage ..... -65°C to +150°C

LEAD TEMPERATURE (During Soldering):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. ..... +265C

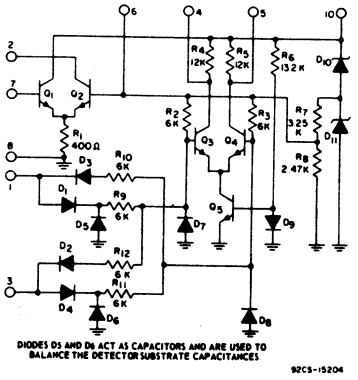


Fig.2 - Schematic diagram CA3044, CA3044V1

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 6 is +20 to 0 volts.

TERMINAL No.	9	10	1	2	3	4	5	6	7	8
9	NO INTERNAL CONNECTION									-
10			+20 0	+20 -10	+20 0	+20 0	+20 0	+20 0	+20 0	▲
1				*	+12 -12	*	*	+6 -6	*	+6 0
2					*	*	*	+20 0	*	+20 0
3						*	*	+6 -6	*	+6 0
4							*	*	*	+12 0
5								*	*	+12 0
6									+5 -5	+5 0
7										+8 -5
8										REF. SUB-STRATE

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
9	-	-
10	50	50
1	5	5
2	20	20
3	5	5
4	5	5
5	5	5
6	5	5
7	5	5
8	50	50

▲ Terminal No. 10 may be connected to any positive voltage source through a suitable dropping resistor—provided the dissipation rating is not exceeded.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

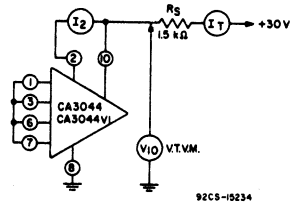


Fig.3 - Test setup: Measurement of total device dissipation, Zener regulating voltage, quiescent operating current (terminal 2).

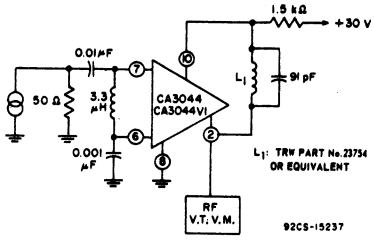


Fig.4 - Input limiting sensitivity test circuit.

CA3044, CA3044V1

ELECTRICAL CHARACTERISTICS at T_A = 25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CIRCUITS FIG.	TEST CONDITIONS	LIMITS CA3044 and CA3044V1 MIN.	TYP.	MAX.	UNITS	CHARACTERISTIC CURVES FIG.
STATIC CHARACTERISTICS								
Device Dissipation	P_T	3	V_{CC} = 30 V, R_S = 1.5 kΩ, T_A = -55°C	90	120	150	mW	-
Device Dissipation	P_T	3	V_{CC} = 30 V, R_S = 1.5 kΩ, T_A = 25°C	110	140	170	mW	-
Device Dissipation	P_T	3	V_{CC} = 30 V, R_S = 1.5 kΩ, T_A = +125°C	130	160	190	mW	-
9-Volt Current Drain	I_T	3	V_{10} = 9 V	2.5	4	5.5	mA	-
Zener Regulating Voltage - DC Supply Voltage at Terminal 10	V_{10}	3	V_{CC} = 30 V, R_S = 1.5 kΩ	10.5	11.2	11.9	V	-
Quiescent Operating Current into Terminal 2	I_2	3		1	2	4	mA	-
Quiescent Operating Voltage at Terminal 4	V_4	-		5.0	6.5	8.0	V	-
Quiescent Operating Voltage at Terminal 5	V_5	-		5.0	6.5	8.0	V	-
Output Offset Voltage between Terminals 4 and 5	V_{4-5}	-		-1.5	0	1.5	V	-
DYNAMIC CHARACTERISTICS (AS RF AMPLIFIER)								
Input Limiting Voltage (Knee)	V_i Limiting	4	f=45.75 MHz	-	75	-	mV	-
Input Admittance	y_{11}	-	f = 45.75 MHz, V_{CC} = 30 V, R_S = 1.5 kΩ	-	0.5+j1.1	-	mmho	-
Reverse Transfer Admittance	y_{12}	-		-	3.8+j3.4	-	μmho	-
Forward Transfer Admittance	y_{21}	-		-	-11.7 +10.1	-	mmho	-
Output Admittance	y_{22}	-		-	0.077+j0.9	-	mmho	-
OUTPUT vs FREQUENCY DEVIATION - AFC								
Correction-Control Voltage at Terminal 4	V corr. (4)	5	V_{CC} = +30 V, V_{in} = 200 mV RMS, f_0 = MHz as indicated	% of V_{10}		% of V_{10}		
			45.750 - 0.025	85	-	-	V	6,7
			45.750 + 0.025	-	-	33	V	
			45.750 - 0.900	75	-	-	V	7
			45.750 + 0.900	-	-	43	V	
			45.750 - 1.500	-	-	85	V	
			45.750 + 1.500	33	-	-	V	
Correction-Control Voltage at Terminal 5	V corr. (5)	5	45.750 - 0.025	-	-	33	V	6,7
			45.750 + 0.025	85	-	-	V	
			45.750 - 0.900	-	-	43	V	7
			45.750 + 0.900	75	-	-	V	
			45.750 - 1.500	33	-	-	V	
			45.750 + 1.500	-	-	85	V	

DYNAMIC CONTROL VOLTAGE CHARACTERISTICS

The CA3044 and CA3044VI are specifically intended for use in the AFT system of color television receivers. Each device is tested so that the control voltages generated by the circuit meet the critical requirements of the system. Figure 5 is the schematic diagram of the test circuit.

Figure 6 and 7 show the control voltages generated at terminals 4 and 5 of the Integrated Circuit as a function of the frequency deviation from the nominal center frequency. Figure 6 shows the region within 25 KHz of the center frequency while Figure 7 covers the entire bandwidth of the system. The horizontal reference lines on the figures are generated by a voltage divider connected between the power supply voltage on Terminal 10 and ground. The dynamic control voltages are compared with these references according to the Output vs Frequency Deviation Table. For example: when the frequency deviation is -25 KHz the control voltage at Terminal 4 is greater than the reference A voltage; the control voltage at Terminal 5 is less than the reference B voltage.

The shape of the correction voltage characteristics is dependent to a large degree upon transformer characteristics and the parts layout. In order to closely duplicate the curves shown, the printed circuit board shown in Figure 8 and the parts layout shown in Figure 9 should be followed as closely as possible.

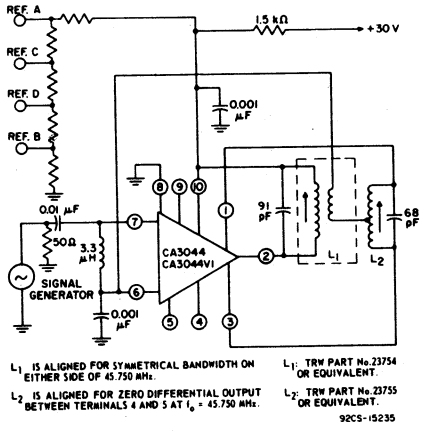


Fig.5 - Correction voltage test circuit for CA3044 and CA3044VI.

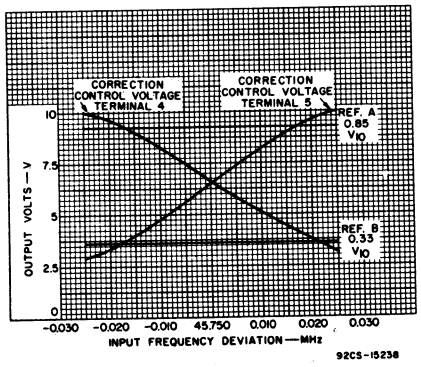


Fig.6 - Typical narrow-band dynamic control voltage characteristics.

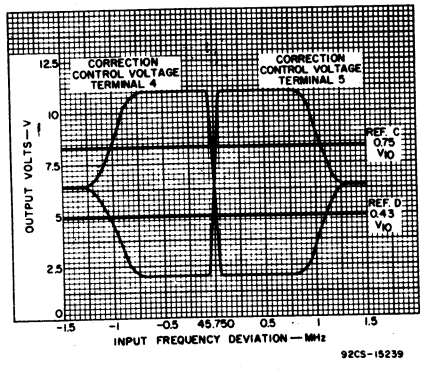


Fig.7 - Typical wide-band dynamic control voltage characteristics.

DEFINITIONS OF TERMS

Input Limiting Voltage (Knee) [v_i(lim)]
The input signal voltage which will cause the output signal to decrease 3 dB from its maximum level.

Total Device Dissipation (P_T)
The total power drain of the device with no signal applied and no external load current.

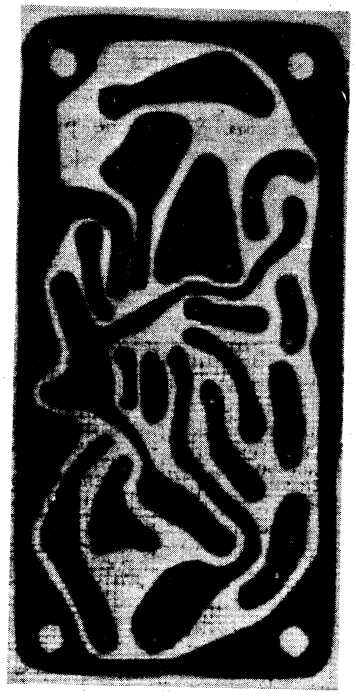
Quiescent Operating Voltage
The dc voltage at the output terminal, with respect to ground, with no signal applied.

Quiescent Operating Current
The average (dc) value of the current in either output, terminal, with no signal applied.

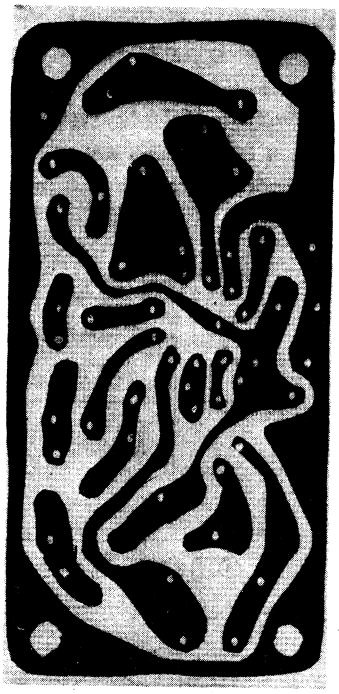
Output Offset Voltage
The dc voltage between output terminals with no signal applied.

Control Voltage
The dc voltage at either output terminal with respect to ground with an RF signal of specified frequency applied.

CA3044, CA3044V1



a) Top view



b) Bottom view

Fig.8 - Printed Circuit Board for Test Circuit -- Full Size

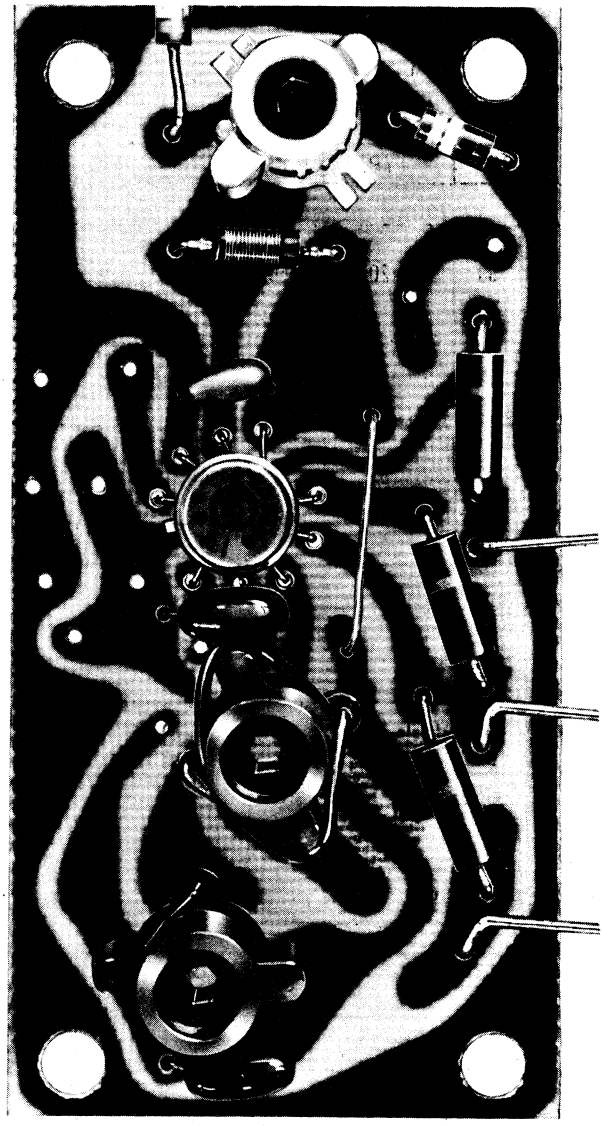


Fig.9 - Top view of wired test board.

CA3045, CA3046 Types

General-Purpose Transistor Arrays For Low-Power Applications at Frequencies from DC through the VHF Range

THREE ISOLATED TRANSISTORS AND ONE DIFFERENTIALLY-CONNECTED TRANSISTOR PAIR

The CA3045 and CA3046 each consist of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair.

The transistors of the CA3045 and CA3046 are well suited to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits. However, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching.

The CA3045 is supplied in a 14-lead dual-in-line hermetic (welded-seal) ceramic package and the CA3045F in a 14-lead dual-in-line hermetic (frit-seal) ceramic package.

The CA3046 is electrically identical to the CA3045 but is supplied in a dual-in-line plastic package for applications requiring only a limited temperature range.

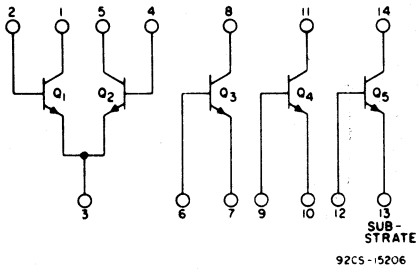


Fig.1 - Schematic diagram.

ABSOLUTE MAXIMUM RATINGS AT T_A = 25°C

	CA3045		CA3045F, CA3046		
	Each Transistor	Total Package	Each Transistor	Total Package	
Power Dissipation:					
T_A up to 55°C	–	–	300	750	mW
T_A > 55°C	–	–	Derate at 6.67		mW/°C
T_A up to 75°C	300	750	–	–	mW
T_A > 75°C	Derate at 8		–	–	mW/°C
Collector-to-Emitter Voltage, V_{CEO}	15	–	15	–	V
Collector-to-Base Voltage, V_{CBO}	20	–	20	–	V
Collector-to-Substrate Voltage, V_{CIO}*	20	–	20	–	V
Emitter-to-Base Voltage, V_{EBO}	5	–	5	–	V
Temperature Range:					
Operating	–55 to +125		–55 to +125		°C
Storage	–65 to +150		–65 to +150		°C
Lead Temperature (During Soldering):					
At distance 1/16 ±1/32" (1.59 ±0.79 mm) from case for 10 seconds max:	+265		+265		°C

* The collector of each transistor of the CA3045 and CA3046 is isolated from the substrate by an integral diode. *The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

Characteristics apply for each transistor in the CA3045 and CA3046 as specified.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS Type CA3045 Type CA3046 MIN.	TYP.	MAX.	UNITS
STATIC CHARACTERISTICS						
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	20	60	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	15	24	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	5	7	-	V
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	-	0.002	40	nA
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10 V, I_B = 0	-	See curve	0.5	μA
Static Forward Current-Transfer Ratio (Static Beta)	h_{FE}	V_{CE} = 3 V, I_C = 10 mA	-	100	-	-
		V_{CE} = 3 V, I_C = 1 mA	40	100	-	-
		V_{CE} = 3 V, I_C = 10 μA	-	54	-	-
Input Offset Current for Matched Pair Q_1 and Q_2: $\lvert I_{IO_1} - I_{IO_2} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.3	2	μA
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_E = 1 mA	-	0.715	-	V
		V_{CE} = 3 V, I_E = 10 mA	-	0.800	-	
Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE_1} - V_{BE_2} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.45	5	mV
Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE_3} - V_{BE_4} \rvert$, $\lvert V_{BE_4} - V_{BE_5} \rvert$, $\lvert V_{BE_5} - V_{BE_3} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.45	5	mV
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA	-	-1.9	-	mV/°C
Collector-to-Emitter Saturation Voltage	V_{CES}	I_B = 1 mA, I_C = 10 mA	-	0.23	-	V
Temperature Coefficient: Magnitude of Input-Offset Voltage	$\frac{\lvert \Delta V_{10} \rvert}{\Delta T}$	V_{CE} 3 V, I_C 1 mA	-	1.1	-	μV/°C

FEATURES

- Two matched pairs of transistors
  V_{BE} matched ±5 mV
  Input offset current 2 μA max. at I_C = 1 mA
- 5 general purpose monolithic transistors
- Operation from DC to 120 MHz
- Wide operating current range
- Low noise figure - - 3.2 dB typ. at 1 kHz
- Full military temperature range for CA3045
  -55 to +125°C
- The CA3045 is available in a sealed-junction Beam-Lead version (CA3045L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".

APPLICATIONS

- General use in all types of signal processing systems operating anywhere in the frequency range from DC to VHF
- Custom designed differential amplifiers
- Temperature compensated amplifiers
- See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Integrated-Circuit Transistor Array" for suggested applications.

STATIC CHARACTERISTICS

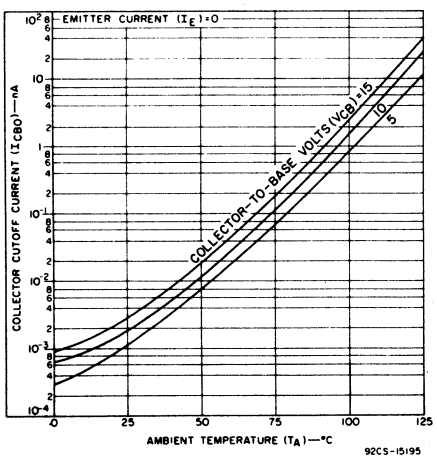


Fig.2 - Typical collector-to-base cutoff current vs ambient temperature for each transistor.

CA3045, CA3046 Types

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

Characteristics apply for each transistor in the CA3045 and CA3046 as specified.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS Type CA3045 Type CA3046 MIN.	TYP.	MAX.	UNITS
DYNAMIC CHARACTERISTICS						
Low-Frequency Noise Figure	NF	f = 1 kHz, V_{CE} = 3V, I_C = 100 μA Source Resistance = 1 kΩ	-	3.25	-	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:						
Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA	-	110	-	-
Short-Circuit Input Impedance	h_{ie}		-	3.5	-	kΩ
Open-Circuit Output Impedance	h_{oe}		-	15.6	-	μmho
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		-	1.8×10^{-4}	-	-
Admittance Characteristics:						
Forward Transfer Admittance	Y_{fe}	f = 1 MHz, V_{CE} = 3 V, I_C = 1 mA	-	31-j1.5	-	-
Input Admittance	Y_{ie}		-	0.3+j0.04	-	-
Output Admittance	Y_{oe}		-	0.001+j0.03	-	-
Reverse Transfer Admittance	Y_{re}		-	See curve	-	-
Gain-Bandwidth Product	f_T	V_{CE} = 3 V, I_C = 3 mA	300	550	-	-
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3 V, I_E = 0	-	0.6	-	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3 V, I_C = 0	-	0.58	-	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3 V, I_C = 0	-	2.8	-	pF

STATIC CHARACTERISTICS

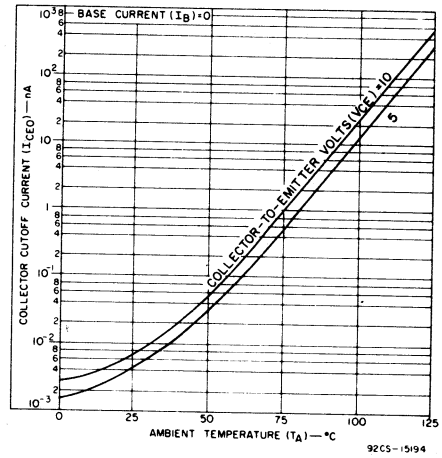


Fig.3 - Typical collector-to-emitter cutoff current vs ambient temperature for each transistor.

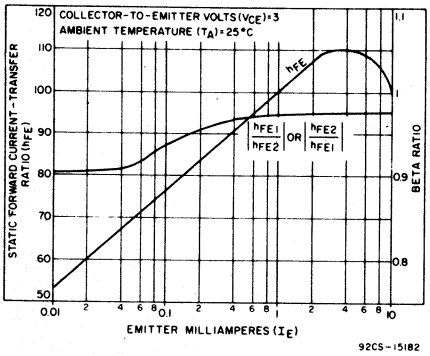


Fig.4 - Typical static forward current-transfer ratio and beta ratio for transistors Q_1 and Q_2 vs emitter current.

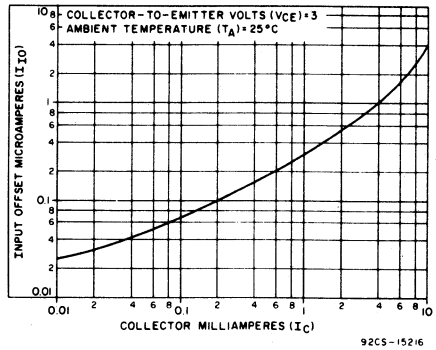


Fig.5 - Typical input offset current for matched transistor pair Q_1Q_2 vs collector current.

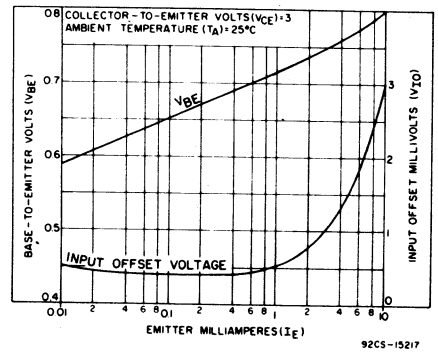


Fig.6 - Typical static base-to-emitter voltage characteristic and input offset voltage for differential pair and paired isolated transistors vs emitter current.

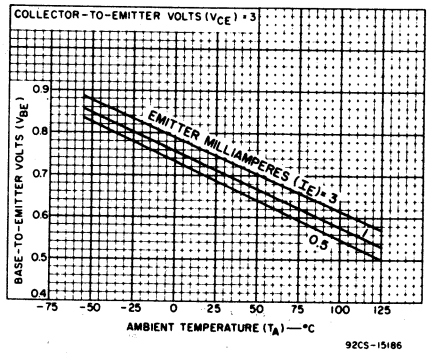


Fig.7 - Typical base-to-emitter voltage characteristic vs ambient temperature for each transistor.

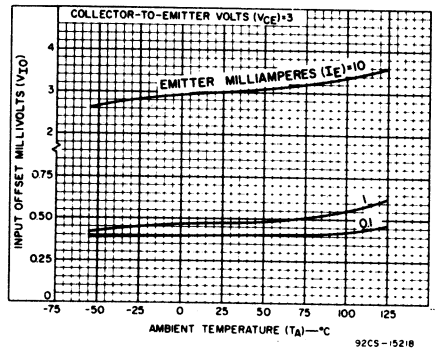


Fig.8 - Typical input offset voltage characteristics for differential pair and paired isolated transistors vs ambient temperature.

CA3045, CA3046 Types

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

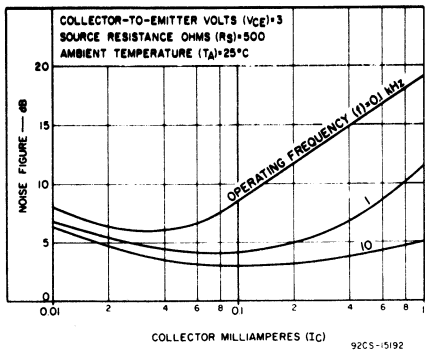


Fig.9(a) - Typical noise figure vs collector current.

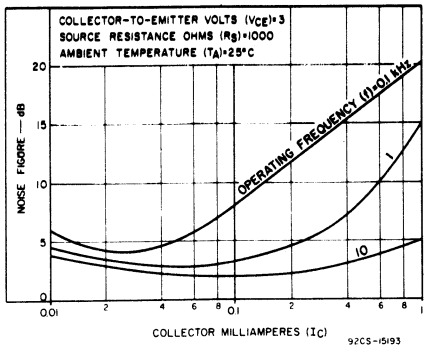


Fig.9(b) - Typical noise figure vs collector current.

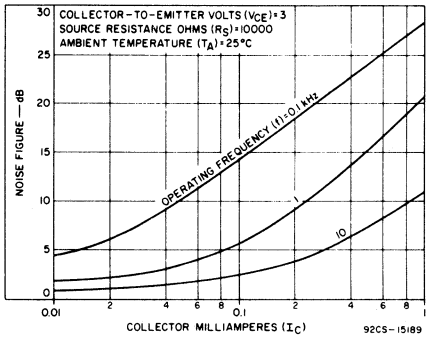


Fig.9(c) - Typical noise figure vs collector current.

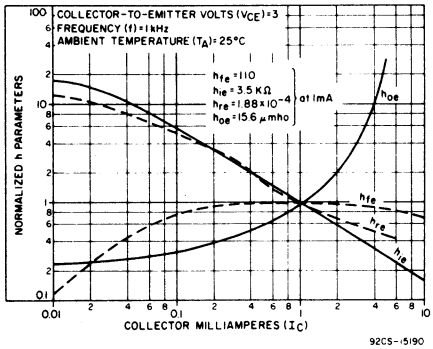


Fig.10 - Typical normalized forward current-transfer ratio, short-circuit input impedance, open-circuit output impedance, and open-circuit reverse voltage-transfer ratio vs collector current.

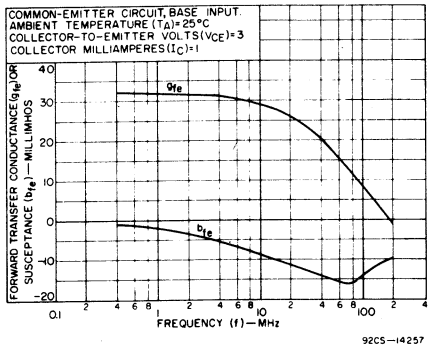


Fig.11 - Typical forward transfer admittance vs frequency.

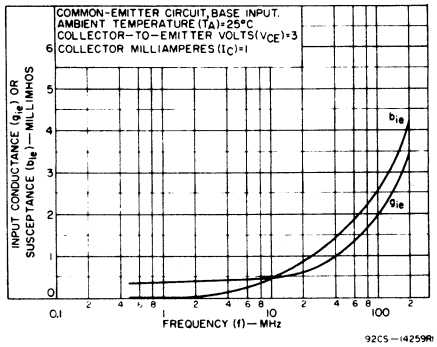


Fig.12 - Typical input admittance vs frequency.

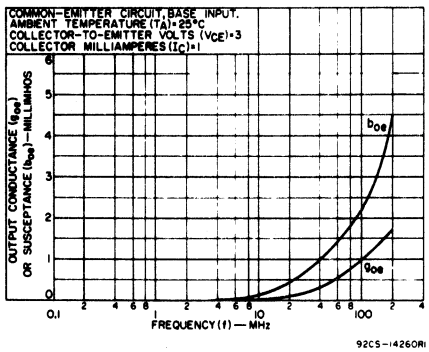


Fig.13 - Typical output admittance vs frequency.

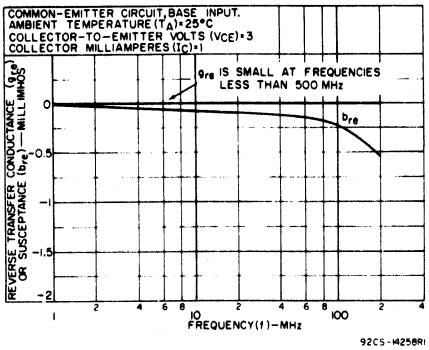


Fig.14 - Typical reverse transfer admittance vs frequency.

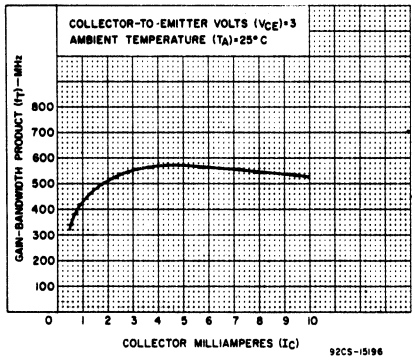


Fig.15 - Typical gain-bandwidth product vs collector current.

CA3048

Amplifier Array

FOUR INDEPENDENT AC AMPLIFIERS

For Low-Noise and General AC Applications In Industrial Service

The RCA CA3048 is a silicon monolithic integrated circuit consisting of four independent identical AC amplifiers which can operate from a single-ended power supply.

The amplifiers include internal DC bias and feedback to provide temperature-stabilized operation. They may be used in a wide variety of AC applications in which operational amplifiers have previously been used.

Each high gain amplifier has a high impedance non-inverting input, and a lower impedance inverting input for the application of feedback. Two power-supply terminals and two ground terminals are provided to reduce internal and external coupling between amplifiers.

The CA3048 is supplied in a 16-lead dual-in-line plastic package.

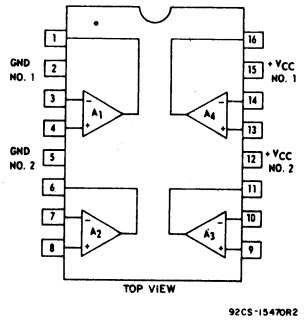


Fig.1 - Block diagram for CA3048.

ABSOLUTE-MAXIMUM RATINGS at T_A = 25°C:

DISSIPATION:
- At T_A = 55°C ..... 750 mW
- Above T_A = 55°C ..... Derate linearly at 7.7 mW/°C

TEMPERATURE RANGE:
- Operating ..... -40°C to +85°C
- Storage ..... -65°C to +150°C

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ±0.79mm) from case for 10 seconds max. ..... +265°C

POWER SUPPLY VOLTAGE ..... +16 V

AC INPUT VOLTAGE ..... 0.5 V rms

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 4 is +2 to -3.6 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1		+16 0	*	*	*	*	*	*	*	*	*	*	*	*	0 -16	*
2			*	+2 -3.6	0	*	*	+2 -3.6	-3.6	*	*	+16 0	+2 -3.6	*	+16 0	0 -16
3				+5 -5	*	*	*	*	*	*	*	*	*	*	*	*
4					+3.6 -2	*	*	*	*	*	*	*	*	*	*	*
5						0 -16	*	+2 -3.6	+2 -3.6	*	0 -16	+16 0	+2 -3.6	*	+16 0	*
6							*	*	*	*	*	*	0 -16	*	*	*
7								+5 -5	*	*	*	*	*	*	*	*
8									*	*	*	*	*	*	*	*
9										+5 -5	*	*	*	*	*	*
10											*	*	*	*	*	*
11												*	*	*	*	*
12													0 -16	*	*	*
13														+5 -5	*	*
14															*	*
15																+16 0
16																

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

FEATURES

- Four AC amplifiers on a common substrate
- Independently accessible inputs and outputs
- Operates from single-ended supply

EACH AMPLIFIER
- Noise figure at 1kHz ..... 2 dB typ.
- High voltage gain ..... 53 dB min.
- High input resistance ..... 90 kΩ typ.
- Undistorted output voltage ..... 2 V rms min.
- Output Impedance ..... 1 kΩ typ.
- Open-loop bandwidth ..... 300 kHz typ.

APPLICATIONS

- Multi-channel or cascade operation
- Low-level preamplifiers
- Equalizers
- Linear signal mixers
- Tone generators
- Multivibrators
- AC integrators

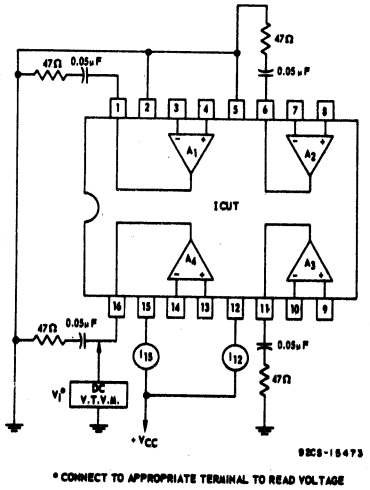


Fig.2 - Test circuit for measurement of collector supply voltage and currents.

CA3048

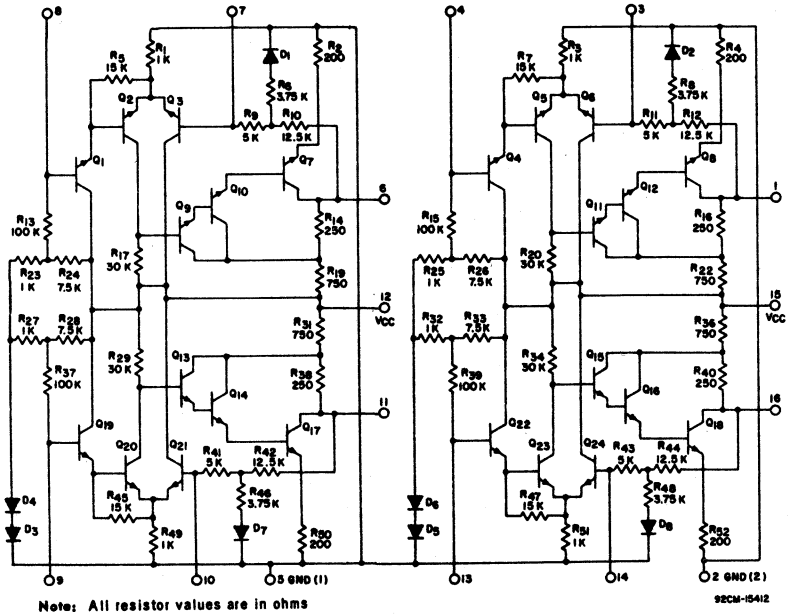


Fig.3 - Schematic diagram for CA3048.

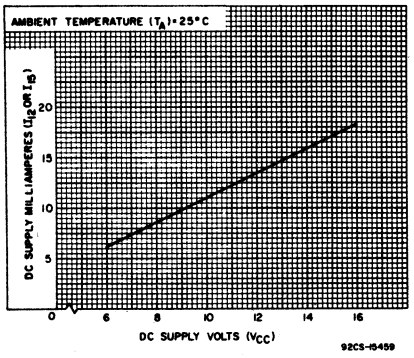


Fig.4 - Typical DC supply current vs supply voltage.

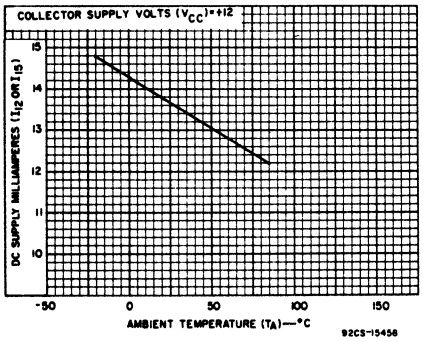
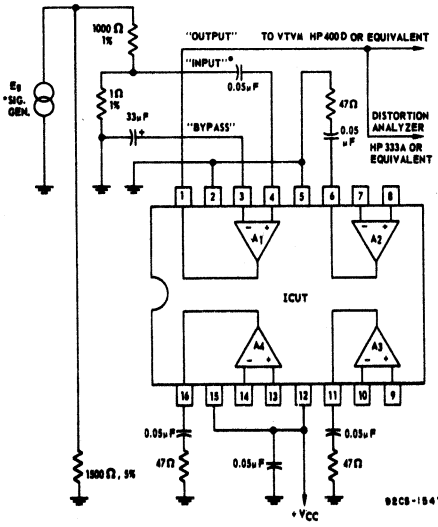


Fig.5 - Typical DC supply current vs ambient temperature.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIRCUIT FIG.	LIMITS CA3048 MIN.	LIMITS CA3048 TYP.	LIMITS CA3048 MAX.	UNITS	TYPICAL CHARACTERISTICS CURVES FIG.
STATIC								
Current drain per amplifier pair	I_{12} or I_{15}	V_{CC} = +12V	2	9.5	13.5	17.5	mA	4,5
DC Voltage at Output Terminals	V_1, V_6, V_{11}, V_{16}	V_{CC} = +12V	2	6.1	6.9	8.1	V	-
DC Voltage at Feedback Terminals	V_3, V_7, V_{10}, V_{14}	V_{CC} = +12V	2	1.7	2.0	2.3	V	-
DC Voltage at Input Terminals	V_4, V_8, V_9, V_{13}	V_{CC} = +12V	2	2.2	2.5	2.8	V	-
DYNAMIC (Characteristics given are for each amplifier with no AC feedback)								
Open-Loop Gain	A_{OL}	V_{CC} = +12V, E_{IN} = 2mV, f = 10kHz	6	53	58	-	dB	7,8
Output Voltage Swing	$V_{O(rms)}$	V_{CC} = +12V, f = 1kHz, THD = 5%	6	2.0	2.4	-	V	-
Open-Loop -3dB Bandwidth	BW	V_{CC} = +12V, E_{IN} = 2mV	6	250	300	-	kHz	9
Total Harmonic Distortion	THD	V_{CC} = +12V, f = 1kHz, E_{OUT} = 2V rms	6	-	0.65	-	%	10
Input Resistance	R_{IN}	OPEN LOOP Terminals 3, 7, 10, and 14 are by-passed to ground, f = 1kHz	-	-	90	-	kΩ	-
Input Capacitance	C_{IN}	f = 1MHz	-	-	9	-	pF	-
Output Resistance	R_{OUT}	Terminals 3, 7, 10 and 14 are by-passed to ground	-	-	1	-	kΩ	-
Output Capacitance	C_{OUT}	f = 1MHz	-	-	18	-	pF	-
Feedback Capacitance (Output to non-inverting input)	C_{FB}	V_{CC} = +12V, f = 1MHz	-	-	<0.1	-	pF	-
Broad-Band Output Noise Voltage	E_N	V_{CC} = +12V, R_S = 10kΩ, A = 40dB, Equivalent Noise BW = 50kHz	11	-	0.3	1	mV	-
Output Noise Voltage "Weighted"	$E_{N(WT)}$		12	-	0.5	2.2	mV	-
Noise Figure	NF (R_S = 5 kΩ)	f = 10 Hz	-	-	10	-	dB	-
		f = 100 Hz	-	-	5.8	-	dB	
		f = 1 kHz	-	-	2	-	dB	
		f = 10 kHz	-	-	1.1	-	dB	
		f = 100 kHz	-	-	0.6	-	dB	
Inter-Amplifier Audio Separation "Cross Talk"		V_{CC} = +12V, f = 1kHz, 0dB = 0.78V	13	-	<-45	-	dB	-
Inter-Amplifier Capacitance (Any amplifier output to any *other* amplifier input)	C	V_{CC} = +12V, f = 1MHz	-	-	<0.02	-	pF	-



* Sig Gen should be a low distortion type (0.2% THD or less) HP206A or equivalent.

● Adjustment of E_g to 2 volts will make E_g = 2mV.

Test Circuit shows Amplifier #1 under test, to test Amplifiers 2, 3, or 4; Connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig.6 - Test circuit for measurement of distortion, open-loop gain and bandwidth characteristics.

CA3048

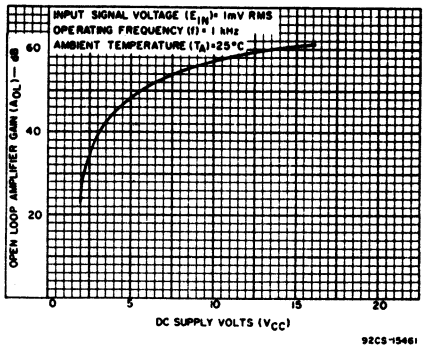


Fig.7 - Typical amplifier gain vs DC supply voltage.

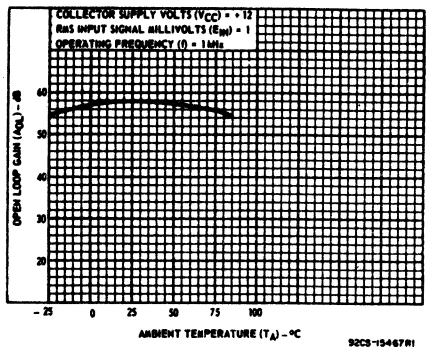


Fig.8 - Typical open-loop gain vs ambient temperature.

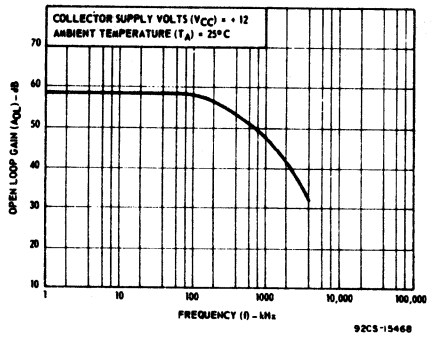


Fig.9 - Typical open-loop gain vs frequency.

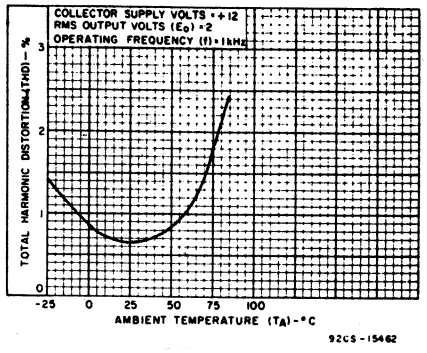
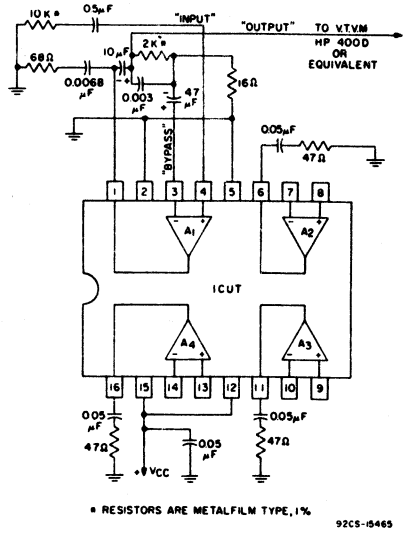


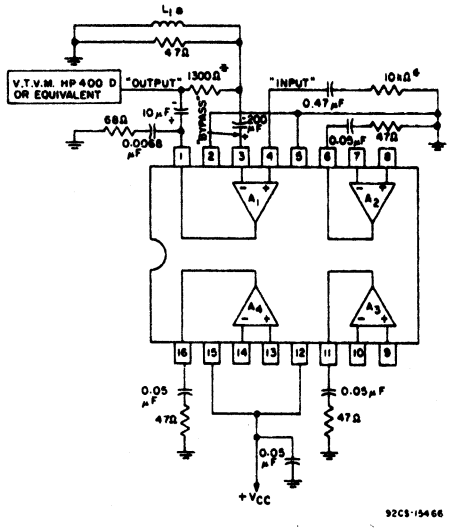
Fig.10 - Typical total harmonic distortion vs ambient temperature.



To test Amplifiers 1, 2, 3, or 4, connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig.11 - Test circuit for measurement of broadband noise characteristic.

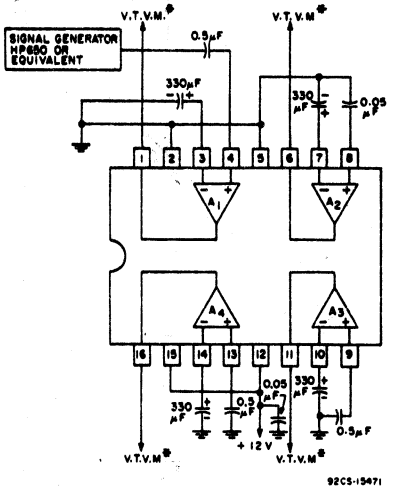


● L_1 - 2.5 millihenry inductor, dc resistance 0.3 ohms or less.

* Resistors metal film type, 1%. To test amplifiers, connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig.12 - Test circuit for measurement of "weighted" output noise voltage characteristic.



* V.T.V.M. - Hewlett-Packard Model 400D or equivalent.

Procedure:

1. Adjust Signal Generator for 0 dB output at reference terminal.
2. Read voltage at other output terminals (Figure shows terminal #1 used as reference).

Fig.13 - Test circuit for measurement of inter-amplifier audio separation "cross talk" characteristic.

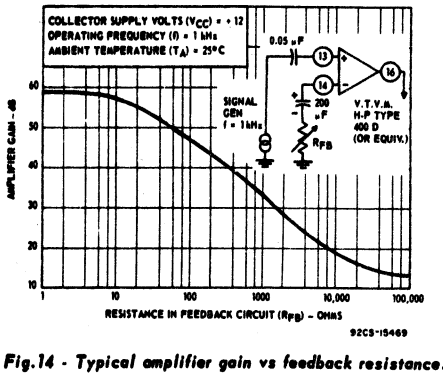


Fig.14 - Typical amplifier gain vs feedback resistance.

OPERATING CONSIDERATIONS

Economical Gain Control

The CA3048 is designed to permit flexibility in the methods by which amplifier gain can be controlled. Fig.14 shows a curve of the gain of an amplifier when the internal resistive feedback of the device is used in conjunction with an external resistor. Although measured gain of various amplifiers will not be uniform, because of tolerances of internal resistances, this method is very economical and easy to apply.

Stability

The CA3048, as in other devices having high gain-bandwidth product, requires some attention to circuit layout, design, and construction to achieve stability.

Should the CA3048 be left unterminated, socket capacitance alone will provide sufficient feedback to cause high frequency oscillations; therefore, all test circuits in this data bulletin include loading networks that provide stability under all conditions.

CA3049T, CA3102E

DUAL HIGH-FREQUENCY DIFFERENTIAL AMPLIFIERS

For Low-Power Applications at Frequencies up to 500 MHz

Features:

- **Power Gain 23 dB (typ.) at 200 MHz**
- **Noise Figure 4.6 dB (typ.) at 200 MHz**
- **Two differential amplifiers on a common substrate**
- **Independently accessible inputs and outputs**
- **Full military-temperature-range capability- (–55°C to + 125°C) for the CA3102E and for the CA3049T**
- **The CA3049 is available in a sealed-junction Beam-Lead version (CA3049L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".**

RCA-CA3049T and CA3102E consist of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six transistors which comprise the amplifiers are general-purpose devices which exhibit low I/f noise and a value of f_T in excess of 1 GHz. These features make the CA3049T and CA3102E useful from dc to 500 MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

The monolithic construction of the CA3049T and CA3102E provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual-channel applications where matched performance of the two channels is required.

The CA3102E is like the CA3049T except that it has a separate substrate connection for greater design flexibility. The CA3049T is supplied in the 12-lead TO-5 package; the CA3102E, in the 14-lead plastic dual-in-line package.

Applications

- VHF amplifiers
- VHF mixers
- Multifunction combinations – RF/Mixer/Oscillator; Converter/IF
- IF amplifiers (differential and/or cascode)
- Product detectors
- Doubly balanced modulators and demodulators
- Balanced quadrature detectors
- Cascade limiters
- Synchronous detectors
- Balanced mixers
- Synthesizers
- Balanced (push-pull) cascode amplifiers
- Sense amplifiers

MAXIMUM RATINGS, *ABSOLUTE-MAXIMUM VALUES, AT T_A = 25°C*

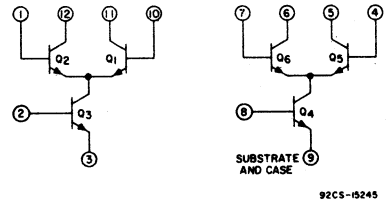
	CA3049T	CA3102E	
Power Dissipation, P:			
Any one transistor	300	300	mW
Total package	600	750	mW
For $T_A > 55°C$ Derate at:	5	6.67	mW/°C
Temperature Range:			
Operating	–55 to + 125	–55 to + 125	°C
Storage	–65 to + 150	–65 to + 150	°C

Lead Temperature (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. ..... +265°C

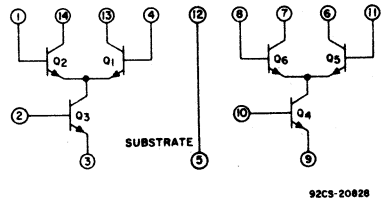
The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

*The collector of each transistor of the CA3049T and CA3102E is isolated from the substrate by an integral diode. The substrate (terminal 9) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.



Schematic Diagram for CA3049T



Schematic Diagram for CA3102E

Typical Characteristics for CA3049T and CA3102E

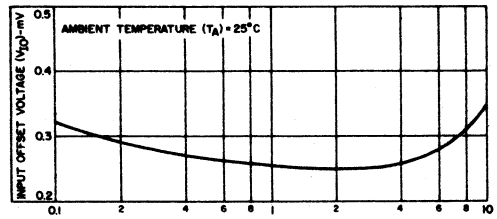


Fig. 4—Input offset voltage vs. emitter current.

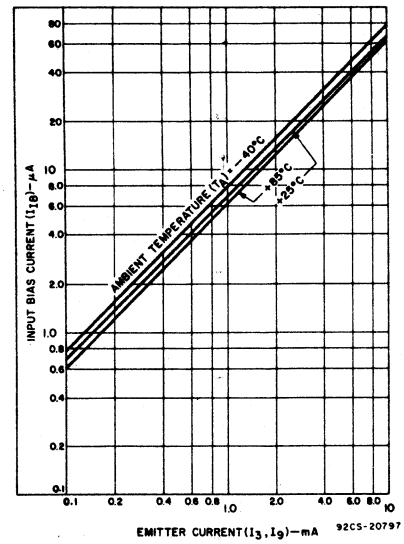


Fig. 5—Input bias current vs. emitter current.

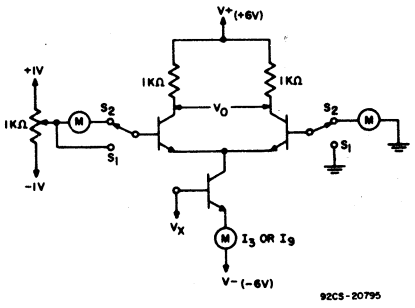


Fig. 1—Static characteristics test circuit for CA3102E.

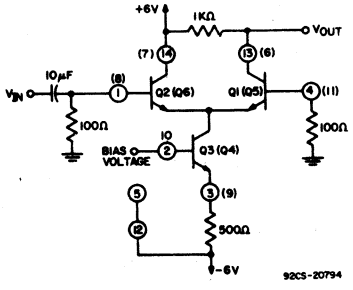
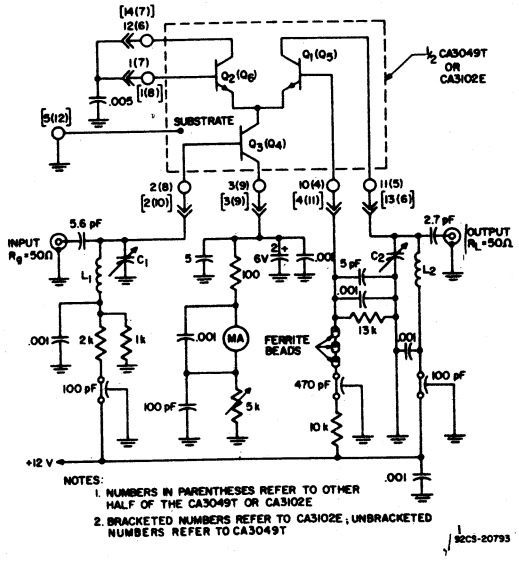


Fig. 2—AGC range and voltage gain test circuit for CA3102E.



L_1, L_2 – Approx. 1/2 Turn #18 Tinned Copper Wire, 5/8" Dia.
C_1, C_2 – 15 pF Variable Capacitors (Hammarlund, MAC-15; or Equivalent)
All Capacitors in μF Unless Otherwise Indicated
All Resistors in Ohms Unless Otherwise Indicated

Fig. 3—200 MHz cascode power gain and noise figure test circuit.

CA3049T, CA3102E

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		TEST CIRCUIT FIG.	CA3049T LIMITS MIN.	TYP.	MAX.	UNITS	TYPICAL CHARACTERISTICS CURVES FIG.
STATIC CHARACTERISTICS									
For Each Differential Amplifier									
Input Offset Voltage	V_{IO}			1	---	0.25	---	mV	4
Input Offset Current	I_{IO}	$I_3 = I_9$ = 2 mA		1	---	0.3	---	μA	---
Input Bias Current	I_{IB}			1		13.6	33	μA	5
Temperature Coefficient Magnitude of Input-Offset Voltage	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$			1	---	1.1	---	μV/°C	4
For Each Transistor									
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CE} = 6 V, I_C = 1 mA		---	---	774	---	mV	6
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 6 V, I_C = 1 mA		---	---	-0.9	---	mV/°C	6
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0		---	---	0.0013	100	nA	7
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0		---	15	24	---	V	---
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0		---	20	60	---	V	---
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_B = 0, I_E = 0		---	20	60	---	V	---
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0		---	5	7	---	V	---
DYNAMIC CHARACTERISTICS									
1/f Noise Figure (For Single Transistor)	NF	f = 100 KH$_3$, R_S = 500 Ω, I_C = 1 mA		---	---	1.5	---	dB	12
Gain-Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 6 V, I_C = 5 mA		---	---	1.35	---	GH$_z$	11
Collector-Base Capacitance	C_{CB}	I_C = 0	V_{CB} = 5V	*	---	0.28	---	pF	8
				**	---	0.28	---	pF	
Collector-Substrate Capacitance	C_{CI}	I_C = 0	V_{CI} = 5V		---	1.65	---	pF	8
For Each Differential Amplifier									
Common-Mode Rejection Ratio	CMR	$I_3 = I_9$ = 2 mA		---	---	100	---	dB	---
AGC Range, One Stage	AGC	Bias Voltage = -6V		2	---	75	---	dB	---
Voltage Gain, Single-Ended Output	A	Bias Voltage = -4.2V, f = 10 MHz		2	---	22	---	dB	9, 10
Insertion Power Gain	G_p	f = 200 MHz	Cascode	3	---	23	---	dB	---
Noise Figure	NF	V_{CC} = 12V	Cascode	3	---	4.6		dB	---
Input Admittance	Y_{11}	For Cascode Configuration $I_3 = I_9$ = 2 mA	Cascode	---	---	1.5 + j 2.45	---	mmho	14, 16, 18
			Diff.Amp.	---	---	0.878 + j 1.3	---		15, 17, 19
Reverse Transfer Admittance	Y_{12}	For Diff. Amplifier Configuration $I_3 = I_9$ = 4mA (each collector $I_C \simeq$ 2mA)	Cascode	---	---	0 - j 0.008	---	mmho	---
			Diff.Amp.	---	---	0 - j 0.013	---		---
Forward Transfer Admittance	Y_{21}		Cascode	---	---	17.9 - j 30.7	---	mmho	26, 28, 30
			Diff. Amp.	---	---	- 10.5 + j 13	---		27, 29, 31
Output Admittance	Y_{22}		Cascode	---	---	- 0.503 - j 15	---	mmho	20, 22, 24
			Diff.Amp.	---	---	0.071 + j 0.62	---		21, 23, 25

*Terminals 1 & 14, or 7 & 8. (CA3102E) 1 & 12 or 6 & 7 (CA3049T)
**Terminals 13 & 4, or 6 & 11. (CA3102E) 10 & 11 or 4 & 5 (CA3049T)

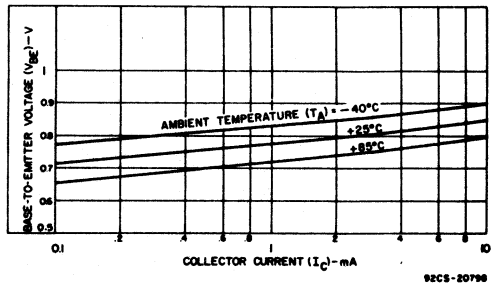


Fig. 6—Base-to-emitter voltage vs. collector current.

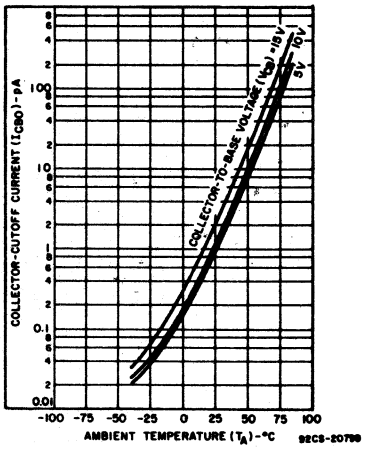


Fig. 7—Collector-cutoff current vs. temperature.

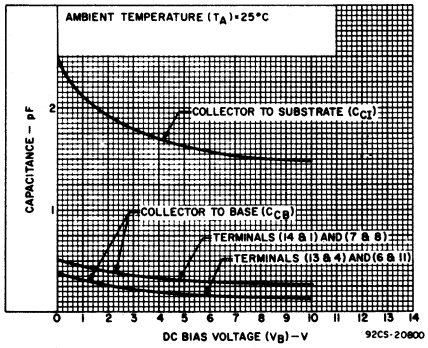


Fig. 8—Capacitance vs. dc bias voltage.

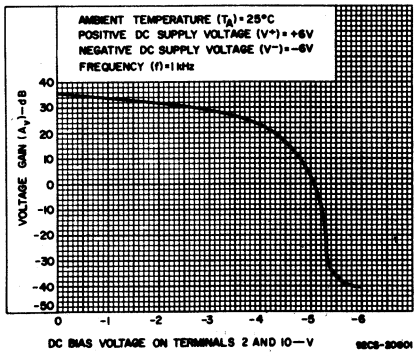


Fig. 9—Voltage gain vs. dc bias voltage.

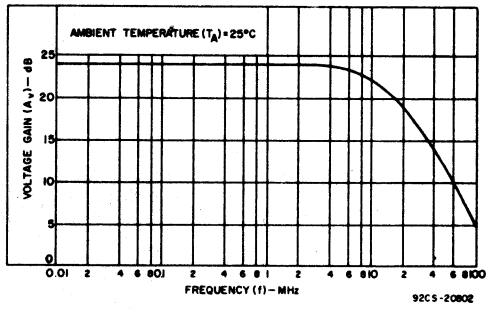


Fig. 10—Voltage gain vs. frequency.

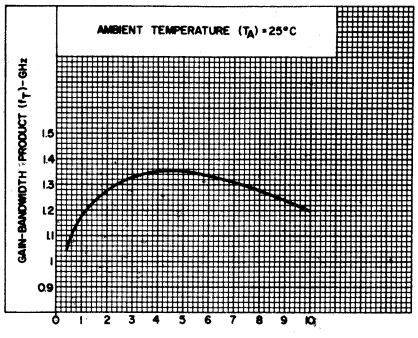


Fig. 11—Gain-bandwidth product vs. collector current.

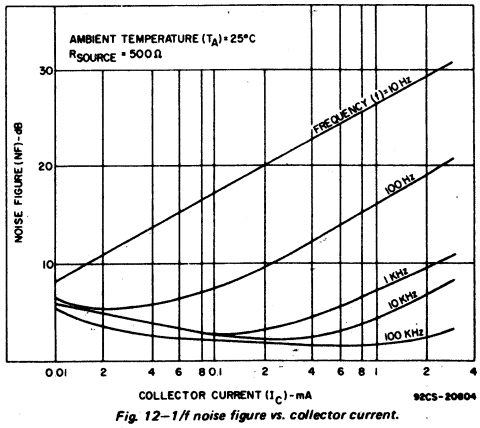


Fig. 12—1/f noise figure vs. collector current.

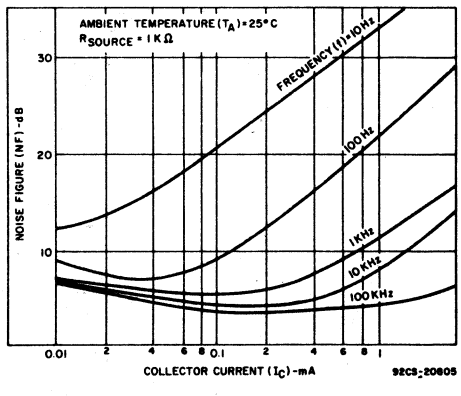


Fig. 13—1/f noise figure vs. collector current.

CA3049T, CA3102E

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		TEST CIR-CUIT FIG.	CA3102E LIMITS MIN.	TYP.	MAX.	UNITS	TYPICAL CHARAC-TERISTICS CURVES FIG.
STATIC CHARACTERISTICS									
For Each Differential Amplifier									
Input Offset Voltage	V_{IO}			1	...	0.25	5	mV	-4
Input Offset Current	I_{IO}	$I_3 = I_9$ = 2 mA		1	...	0.3	3	μA	...
Input Bias Current	I_{IB}			1	...	13.5	33	μA	5
Temperature Coefficient Magnitude of Input-Offset Voltage	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$			1	...	1.1	...	μV/°C	4
For Each Transistor									
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CE} = 6 V, I_C = 1 mA		...	674	774	874	mV	6
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 6 V, I_C = 1 mA		...	...	-0.9	...	mV/°C	6
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0		...	...	0.0013	100	nA	7
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0		...	15	24	...	V	...
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0		...	20	60	...	V	...
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_B = 0, I_E = 0		...	20	60	...	V	...
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0		...	5	7	...	V	...
DYNAMIC CHARACTERISTICS									
1/f Noise Figure (For Single Transistor)	NF	f = 100 KH$_3$, R_S = 500 Ω, I_C = 1 mA		...	...	1.5	...	dB	12
Gain-Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 6 V, I_C = 5 mA		...	...	1.35	...	GH$_z$	11
Collector-Base Capacitance	C_{CB}	I_C = 0, V_{CB} = 5V	*	...	...	0.28	...	pF	8
			**	...	...	0.15	...	pF	
Collector-Substrate Capacitance	C_{CI}	I_C = 0, V_{CI} = 5V		...	...	1.65	...	pF	8
For Each Differential Amplifier									
Common-Mode Rejection Ratio	CMR	$I_3 = I_9$ = 2 mA		...	...	100	...	dB	...
AGC Range, One Stage	AGC	Bias Voltage = -6V		2	...	75	...	dB	...
Voltage Gain, Single-Ended Output	A	Bias Voltage = -4.2V, f = 10 MHz		2	18	22	...	dB	9, 10
Insertion Power Gain	G_p	f = 200 MHz, V_{CC} = 12V	Cascode	3	...	23	...	dB	...
Noise Figure	NF		Cascode	3	...	4.6	...	dB	...
Input Admittance	Y_{11}	For Cascode Configuration, $I_3 = I_9$ = 2 mA	Cascode	...	...	1.5 + j 2.45	...	mmho	14, 16, 18
			Diff.Amp.	...	...	0.878 + j 1.3	...		15, 17, 19
Reverse Transfer Admittance	Y_{12}	For Diff. Amplifier Configuration, $I_3 = I_9$ = 4mA (each collector $I_C \simeq$ 2mA)	Cascode	...	...	0 - j 0.008	...	mmho	...
			Diff.Amp.	...	...	0 - j 0.013	...		...
Forward Transfer Admittance	Y_{21}		Cascode	...	...	17.9 - j 30.7	...	mmho	26, 28, 30
			Diff. Amp.	...	...	- 10.5 + j 13	...		27, 29, 31
Output Admittance	Y_{22}		Cascode	...	...	- 0.503 - j 15	...	mmho	20, 22, 24
			Diff.Amp.	...	...	0.071 + j 0.62	...		21, 23, 25

*Terminals 1 & 14, or 7 & 8. (CA3102E) 1 & 12 or 6 & 7 (CA3049T)
**Terminals 13 & 4, or 6 & 11. (CA3102E) 10 & 11 or 4 & 5 (CA3049T)

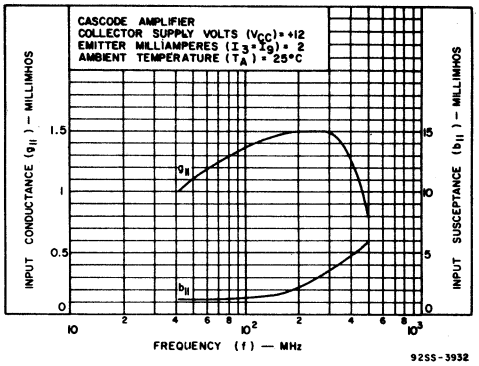


Fig. 14—Input admittance (Y_{11}) vs. frequency.

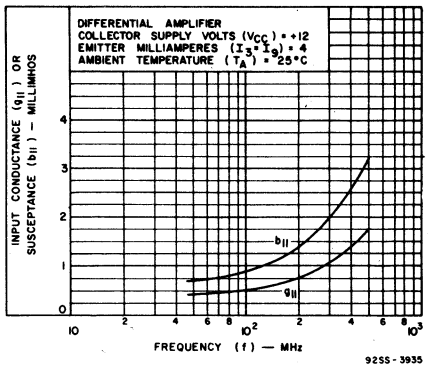


Fig. 15—Input admittance (Y_{11}) vs. frequency.

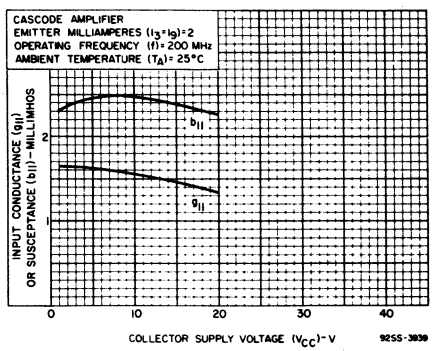


Fig. 16—Input admittance (Y_{11}) vs. collector supply voltage.

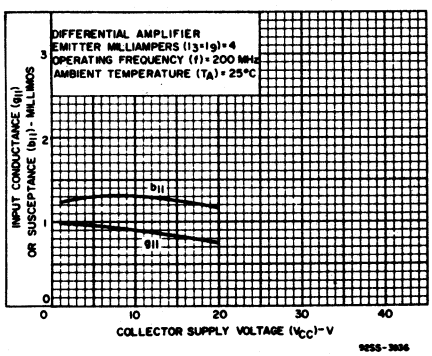


Fig. 17—Input admittance (Y_{11}) vs. collector supply voltage.

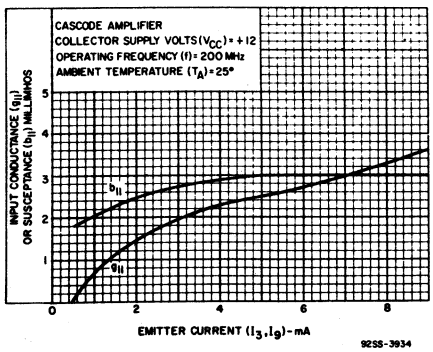


Fig. 18—Input admittance (Y_{11}) vs. emitter current.

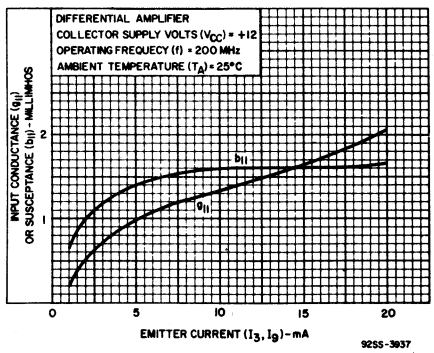


Fig. 19—Input admittance (Y_{11}) vs. emitter current.

CA3049T, CA3102E

Typical Output Admittance Characteristics for CA3049T and CA3102E

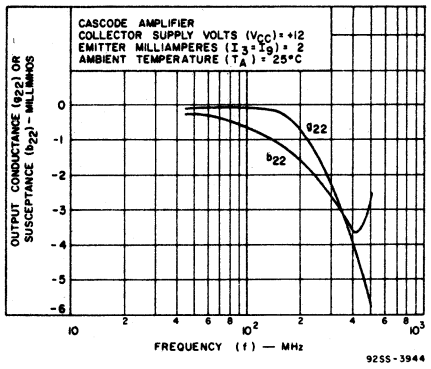


Fig. 20—Output admittance (Y_{22}) vs. frequency.

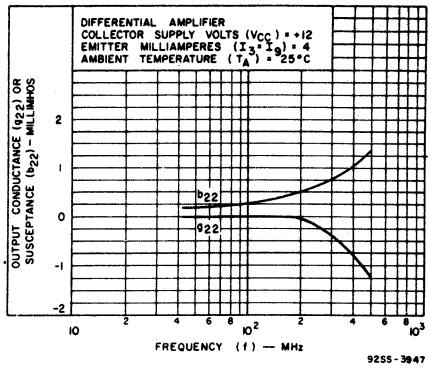


Fig. 21—Output admittance (Y_{22}) vs. frequency.

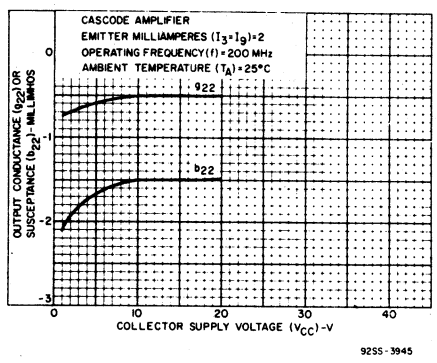


Fig. 22—Output admittance (Y_{22}) vs. collector supply voltage.

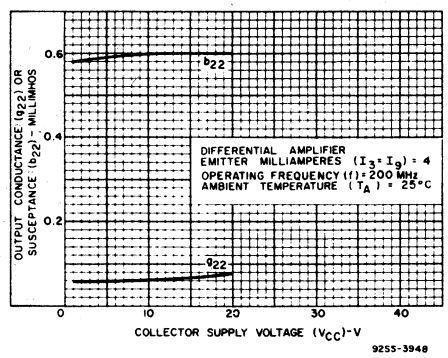


Fig. 23—Output admittance (Y_{22}) vs. collector supply voltage.

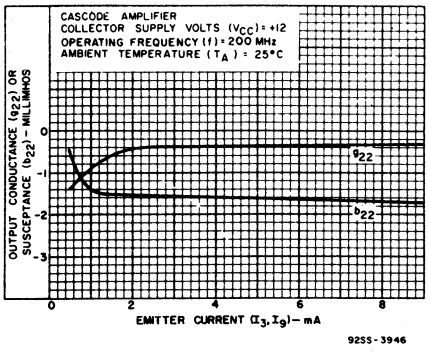


Fig. 24—Output admittance (Y_{22}) vs. emitter current.

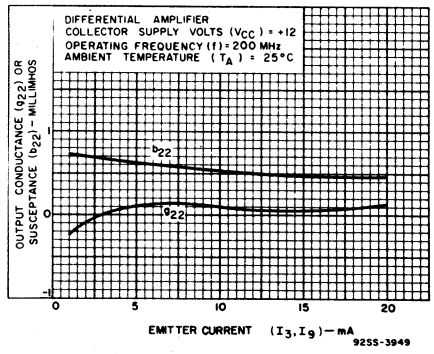


Fig. 25—Output admittance (Y_{22}) vs. emitter current.

Typical Forward Transfer Characteristics for CA3049T and CA3102E

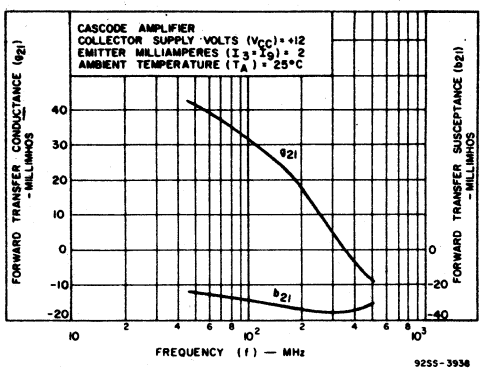


Fig. 26—Forward transfer admittance (Y_{21}) vs. frequency.

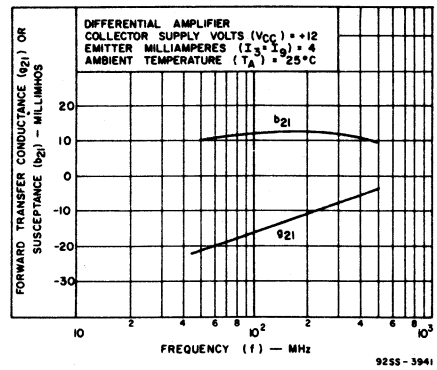


Fig. 27—Forward transfer admittance (Y_{21}) vs. frequency.

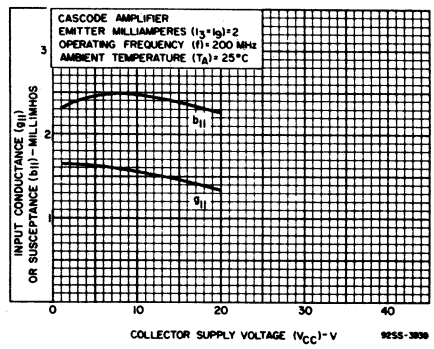


Fig. 28—Forward transfer admittance (Y_{21}) vs. collector supply voltage.

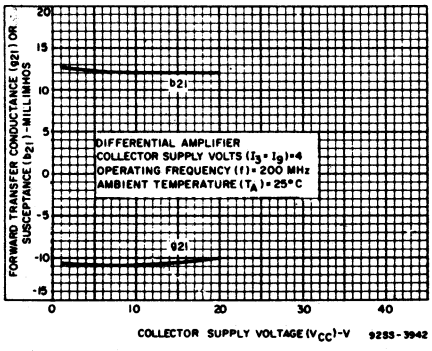


Fig. 29—Forward transfer admittance (Y_{21}) vs. collector supply voltage.

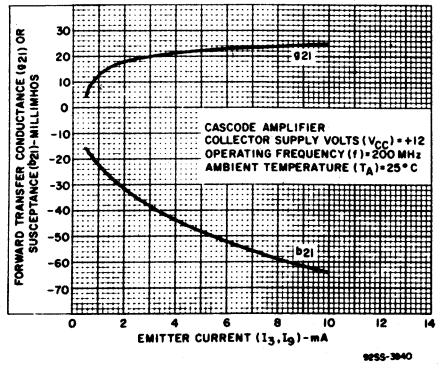


Fig. 30—Forward transfer admittance (Y_{21}) vs. emitter current.

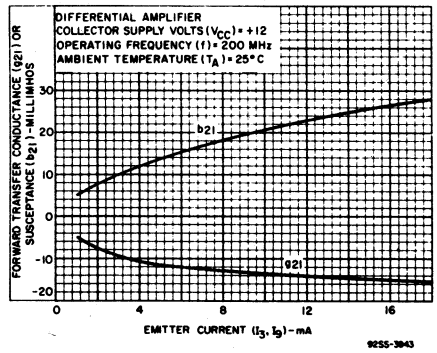


Fig. 31—Forward transfer admittance (Y_{21}) vs. emitter current.