CA3050, CA3051

Dual Differential Amplifiers For Low-Power Applications at Frequencies from DC to 20 MHz

TWO DARLINGTON-CONNECTED DIFFERENTIAL AMPLIFIERS WITH DIODE BIAS STRING

The CA3050 and CA3051 each consists of two differential amplifiers with associated constant current transistors on a common substrate. Each amplifier is driven by Darlington-connected emitter follower inputs to provide high input impedance, low bias current, and low offset current. A string of diodes is included to provide temperature-compensated bias to the constant current transistors and a low impedance bias point for the inputs to the differential amplifiers when a single power supply is used.

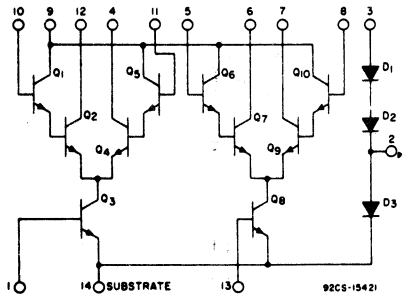

Fig.1 - Schematic diagram.

APPLICATIONS

- Matched dual amplifiers
- Dual sense amplifiers
- Dual Schmitt triggers
- Dual multivibrators
- Doubly balanced detectors and modulators
- Balanced quadrature detectors
- Synthesizer mixers
- Product detectors

FEATURES

- Input offset current . . . . . 70 nA max.
- Input bias current . . . . . 500 nA max.
- Input offset voltage . . . . . 5 mV max.
- Input impedance . . . . . 460 kΩ typ.
- Independently accessible inputs and outputs

- **CA3050—14-lead dual-in-line ceramic package**
- **CA3051—14-lead dual-in-line plastic package**

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES, AT T_A = 25°C

	CA3050	CA3051	
Power Dissipation, P:			
Any one transistor	150	150	mW
Total package	900	750	mW
For T_A > 55°C, Derate at	8	6.67	mW/°C
Temperature Range:			
Operating	-55 to +125		°C
Storage	-65 to +150		°C
LEAD TEMPERATURE (During Soldering) At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265		°C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

* The collector of each transistor of the CA3050 and CA3051 is isolated from the substrate by an integral diode. *The substrate (terminal 14) must be more negative than all collectors to maintain isolation between transistors and to provide for normal transistor action.*

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 3 is +5 to −2 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	–	•	•	•	•	•	•	•	•	•	•	•	•	+1 -5
2			+5 -2	•	•	•	•	•	•	•	•	•	•	+1 -1
3				•	•	•	•	•	•	•	•	•	•	+3 -1
4					•	•	•	•	•	+14 -2.5 Note 3	+14 -2.5 Note 4	•	•	+20 -1
5						+2.5 -14 Note 1	+2.5 -14 Note 1	+10 -10	+1 -20	•	•	•	•	+16 -1
6							•	+14 -2.5 Note 2	•	•	•	•	•	+20 -1
7								+14 -2.5 Note 2	•	•	•	•	•	+20 -1
8									+1 20	•	•	•	•	+16 -1
9										+20 -1	+20 -1	•	•	+20 -1
10											+10 -10	+2.5 -14 Note 3	•	+16 -1
11												+2.5 -14 Note 4	•	+16 -1
12														+20 -1
13														+1 -5
14														Ref. Substrate

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	5	0.1
2	50	50
3	50	1
4	50	1
5	5	0.1
6	50	1
7	50	1
8	5	0.1
9	50	1
10	5	0.1
11	5	0.1
12	50	1
13	5	0.1
14	100	5

NOTE 1: This rating is important only when terminal 6 is more positive than terminal 8.

NOTE 2: This rating is important only when terminal 8 is more positive than terminal 5.

NOTE 3: This rating is important only when terminal 10 is more positive than terminal 11.

NOTE 4: This rating is important only when terminal 11 is more positive than terminal 10.

*Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

TYPICAL STATIC CHARACTERISTICS

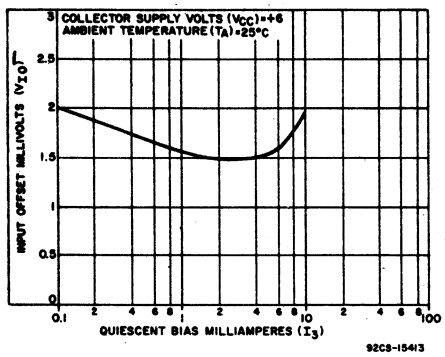

Fig.2(a) - Typical input offset voltage vs quiescent bias current.

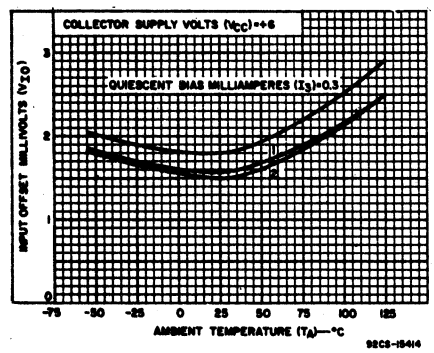

Fig.2(b) - Typical input offset voltage vs ambient temperature.

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ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIRCUIT FIG.	LIMITS CA3050/CA3051 MIN.	TYP.	MAX.	UNITS	TYPICAL CHARACTERISTICS CURVES FIG.
STATIC								
Amplifier Characteristics								
Input Offset Voltage	V_{IO}		–	–	1.5	5	mV	2a,b
Input Offset Current	I_{IO}		–	–	7	70	nA	3a,b
Input Bias Current	I_{IB}		–	–	200	500	nA	4a,b
Quiescent Operating Current Ratio	$\frac{(I_4+I_{12})}{I_3}$ or $\frac{(I_6+I_7)}{I_3}$	V_{CC} = + 6 V, I_3 = 2 mA	–	0.9	1.00	1.13	–	5a,b
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_C = 50 μA	–	–	0.645	0.700	V	6
		V_{CE} = 3 V, I_C = 1 mA	–	–	0.725	0.800	V	6
		V_{CE} = 3 V, I_C = 3 mA	–	–	0.760	0.850	V	6
		V_{CE} = 3 V, I_C = 10 mA	–	–	0.805	0.900	V	6
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA	–	–	-1.9	–	mV/°C	7
Transistor Characteristics								
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	–	0.002	100	nA	8
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	–	15	24	–	V	–
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	–	20	60	–	V	–
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	–	20	60	–	V	–
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	–	5	7	–	V	–
DYNAMIC								
Transistor Characteristics								
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3 V, I_E = 0	–	–	0.78	–	pF	9
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3 V, I_C = 0	–	–	0.47	–	pF	9
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3 V, I_C = 0	–	–	1.92	–	pF	9
Amplifier Characteristics								
Gain-Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 5 V, I_C = 3 mA	–	–	600	–	MHz	10
Forward Transadmittance (With single-ended input and output)	$\lvert y_{21} \rvert$	V_{CC} = 10 V, I_3 = 2 mA f = 1 MHz	11	7	9	11	mmho	11
Bandwidth at -3 dB Point	BW	V_{CC} = 10 V, I_3 = 2 mA	11	–	4.3	–	MHz	11
Input Impedance	Z_I	V_{CC} = 10 V, I_3 = 2 mA f = 1 KHz	12	–	460	–	kΩ	12
Output Impedance	Z_O	I_3 = 2 mA, f = 1 KHz	13	–	170	–	kΩ	13
Common-Mode Rejection Ratio	CMR	I_3 = 2 mA, f = 1 KHz	–	–	65	–	dB	–
AGC Range	AGC	I_3 = 2 mA, f = 1 KHz Terminal No.3 Grounded	11	–	60	–	dB	–

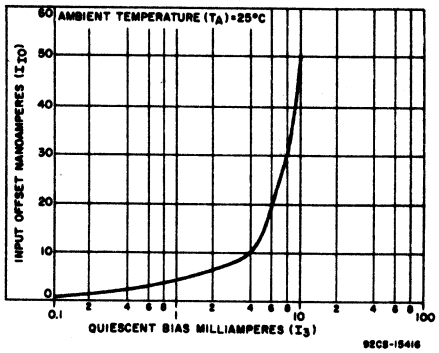

Fig.3(a) - Typical input offset current vs quiescent bias current.

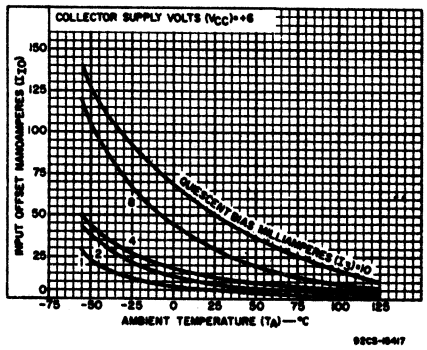

Fig.3(b) - Typical input offset current vs ambient temperature.

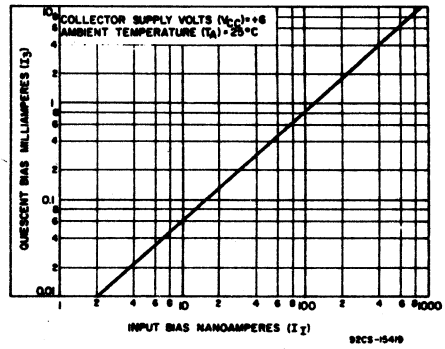

Fig.4(a) - Typical quiescent bias current vs input bias current.

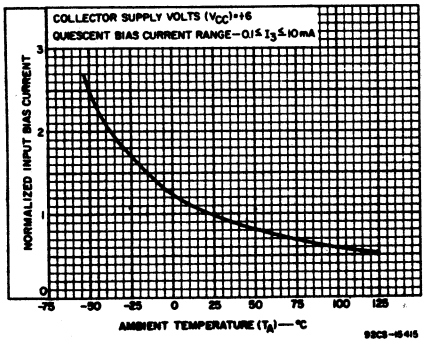

Fig.4(b) - Typical normalized input bias current vs ambient temperature.

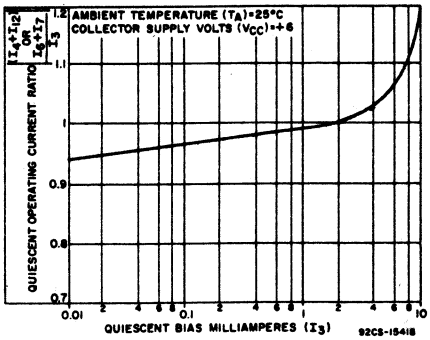

Fig.5(a) - Typical quiescent operating current ratio vs quiescent bias current.

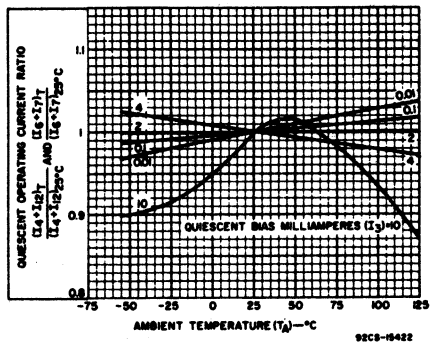

Fig.5(b) - Typical quiescent operating current ratio vs ambient temperature.

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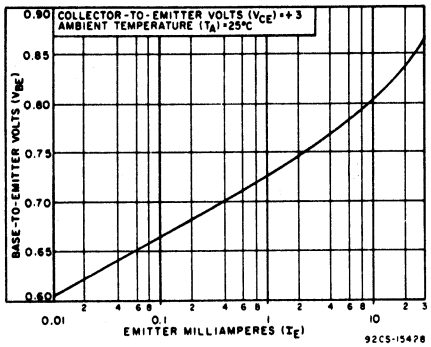


Fig.6 - Typical static base-to-emitter voltage characteristic vs emitter current for all transistors and forward diode voltage drops.

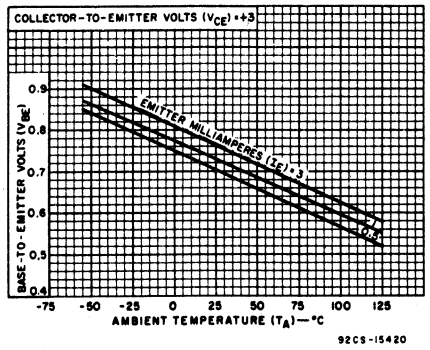


Fig.7 - Typical base-to-emitter voltage characteristic vs ambient temperature for each transistor.

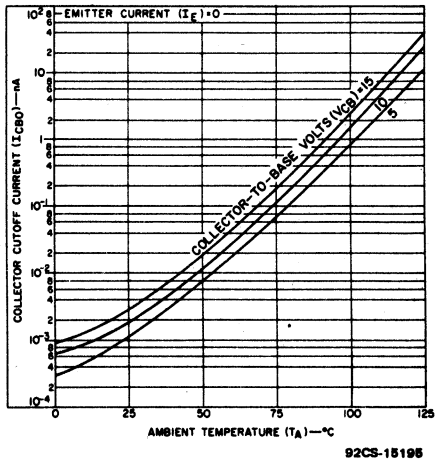


Fig.8 - Typical collector-to-base cutoff current vs ambient temperature for each transistor.

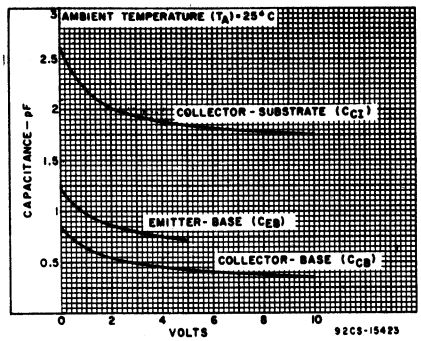


Fig.9 - Typical capacitance for each transistor.

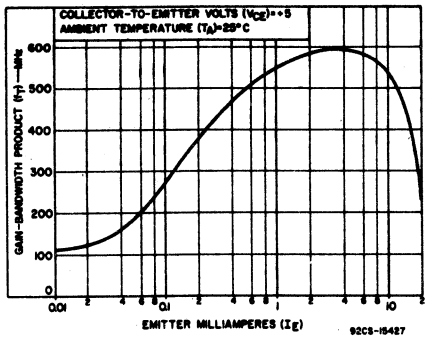
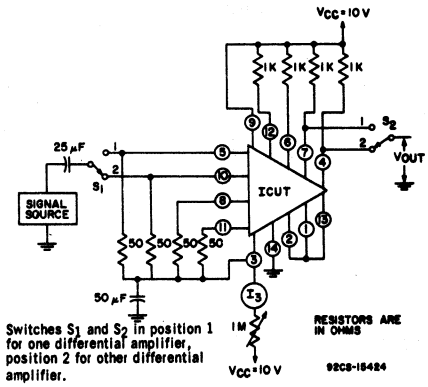


Fig.10 - Typical gain-bandwidth product (f_T) for each transistor vs emitter current.



Switches S_1 and S_2 in position 1 for one differential amplifier, position 2 for other differential amplifier.

Fig.11(a) - Test circuit for forward transadmittance, -3 dB bandwidth, and AGC range.

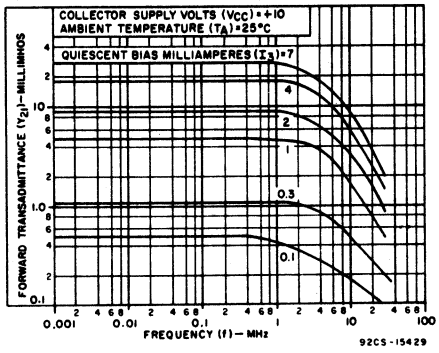


Fig.11(b) - Typical differential amplifier forward transadmittance with single-ended output vs frequency.

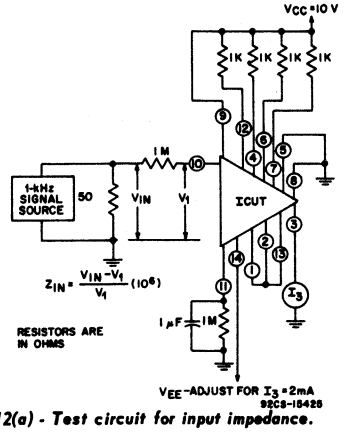


Fig.12(a) - Test circuit for input impedance.

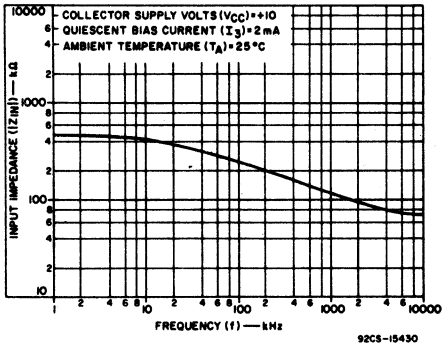
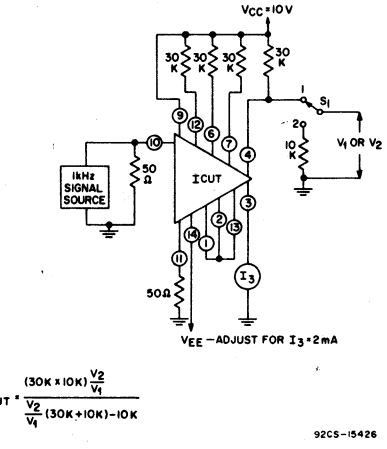


Fig.12(b) - Typical input impedance vs frequency with output short-circuited.



$$Z_{OUT} = \frac{(30K \times 10K)\frac{V_2}{V_1}}{\frac{V_2}{V_1}(30K+10K)-10K}$$

Fig.13(a) - Test circuit for output impedance.

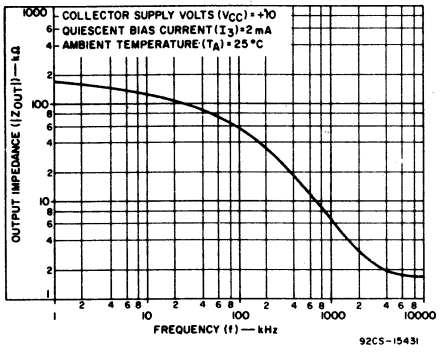


Fig.13(b) - Typical output impedance vs frequency with input short-circuited.

CA3052

Special-Function Sub-System Stereo Preamplifier

FOUR INDEPENDENT AC AMPLIFIERS

For Stereo Preamplifiers, Magnetic Pickups, Tape Heads, etc.

The RCA CA3052 is a silicon monolithic integrated circuit designed specifically for stereo preamplifier service. The circuit consists of four independent AC amplifiers which can operate from a single-ended supply.

The CA3052 can operate as an equalizer amplifier in tape recorders, magnetic cartridge phonograph applications, and tone control amplifiers. The CA3052 can provide all of the amplification necessary for a full-function stereo preamplifier.

The CA3052 is supplied in a 16-lead dual-in-line plastic package.

APPLICATIONS

- Full-function stereo preamplifiers
- Tape recorder and playback preamplifiers
- Tone Generators

FEATURES

- Four AC amplifiers on a common substrate
- Independently accessible inputs and outputs
- Operates from single-ended supply

EACH AMPLIFIER

- High voltage gain . . . . . 53 dB min.
- High input resistance . . . . . 90 k Ω typ.
- Undistorted output voltage . . . . . 2 V rms min.
- Output Impedance . . . . . 1 k Ω typ.
- Open-loop bandwidth . . . . . 300 kHz typ.

RCA CA3048 Amplifier Array (File No.377) is schematically identical with the CA3052. Each amplifier of the CA3048 is tightly specified for equivalent output noise under a variety of test methods. The CA3052 is specified using RIAA test methods for equivalent input noise using one test method for amplifiers 1 and 4, and an appropriately different method for amplifiers 2 and 3.

ABSOLUTE-MAXIMUM RATINGS at T_A = 25°C:

DISSIPATION:
- Up to T_A = 55°C . . . . . 750 mW
- Above T_A = 55°C . . . . . Derate linearly at 7.7 mW/°C

TEMPERATURE RANGE:
- Operating . . . . . −40°C to +85°C
- Storage . . . . . −65°C to +150°C

LEAD TEMPERATURE (During Soldering):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . . +265°C

POWER SUPPLY VOLTAGE . . . . . +16 V

AC INPUT VOLTAGE . . . . . 0.5 V rms

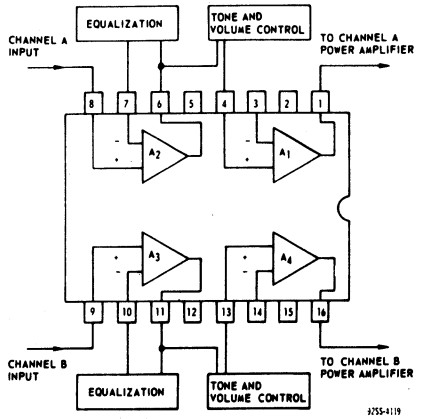


Fig. 1 – Block diagram of stereo preamplifier using CA3052.

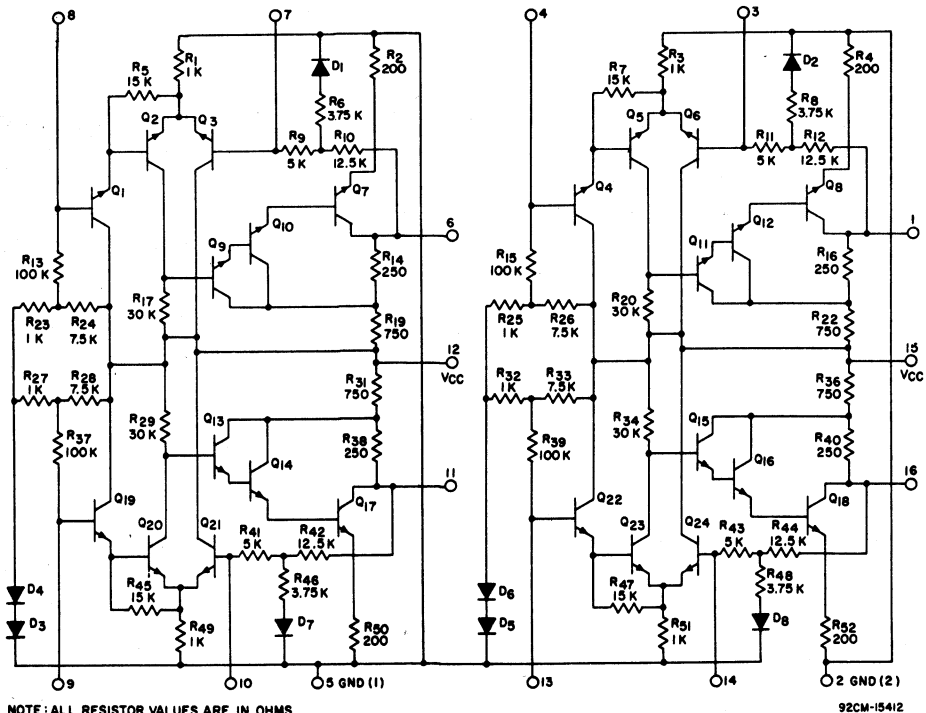


Fig. 2 - Schematic diagram for CA3052.

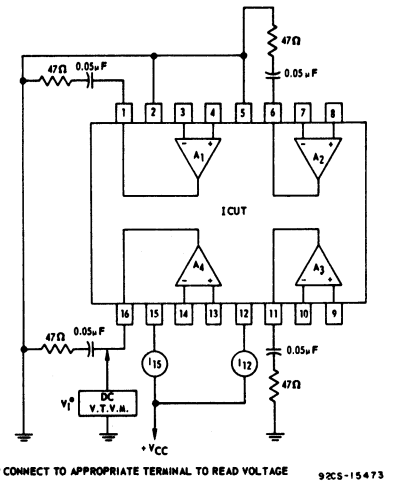


Fig. 3 - Test circuit for measurement of collector supply voltage and currents.

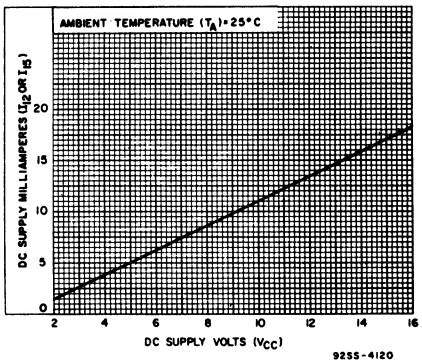


Fig. 4 - Typical DC supply current vs supply voltage.

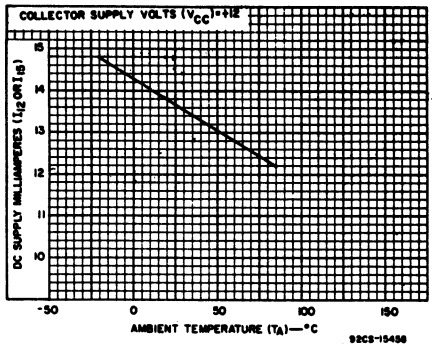


Fig. 5 - Typical DC supply current vs ambient temperature.

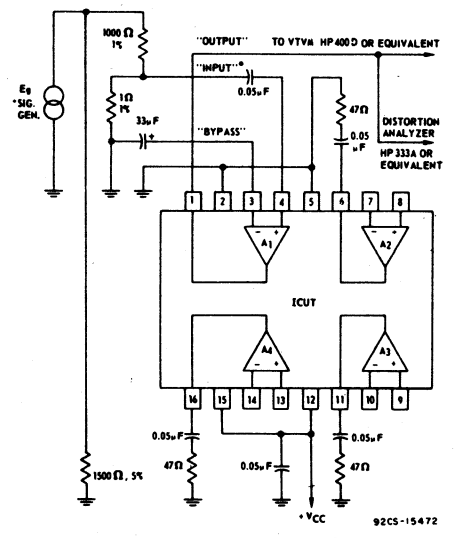
CA3052

MAXIMUM VOLTAGE RATINGS

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 4 is +2 to -3.6 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1		+16 0	*	*	*	*	*	*	*	*	*	*	*	*	0 -16	*
2			*	+2 -3.6	0	*	*	+2 -3.6	+2 -3.6	*	*	+16 0	+2 -3.6	*	+16 0	0 -16
3				+5 -5	*	*	*	*	*	*	*	*	*	*	*	*
4					+3.6 -2	*	*	*	*	*	*	*	*	*	*	*
5						0 -16	*	+2 -3.6	+2 -3.6	*	0 -16	+16 0	+2 -3.6	*	+16 0	*
6							*	*	*	*	*	*	0 -16	*	*	*
7								+5 -5	*	*	*	*	*	*	*	*
8									*	*	*	*	*	*	*	*
9										+5 -5	*	*	*	*	*	*
10											*	*	*	*	*	*
11												*	*	*	*	*
12													0 -16	*	*	*
13														+5 -5	*	*
14															*	*
15																+16 0
16																

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.



* Sig. Gen. should be a low distortion type (0.2% THD or less) HP206A or equivalent.

● Adjustment of E_g to 2 volts will make E_s = 2mV.

Test Circuit shows Amplifier #1 under test, to test Amplifiers 2, 3, or 4; Connect terminals as shown in Table.

AMPLIFIER	TERMINALS		
	OUTPUT	INPUT	BYPASS
1	1	4	3
2	6	8	7
3	11	9	10
4	16	13	14

Fig. 6 - Test circuit for measurement of distortion, open-loop gain, and bandwidth characteristics.

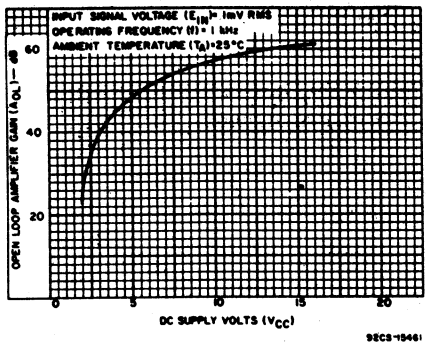


Fig. 7 - Typical amplifier gain vs DC supply voltage.

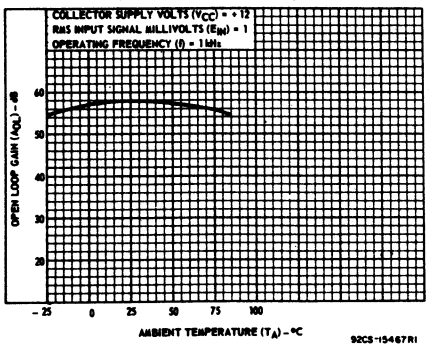


Fig. 8 - Typical open-loop gain vs ambient temperature.

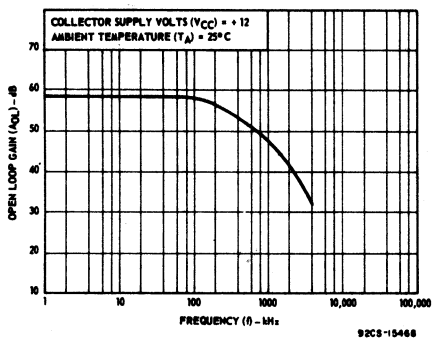


Fig. 9 - Typical open-loop gain vs frequency.

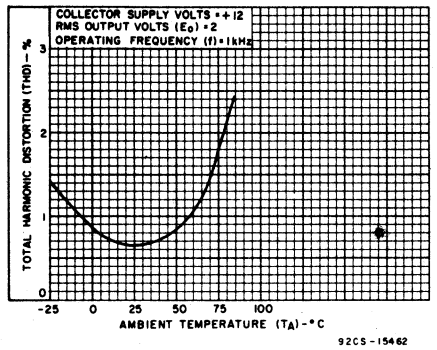
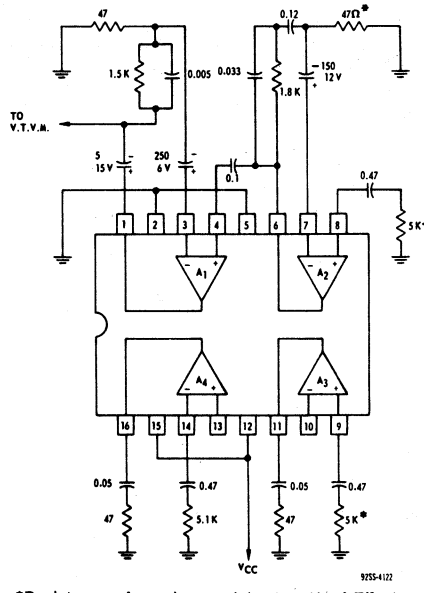


Fig. 10. - Typical total harmonic distortion vs ambient temperature.



*Resistors are low noise precision (1%) Metal Film type.

Fig. 11 - Test circuit for equivalent input noise voltage measurement, RIAA compensated.

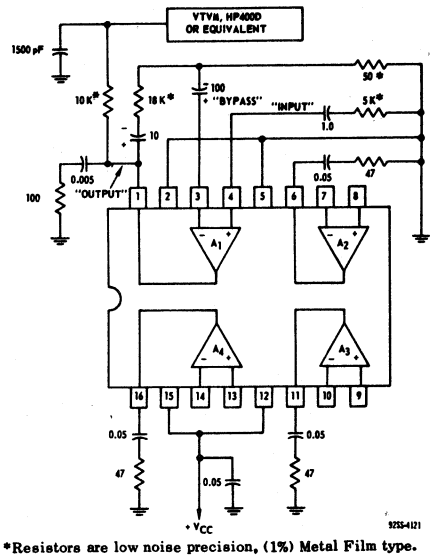
CA3052

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIR-CUIT	LIMITS CA3052			UNITS	TYPICAL CHARAC-TERISTICS CURVES
			FIG.	MIN.	TYP.	MAX.		FIG.
STATIC								
Current drain per amplifier pair	I_{12} or I_{15}	V_{CC} = +12 V	3	9.5	13.5	17.5	mA	4, 5
DC Voltage at Output Terminals	V_1, V_6, V_{11}, V_{16}	V_{CC} = +12 V	3	6.1	6.9	8.1	V	–
DC Voltage at Feedback Terminals	V_3, V_7, V_{10}, V_{14}	V_{CC} = +12 V	3	1.7	2.0	2.3	V	–
DC Voltage at Input Terminals	V_4, V_8, V_9, V_{13}	V_{CC} = +12 V	3	2.2	2.5	2.8	V	–
DYNAMIC each amplifier with no AC feedback unless otherwise noted–terminals 3, 7, 10, & 14 bypassed to ground								
Open-Loop Gain	A_{OL}	V_{CC} = +12 V E_{IN} = 2 mV f = 10 kHz	6	53	58	–	dB	7, 8
Open-Loop Output Voltage Swing	V_O(rms)	V_{CC} = +12 V f = 1 kHz THD = 5%	6	2.0	2.4	–	V	–
Open-Loop -3 dB Bandwidth	BW	V_{CC} = +12 V E_{IN} = 2 mV	6	–	300	–	kHz	9
Open-Loop Total Harmonic Distortion	THD	V_{CC} = +12 V, f = 1 kHz E_{OUT} = 2 V rms	6	–	0.65	–	%	10
Input Resistance	R_I	V_{CC} = +12 V, f = 1 kHz	–	–	90	–	kΩ	–
Input Capacitance	C_I	V_{CC} = +12 V, f = 1 MHz	–	–	9	–	pF	–
Output Resistance	R_O	V_{CC} = +12 V, f = 1 kHz	–	–	1	–	kΩ	–
Feedback Capacitance (Output to non-inverting Input)	C_{FB}	V_{CC} = +12 V f = 1 MHz	–	–	<0.1	–	pF	–
Equivalent Input Noise Voltage (Amplifiers 1 & 4), "C" Filter at Output*	E_{NI}‡	V_{CC} = +10 V R_S = 5 kΩ A = 45 dB	12	–	1.7	6.4	μV	–
Equivalent Input Noise Voltage (Amplifiers 2 & 3) RIAA Compensated*	E_{N2}‡	V_{CC} = +10 V R_S = 5 kΩ A = 64 dB (1 kHz)	11	–	4	15.0	μV	–
Inter-Amplifier Audio Separation "Cross Talk"		V_{CC} = +12 V f = 1 kHz 0 dB = 0.78 V	13	–	<-45	–	dB	–
Inter-Amplifier Capacitance (Any amplifier output to any *other* amplifier input)	C	V_{CC} = +12 V f = 1 MHz	–	–	< 0.02	–	pF	–

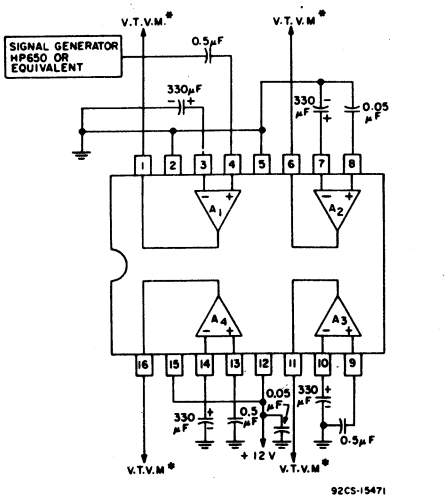
*Per IHF Standard Methods of Measurement for Audio Amplifiers IHF–A–201, 1966

‡ ac feedback included in test circuit



*Resistors are low noise precision, (1%) Metal Film type. Resistor values are in ohms; capacitance values are in microfarads, unless otherwise specified.

Fig. 12 - Test circuit for measurement of equivalent input noise voltage of amplifiers 1 and 4.



*V.T.V.M. - Hewlett-Packard Model 400D or equivalent.

Procedure:

1. Adjust Signal Generator for 0 dB output at reference terminal.
2. Read voltage at other output terminals (Figure shows terminal #1 used as reference).

Fig. 13 - Test circuit for measurement of inter-amplifier audio separation "cross talk" characteristic.

CA3058, CA3059, CA3079

Zero-Voltage Switches

For 50/60 and 400 Hz Thyristor Control Applications

The RCA-CA3058, CA3059, and CA3079 zero-voltage switches are monolithic silicon integrated circuits designed to control a thyristor in a variety of AC power switching applications for AC input voltages of 24 V, 120 V, 208/230 V, and 277 V at 50/60 and 400 Hz. Each of the zero-voltage switches incorporates 4 functional blocks (see Fig. 1) as follows:

1. Limiter-Power Supply—Permits operation directly from an AC line.
2. Differential On/Off Sensing Amplifier—Tests the condition of external sensors or command signals. Hysteresis or proportional-control capability may easily be implemented in this section.
3. Zero-Crossing Detector—Synchronizes the output pulses of the circuit at the time when the AC cycle is at zero voltage point; thereby eliminating radio-frequency interference (RFI) when used with resistive loads.
4. Triac Gating Circuit—Provides high-current pulses to the gate of the power controlling thyristor.

In addition, the CA3058 and CA3059 provide the following important auxiliary functions (see Fig. 1):

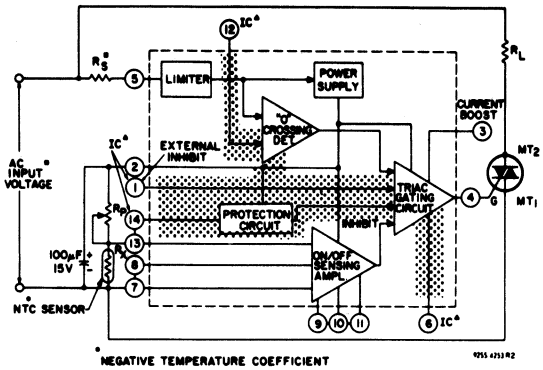
1. A built-in protection circuit that may be actuated to remove drive from the triac if the sensor opens or shorts.
2. Thyristor firing may be inhibited through the action of an internal diode gate connected to Terminal 1.
3. High-power dc comparator operation is provided by overriding the action of the zero-crossing detector. This is accomplished by connecting Terminal 12 to Terminal 7. Gate current to the thyristor is continuous when Terminal 13 is positive with respect to Terminal 9.

For an explanation of these functions see Operating Considerations. For detailed application information, see companion Application Note, ICAN-6182, "Features and Applications of RCA Integrated-Circuit Zero-Voltage Switches (CA3058, CA3059, and CA3079)".

The CA3058 is supplied in a hermetic 14-lead dual-in-line ceramic package. Types CA3059 and CA3079 are supplied in 14-lead dual-in-line plastic packages.

Applications:

- **Relay control**
- **Heater control**
- **Valve control**
- **Lamp control**
- **Synchronous switching of flashing lights**
- **On-off motor switching**
- **Differential comparator with self-contained power supply for industrial applications**
- **Photosensitive control**
- **Power one-shot control**



● NEGATIVE TEMPERATURE COEFFICIENT

AC Input Voltage (50/60 or 400 Hz) V AC	Input Series Resistor (R_S) k Ω	Dissipation Rating for R_S W
24	2	0.5
120	10	2
208/230	20	4
277	25	5

NOTE:
Circuitry, within shaded areas, not included in CA3079

■ See chart

▲ IC = Internal Connection - - DO NOT USE (Terminal Restriction applies only to CA3079).

Fig. 1—Functional block diagram of CA3058, CA3059, and CA3079.

Features	CA3058	CA3059	CA3079
■ 24V, 120V, 208/230V, 277V at 50 60, or 400 Hz operation	√	√	√
■ Differential Input	√	√	√
■ Low Balance Input Current (max.) -μA	1	1	2
■ Built-in Protection Circuit for opened or shorted sensor (Term. 14)	√	√	
■ Sensor Range (R_X) - kΩ	2 to 100	2 to 100	2 to 50
■ DC Mode (Term 12)	√	√	
■ External Trigger (Term. 6)	√	√	
■ External Inhibit (Term. 1)	√	√	
■ DC Supply Volts (max.)	14	14	10
■ Operating Temperature Range - °C		−55 to +125	

MAXIMUM RATINGS,
Absolute-Maximum Values at T_A = 25°C

DC SUPPLY VOLTAGE (BETWEEN TERMS. 2 AND 7):
CA3058, CA3059 ..... 14 V
CA3079 ..... 10 V
DC SUPPLY VOLTAGE (BETWEEN TERMS. 2 AND 8):
CA3058, CA3059 ..... 14 V
CA3079 ..... 10 V
PEAK SUPPLY CURRENT (TERMS. 5 AND 7)
..... ±50 mA
OUTPUT PULSE CURRENT (TERM. 4)
..... 150 mA

POWER DISSIPATION:
Up to T_A=75°C – CA3058 ..... 700 mW
Up to T_A=55°C – CA3059,CA3079 ... 700 mW
Above T_A=75°C – CA3058
..... Derate Linearly 8 mW/°C
Above T_A=55°C – CA3059,CA3079
..... Derate linearly 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:
Operating ..... −55 to +125°C
Storage ..... −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At a distance 1/16" ± 1/32" (1.59 ± 0.79 mm)
from case for 10 seconds max. ..... +265°C

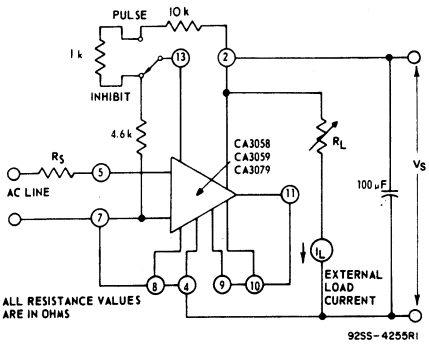


Fig. 2(a)—DC supply voltage test circuit for CA3058, CA3059, and CA3079.

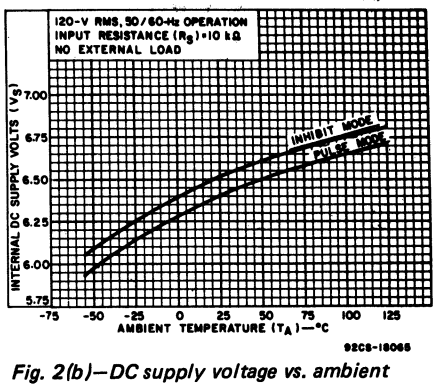


Fig. 2(b)—DC supply voltage vs. ambient temperature for CA3058, CA3059 and CA3079.

CA3058, CA3059, CA3079

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

TERMINAL NO.	1 Note 3	2	3	4	5 Note 1	6 Note 3	7	8	9	10	11	12 Note 3	13	14 Note 2,3	MAXIMUM CURRENT RATINGS I_{IN} mA	I_{OUT} mA
1 Note 3		*	*	*	*	15 0	10 -2	*	*	*	*	*	*	*	10	0.1
2			0 -15	0 -15	2 -14	0 -14	0 ▲ -14	0 ▲ -14	0 -14	0 -14	0 -14	* .	0 -14	0 -14	150	10
3				0 -15	*	*	*	*	*	*	*	*	*	*	*	*
4					*	2 -10	*	*	*	*	*	*	*	*	0.1	150
5 Note 1						*	7 -7	*	*	*	*	*	*	*	50	10
6 Note 3							14 0	*	*	*	*	*	*	*	*	*
7								*	14 0	*	20 0	2.5 -2.5	14 0	6 -6	*	*
8									10 0	*	*	*	*	*	0.1	2
9										*	*	*	*	*	*	*
10											*	*	*	*	*	*
11												*	*	*	*	*
12 Note 3													*	*	50	50
13														*	*	*
14 Note 3															2	2

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of horizontal Terminal 6 to vertical Terminal 4 is 2 to −10 volts.

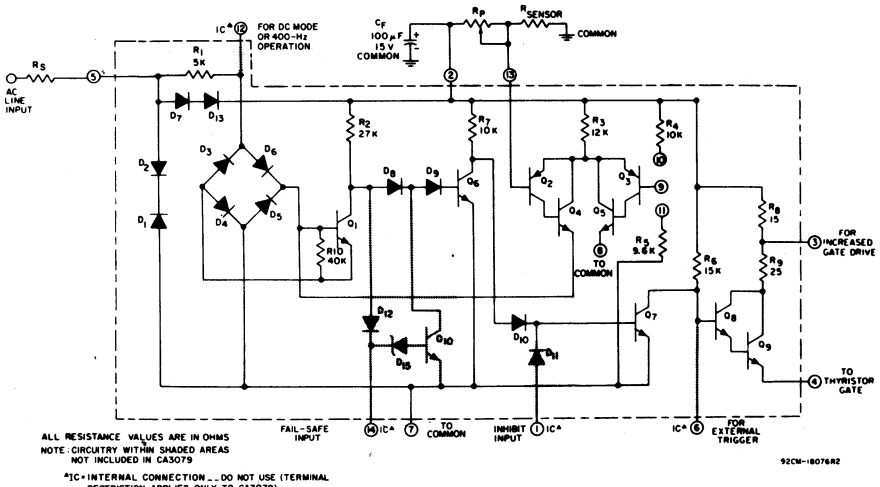
Note 1 – Resistance should be inserted between Terminal 5 and external supply or line voltage for limiting current into Terminal 5 to less than 50 mA.

Note 2 – Resistance should be inserted between Terminal 14 and external supply for limiting current into Terminal 14 to less than 2 mA.

Note 3 – For the CA3079 indicated terminal is internally connected and, therefore, should not be used.

▲For CA3079 (0 to −10 V).

*Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.



▲IC• INTERNAL CONNECTION ... DO NOT USE (TERMINAL RESTRICTION APPLIES ONLY TO CA3079)

Fig. 4—Schematic diagram of CA3058, CA3059, and CA3079.

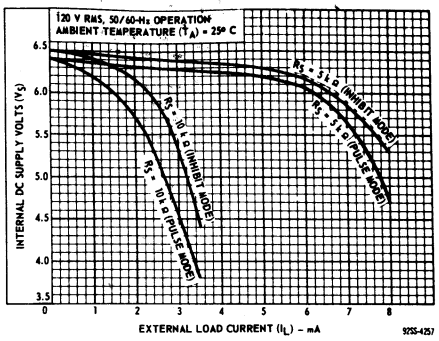


Fig. 2(c)—DC supply voltage vs. external load —current for CA3058, CA3059, and CA3079.

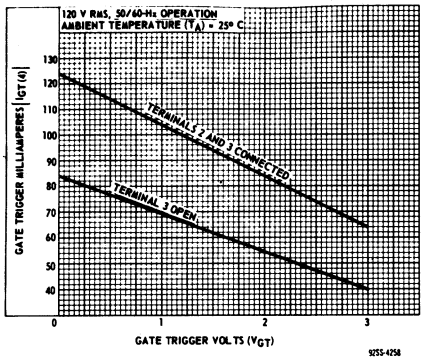
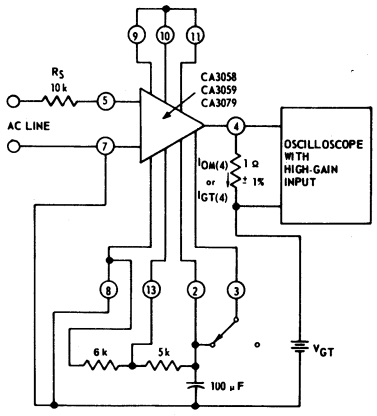


Fig. 3—Gate trigger current vs. gate trigger voltage for CA3058, CA3059, and CA3079.



ALL RESISTANCE VALUES ARE IN OHMS

Fig. 5(a)—Peak output (pulsed) and gate trigger current with internal power supply test circuit for CA3058, CA3059, and CA3079.

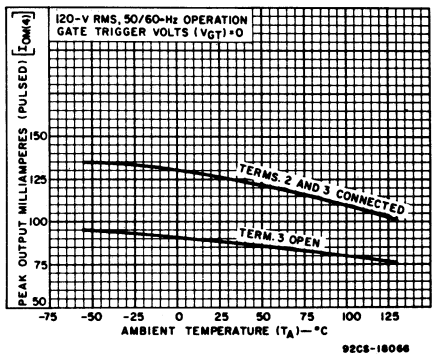


Fig. 5(b)—Peak output current (pulsed) vs. ambient temperature for CA3058, CA3059, and CA3079.

CA3058, CA3059, CA3079

ELECTRICAL CHARACTERISTICS (For all types, unless indicated otherwise)
All voltages are measured with respect to Terminal 7.

CHARACTERISTIC	TEST CONDITIONS $T_A = 25^oC$ (Unless Indicated Otherwise)	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
For Operating at 120 V rms, 50-60 Hz (AC Line Voltage)●					
DC Supply Voltage, V_S Inhibit Mode					
At 50/60 Hz	$R_S = 8\ k\Omega$, $I_L = 0$	6.1	6.5	7	V
At 400 Hz	$R_S = 10\ k\Omega$, $I_L = 0$	–	6.8	–	V
At 50/60 Hz	$R_S = 5\ k\Omega$, $I_L = 2$ mA	–	6.4	–	V
Pulse Mode					
At 50/60 Hz	$R_S = 8\ k\Omega$, $I_L = 0$	6	6.4	7	V
At 400 Hz	$R_S = 10\ k\Omega$, $I_L = 0$	–	6.7	–	V
At 50/60 Hz	$R_S = 5\ k\Omega$, $I_L = 2$ mA	–	6.3	–	V
At 50/60 Hz (CA3058) *See Fig. 2*	$R_S = 8\ k\Omega$, $I_L = 0$, $T_A = -55$ to $+125^oC$	5.5	–	7.5	V
Gate Trigger Current, I_{GT}(4) *See Figs. 3, 5(a)*	Terms. 3 and 2 connected, $V_{GT} = 1$ V	–	105	–	mA
Peak Output Current (Pulsed), I_{OM}(4)	Term. 3 open, Gate Trigger Voltage (V_{GT}) = 0	50	84	–	mA
With Internal Power Supply	Terms. 3 and 2 connected, Gate Trigger Voltage (V_{GT})=0	90	124	–	mA
	Term. 3 open, V^+=12 V, V_{GT}=0	–	170	–	mA
With External Power Supply *See Figs. 5, 6*	Terms. 3 and 2 connected, V^+=12 V, $V_{GT} = 0$	–	240	–	mA
Inhibit Input Ratio, V_9/V_2 All Types	Voltage Ratio of Term. 9 to 2	0.465	0.485	0.520	–
CA3058 *See Fig. 7*	$T_A = -55$ to $+125^oC$	0.450	–	0.520	–
Total Gate Pulse Duration:* For positive dv/dt, t_P					
50-60 Hz	$C_{EXT} = 0$	70	100	140	μs
400 Hz	$C_{EXT} = 0$, $R_{EXT} = \infty$	–	12	–	μs
For negative dv/dt, t_N					
50-60 Hz	$C_{EXT} = 0$	70	100	140	μs
400 Hz *See Fig. 8*	$C_{EXT} = 0$, $R_{EXT} = \infty$	–	10	–	μs
Pulse Duration After Zero Crossing (50-60 Hz): For positive dv/dt, t_{P1}	$C_{EXT} = 0$, $R_{EXT} = \infty$	–	50	–	μs
For negative dv/dt, t_{N1} *See Fig. 8*		–	60	–	μs
Output Leakage Current, I_4 Inhibit Mode: All Types		–	0.001	10	μA
CA3058 *See Fig. 9*	$T_A = -55$ to $+125^oC$	–	–	20	μA
Input Bias Current, I_I CA3058, CA3059		–	220	1000	nA
CA3079 *See Fig. 10*		–	220	2000	nA

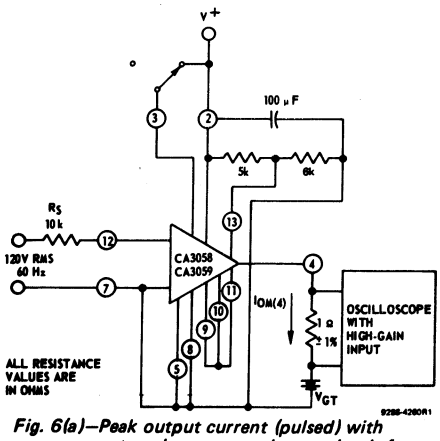


Fig. 6(a)—Peak output current (pulsed) with external power supply test circuit for CA3058 and CA3059.

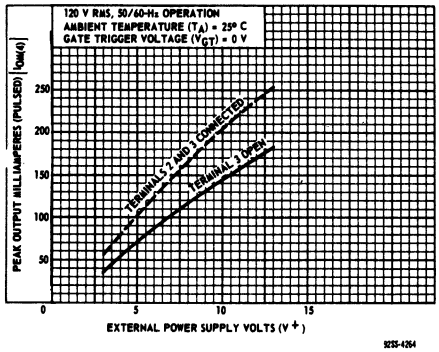


Fig. 6(b)—Peak output current (pulsed) vs. external power supply voltage for CA3058 and CA3059.

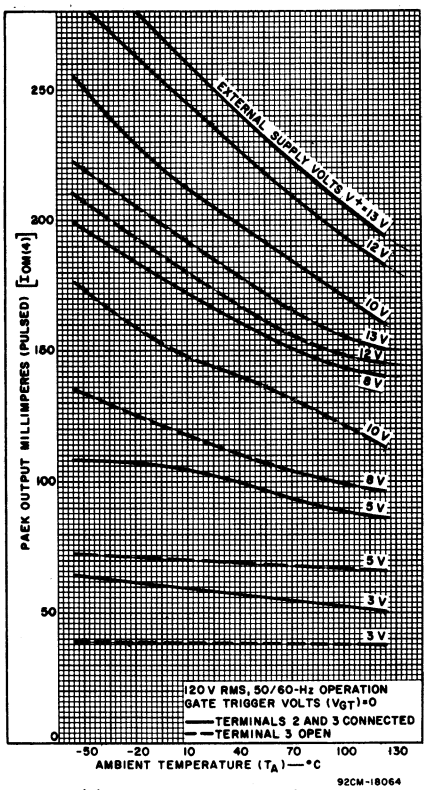


Fig. 6(c)—Peak output current (pulsed) vs. ambient temperature for CA3058 and CA3059.

CA3058, CA3059, CA3079

ELECTRICAL CHARACTERISTICS (For all types, unless indicated otherwise) (Cont'd)
All voltages are measured with respect to Terminal 7.

CHARACTERISTIC	TEST CONDITIONS T_A = 25°C (Unless Indicated Otherwise)	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
For Operating at 120 V rms, 50-60 Hz (AC Line Voltage)●					
Common-Mode Input Voltage Range, V_{CMR}	Terms. 9 and 13 connected	–	1.5 to 5	–	V
Sensitivity, ΔV_{13}≠ (Pulse Mode) *See Figs. 5(a), 12*	Term. 12 open	–	6	–	mV

≠Required voltage change at Term. 13 to either turn OFF the triac when ON or turn ON the triac when OFF.

*Pulse duration in 50 Hz applications is approximately 15% longer than shown in Fig. 8(b).

● The values given in the Electrical Characteristics Chart at 120 V also apply for operation at input voltages of 24 V, 208/230 V, and 277 V, except for Pulse Duration. However, the series resistor (R_S) must have the indicated value, shown in the chart in Fig. 1, for the specified input voltage.

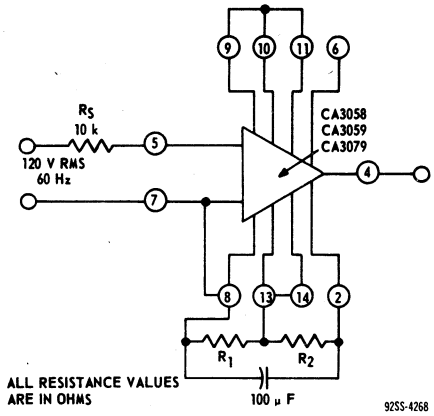


Fig. 7(a)—Input inhibit voltage ratio test circuit for CA3058, CA3059, and CA3079.

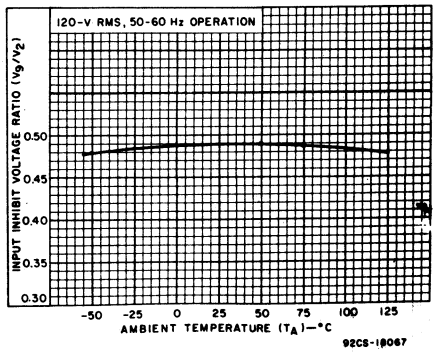


Fig. 7(b)—Input inhibit voltage ratio vs. ambient temperature for CA3058, CA3059, and CA3079.

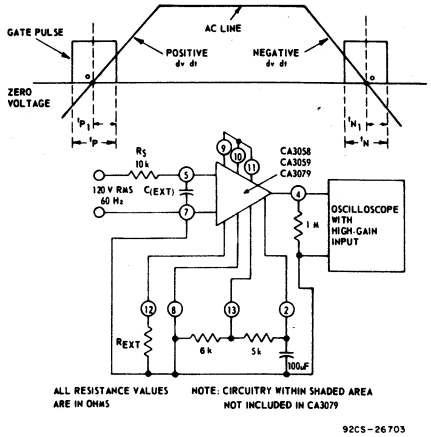


Fig. 8(a)—Gate pulse duration test circuit with associated waveform for CA3058, CA3059, and CA3079.

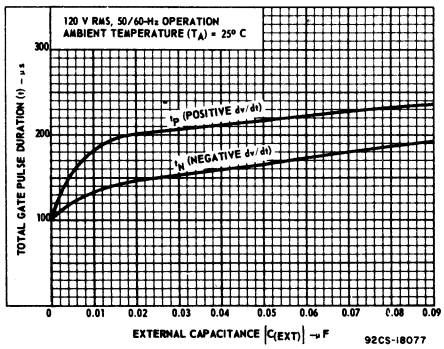


Fig. 8(b)—Total gate pulse duration vs. external capacitance for CA3058, CA3059, and CA3079.

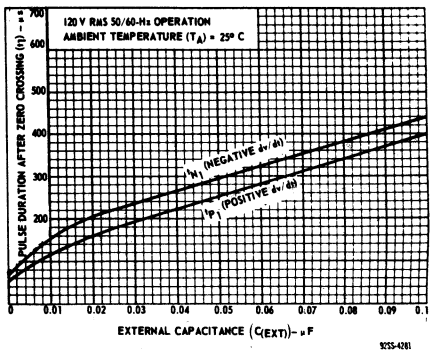


Fig. 8(c)—Pulse duration after zero crossing vs. external capacitance for CA3058, CA3059, and CA3079.

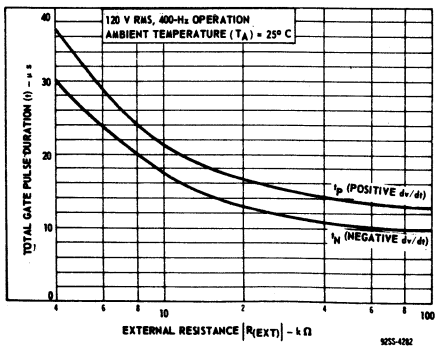


Fig. 8(d)—Total gate pulse duration vs. external resistance for CA3058 and CA3059.

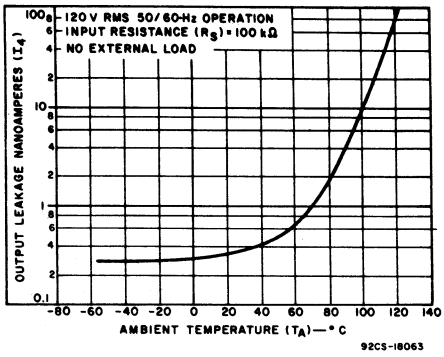


Fig. 9—Output leakage current (inhibit mode) vs. ambient temperature for CA3058, CA3059, and CA3079.

CA3058, CA3059, CA3079

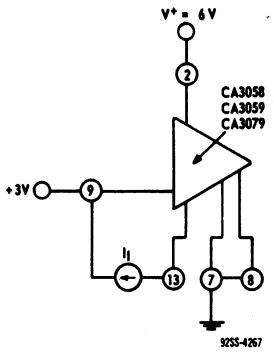


Fig. 10—Input bias current test circuit for CA3058, CA3059, and CA3079.

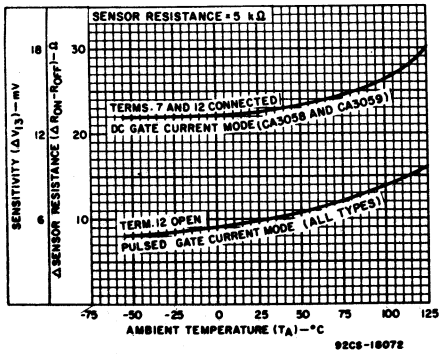


Fig. 12—Sensitivity vs. ambient temperature for CA3058, CA3059, and CA3079.

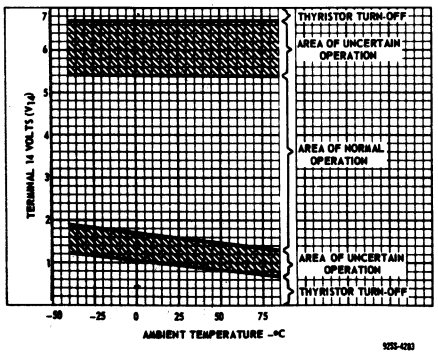


Fig. 13—Operating regions for built-in protection circuit for CA3058 and CA3059.

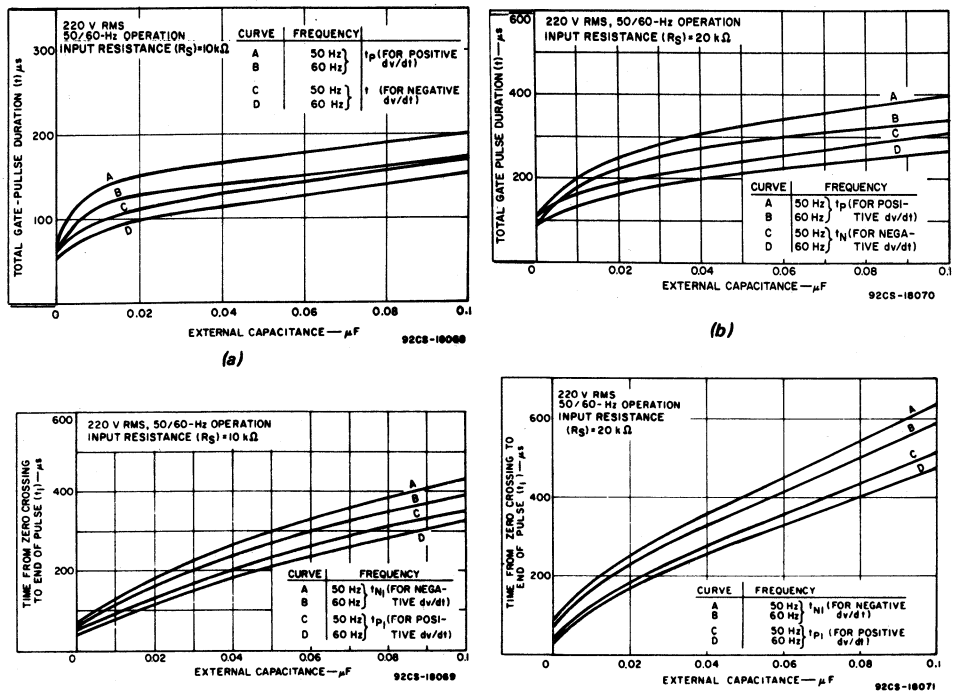


Fig. 11—Relative pulse width and location of zero crossing for 220-volt operation for CA3058, CA3059, and CA3079.

OPERATING CONSIDERATIONS

Power Supply Considerations for CA3058, CA3059, and CA3079

The CA3058, CA3059, and CA3079 are intended for operation as self-powered circuits with the power supplied from an AC line through a dropping resistor. The internal supply is designed to allow for some current to be drawn by the auxiliary power circuits. Typical power supply characteristics are given in Figs. 3(b) and 3(c).

Power Supply Considerations for CA3058 and CA3059

The output current available from the internal supply may not be adequate for higher power applications. In such applications an external power supply with a higher voltage should be used with a resulting increase in the output level. (See Fig. 5 for the peak output current characteristics). When an external power supply is used, Terminal 5 should be connected to Terminal 7 and the synchronizing voltage applied to Terminal 12 as illustrated in Fig. 5(a).

Operation of Built-in Protection for the CA3058, CA3059

A special feature of the CA3058 and CA3059 is the inclusion of a protection circuit which, when connected, removes power from the load if the sensor either shorts or opens. The protection circuit is activated by connecting Terminal 14 to Terminal 13 as shown in Fig. 1. To assure proper operation of the protection circuit the following conditions should be observed:

1. Use the internal supply and limit the external load current to 2 mA with a 5 kΩ dropping resistor.
2. Set the value of R_P and sensor resistance (R_X) between 2 kΩ and 100 kΩ.
3. The ratio of R_X to R_P, typically, should be greater than 0.33 and less than 3. If either of these ratios is not met with an unmodified sensor over the entire anticipated temperature range, then either a series or shunt resistor must be added to avoid undesired activation of the circuit.

If operation of the protection circuit is desired under conditions other than those specified above, then apply the data given in Fig. 13.

External Inhibit Function for the CA3058 and CA3059

A priority inhibit command may be applied to Terminal 1. The presence of at least +1.2 V at 10 μA will remove drive from the thyristor. This required level is compatible with DTL or T^2L logic. A logical 1 activates the inhibit function.

DC Gate Current Mode for the CA3058 and CA3059

Connecting Terminals 7 and 12 disables the zero-crossing detector and permits the flow of gate current on demand from the differential sensing amplifier. This mode of operation is useful when comparator operation is desired or when inductive loads are switched. Care must be exercised to avoid overloading the internal power supply when operating in this mode. A sensitive gate thyristor should be used with a resistor placed between Terminal 4 and the gate in order to limit the gate current.