CA3060, CA3060A Types

Operational Transconductance Amplifier Arrays

APPLICATIONS

- **For low power conventional operational amplifier applications**
- **Active filters**
- **Comparators**
- **Gyrators**
- **Mixers**
- **Modulators**
- **Multiplexers**
- **Multipliers**
- **Strobing and gating functions**
- **Sample and hold functions**

FEATURES

- **Low power consumption — as low as 100 μW per amplifier**
- **Independent biasing for each amplifier**
- **High forward transconductance**
- **Programmable range of input characteristics**
- **Low input bias and input offset current**
- **High input and output impedance**
- **No effect on device under output short-circuit conditions**
- **Zener diode bias regulator**

RCA-CA3060AD, CA3060BD, CA3060D, and CA3060E, monolithic integrated circuits, are arrays of three independent Operational Transconductance Amplifiers. This type of amplifier is a new circuit concept that has the generic characteristics of an operational voltage amplifier with the exception that the forward gain characteristic is best described by transconductance rather than voltage gain (open-loop voltage gain is the product of the transconductance and the load resistance, $g_m R_L$). When operated into a suitable load resistor and with provisions for feedback, these amplifiers are well suited for a wide variety of operational-amplifier and related applications. In addition, the extremely high output impedance makes these types particularly well suited for service in active filters.

The three amplifiers in the CA3060 family are identical push-pull Class A types which can be independently biased to achieve a wide range of characteristics for specific applications. The electrical characteristics of each amplifier are a function of the amplifier bias current (I_{ABC}). This feature offers the system designer maximum flexibility with regard to output current capability, power consumption, slew rate, input resistance, input bias current, and input offset current. The linear variation of the parameters with respect to bias and the ability to maintain a constant dc level between input and output of each amplifier also makes the CA3060 suitable for a variety of non-linear applications such as mixers, multipliers, and modulators.

In addition; the types in the CA3060 family incorporate a unique Zener diode regulator system that permits current regulation below supply voltages normally associated with such systems.

Generic applications of the OTA are described in ICAN-6668, Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers.

The CA3060AD, CA3060BD, and CA3060D are supplied in a hermetic 16-lead dual-in-line ceramic package which can be operated over the full military temperature range, -55°C to +125°C. The CA3060E is supplied in a 16-lead dual-in-line plastic package and is operational from -40°C to +85°C.

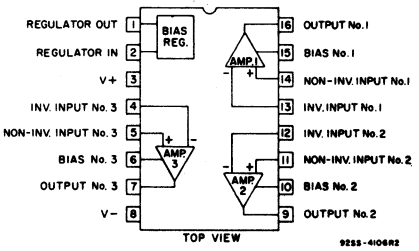


Fig. 1—Functional block diagram for each type in the CA3060 family.

MAXIMUM RATINGS, *Absolute Maximum Values at T_A = 25°C*

DC Supply Voltage (between V^+ and V^- terminals):
- CA3060AD, CA3060BD, CA3060E ..... 36V (±18V)
- CA3060D ..... 14 V (±7V)

Differential Input Voltage (each amplifier):
- CA3060AD, CA3060BD, CA3060E ..... ±5V
- CA3060D ..... ±5V

DC Input Voltage ..... V^+ to V^-

Input Signal Current (each amplifier of each type): ..... ±1 mA

Amplifier Bias Current (each amplifier of each type) ..... 2 mA

Bias Regulator Input Current ..... 5 mA

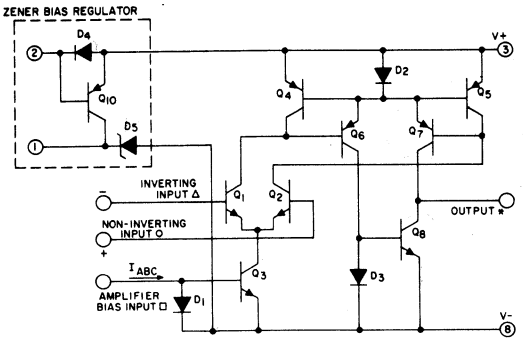
Output Short-Circuit Duration* ..... No limitation

*Short circuit may be applied to ground or to either supply.

Device Dissipation:
- Total Package of each type up to T_A = 75°C ..... 490 mW
- Above T_A = 75°C ..... Derate linearly 6.67 mW/°C

Temperature Range:
- Operating —
  - CA3060AD, CA3060BD, CA3060D ..... -55 to +125°C
  - CA3060E ..... -40 to +85°C
- Storage —
  - CA3060AD, CA3060BD, CA3060D, CA3060E ..... -65 to +150°C

Lead Temperature (During Soldering):
- At distance 1/16 ±1/32 in. (1.59 ±0.79 mm) from case for 10s max ..... +300°C



Δ INVERTING INPUT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 13, 12 AND 4, RESPECTIVELY
○ NON-INVERTING INPUT OF AMPLIFIERS 1, 2, AND 3 IS TERMINAL Nos. 14, 11, AND 5, RESPECTIVELY
* OUTPUT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 16, 9, AND 7, RESPECTIVELY
□ AMPLIFIER BIAS CURRENT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 15, 10, AND 6, RESPECTIVELY

92CS-15860R1

Fig. 2—Simplified schematic diagram showing bias regulator and one operational transconductance amplifier for each type of the CA3060 family.

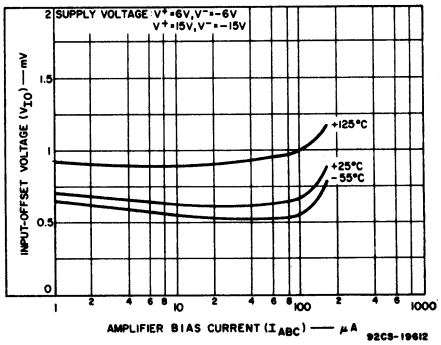


Fig. 3—Input offset voltage vs. amplifier bias current.

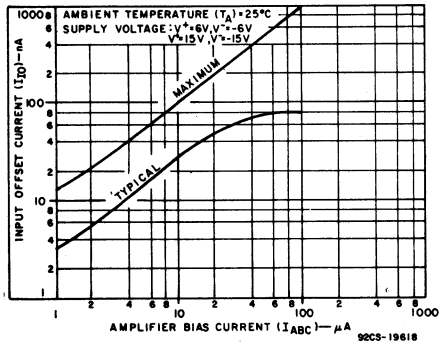


Fig. 4—Input offset current vs. amplifier bias current.

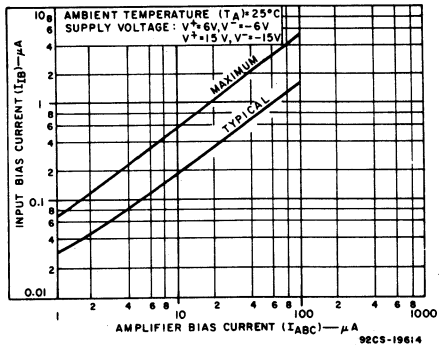


Fig. 5a—Input bias current vs. amplifier bias current

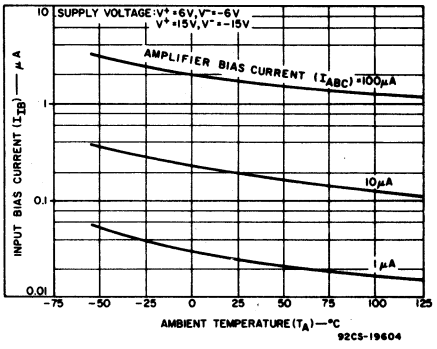


Fig. 5b—Input bias current vs. ambient temperature.

CA3060, CA3060A Types

ELECTRICAL CHARACTERISTICS (CA3060D)
For each amplifier at T_A = 25°C, V^+ = 6 V, V^- = -6 V

CHARACTERISTIC	SYMBOL	TYPICAL CHARACTERISTICS CURVES Fig.	LIMITS — Amplifier Bias Current I_{ABC} = 1 μA MIN.	TYP.	MAX.	I_{ABC} = 10 μA MIN.	TYP.	MAX.	I_{ABC} = 100 μA MIN.	TYP.	MAX.	UNITS
STATIC CHARACTERISTICS												
Input Offset Voltage	V_{IO}	3	–	1	5	–	1	5	–	1	5	mV
Input Offset Current	I_{IO}	4	–	3	14	–	30	100	–	250	1000	nA
Input Bias Current	I_{IB}	5a, b	–	33	70	–	300	550	–	2500	5000	nA
Peak Output Current	I_{OM}	6a, b	1.3	2.3	–	15	26	–	150	240	–	μA
Peak Output Voltage: Positive	V_{OM^+}	7	4.6	5	–	4.5	4.8	–	4.5	4.7	–	V
Peak Output Voltage: Negative	V_{OM^-}	7	5.8	5.95	–	5.8	5.95	–	5.7	5.9	–	V
Amplifier Supply Current (each amplifier)	I_A	8a, b	–	8.5	14	–	85	120	–	850	1200	μA
Power Consumption (each amplifier)	P	–	–	0.10	0.17	–	1	1.45	–	10	14.5	mW
Input Offset-Voltage Sensitivity■: Positive	$\Delta V_{IO}/\Delta V^+$	–	–	1.5	120	–	2	120	–	2	120	μV/V
Input Offset-Voltage Sensitivity■: Negative	$\Delta V_{IO}/\Delta V^-$	–	–	20	120	–	20	120	–	30	120	μV/V
Amplifier Bias Voltage*	V_{ABC}	9	–	0.54	–	–	0.60	–	–	0.66	–	V
DYNAMIC CHARACTERISTICS (at 1 kHz unless specified otherwise)												
Forward Transconductance (large signal)	g_{21}	10a, b	0.3	1.55	–	3	18	–	30	102	–	mmho
Common-Mode Rejection Ratio	CMRR	–	70	110	–	70	110	–	70	90	–	dB
Common-Mode Input-Voltage Range	V_{ICR}	–	4.4 to -5.1 min. 4.7 to -5.3 typ.			4.3 to -5 min. 4.6 to -5.2 typ.			4.3 to -5 min. 4.6 to -5.2 typ.			V
Slew Rate (Test ckt., Fig. 13	SR		–	0.1	–	–	1	–	–	8	–	V/μs
Open-Loop (g_{21}) Bandwidth	BW_{OL}	11	–	20	–	–	45	–	–	110	–	kHz
Input Impedance Components: Resistance	R_I	12	800	1600	–	90	170	–	10	20	–	kΩ
Input Impedance Components: Capacitance at 1 MHz	C_I	–	–	2.7	–	–	2.7	–	–	2.7	–	pF
Output Impedance Components: Resistance	R_O	14	–	200	–	–	20	–	–	2	–	MΩ
Output Impedance Components: Capacitance at 1 MHz	C_O	–	–	4.5	–	–	4.5	–	–	4.5	–	pF
ZENER BIAS REGULATOR CHARACTERISTICS (at T_A = 25°C, I_Z = 0.1 mA)						MIN.	TYP.	MAX.				
Voltage	V_Z	15	Temp. Coeff. = 3 mV/°C			6.2	6.7	7.9				V
Impedance	Z_Z	–					200	300				Ω

* Temperature-Coefficient; -2.2 mV/°C (at V_{ABC} = 0.54 V, I_{ABC} = 1 μA; -2.1 mV/°C (at V_{ABC} = 0.060 V, I_{ABC} = 10 μA); -1.9 mV/°C (at V_{ABC} = 0.66 V, I_{ABC} = 100 μA)

■ Conditions for Input Offset Voltage and Supply Sensitivity:
(a) Bias current derived from the regulator with an appropriate resistor connected from terminal No. 1 to the bias terminal on the amplifier under test —
V^+ is reduced to 5 volts for V^+ sensitivity
V^- is reduced to -5 volts for V^- sensitivity

(b) V^+ sensitivity in μV/V = $\frac{\text{Voffset - Voffset for +5 V and -6 V supplies}}{\text{1 volt}}$

V^- sensitivity in μV/V = $\frac{\text{Voffset - Voffset for -5 V and +6 V supplies}}{\text{1 volt}}$

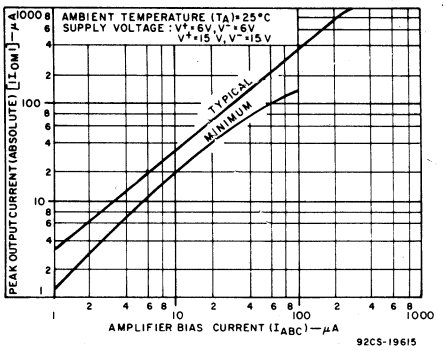


Fig.6a—Peak output current vs. amplifier bias current.

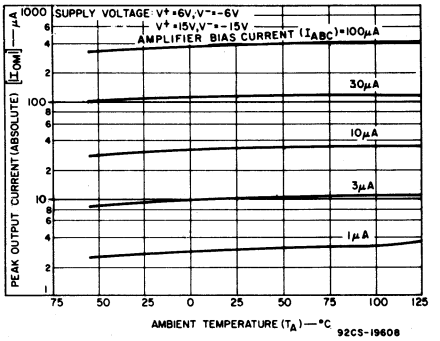


Fig.6b—Peak output current vs. ambient temperature.

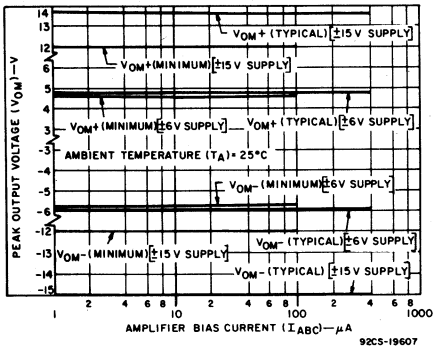


Fig.7—Peak output voltage vs. amplifier bias current.

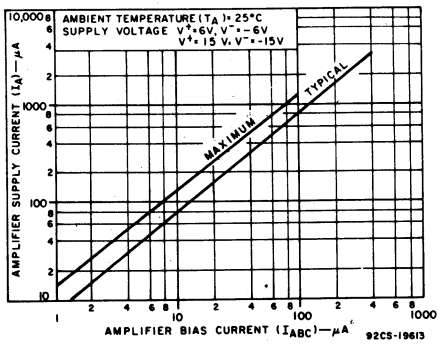


Fig.8a—Amplifier supply current (each amplifier) vs. amplifier bias current.

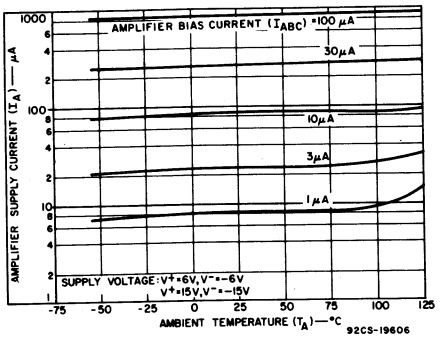


Fig.8b—Amplifier supply current (each amplifier) vs. ambient temperature.

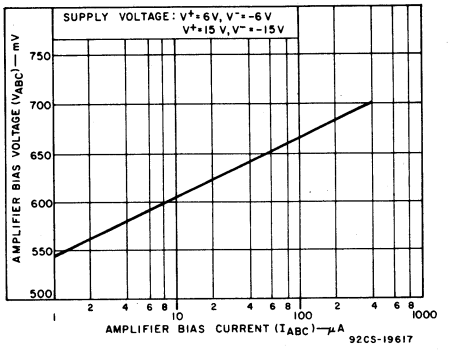


Fig.9—Amplifier bias voltage vs. amplifier bias current.

CA3060, CA3060A Types

ELECTRICAL CHARACTERISTICS (CA3060AD, CA3060BD, CA3060E)
For each amplifier at T_A = 25°C, V^+ = 15 V, V^- = -15 V

CHARACTERISTIC	SYMBOL	TYPICAL CHARACTERISTICS CURVE Fig.	LIMITS — Amplifier Bias Current I_{ABC} = 1 μA MIN.	TYP.	MAX.	I_{ABC} = 10 μA MIN.	TYP.	MAX.	I_{ABC} = 100 μA MIN.	TYP.	MAX.	UNITS
			CA3060BD						CA3060AD CA3060BD CA3060E			
STATIC CHARACTERISTICS												
Input Offset Voltage	V_{IO}	3	–	1	5	–	1	5	–	1	5	mV
Input Offset Current	I_{IO}	4	–	3	14	–	30	100	–	250	1000	nA
Input Bias Current	I_{IB}	5a,b	–	33	70	–	300	550	–	2500	5000	nA
Peak Output Current	I_{OM}	6a,b	1.3	2.3		15	26	–	150	240	–	μA
Peak Output Voltage: Positive	V_{OM^+}	7	12	13.6	–	12	13.6	–	12	13.6	–	V
Negative	V_{OM^-}		12	14.7	–	12	14.7	–	12	14.7	–	
Amplifier Supply Current (each amplifier)	I_A	8a,b	–	8.5	14	–	85	120	–	850	1200	μA
Power Consumption (each amplifier)	P	–	–	0.26	0.42	–	2.6	3.6	–	26	36	mW
Input Offset-Voltage Sensitivity■: Positive	$\Delta V_{IO}/\Delta V^+$	–	–	1.5	150	–	2	150	–	2	150	μV/V
Negative	$\Delta V_{IO}/\Delta V^-$		–	20	150	–	20	150	–	30	150	
Amplifier Bias Voltage*	V_{ABC}	9	–	0.54	–	–	0.60	–	–	0.66	–	V
DYNAMIC CHARACTERISTICS (at 1 kHz unless specified otherwise)												
Forward Transconductance (large signal)	g_{21}	10a,b	0.3	1.55	–	3	18	–	30	102	–	mmho
Common-Mode Rejection Ratio	CMRR	–	70	110	–	70	110	–	70	90	–	dB
Common-Mode Input Voltage Range	V_{ICR}	–	+12 to -12 min. +13 to -14 typ.			+12 to -12 min. +13 to -14 typ.			+12 to -12 min. +13 to -14 typ.			V
Slew Rate (Test ckt., Fig. 13)	SR	–	–	0.1	–	–	1	–	–	8	–	V/μs
Open-Loop (g_{21}) Bandwidth	BW_{OL}	11	–	20	–	–	45	–	–	110	–	kHz
Input Impedance Components: Resistance	R_I	12	800	1600	–	90	170	–	10	20	–	kΩ
Capacitance at 1 MHz	C_I		–	2.7	–	–	2.7	–	–	2.7	–	pF
Output Impedance Components: Resistance	R_O	14	–	200	–	–	20	–	–	2	–	MΩ
Capacitance at 1 MHz	C_O	–	–	4.5	–	–	4.5	–	–	4.5	–	pF
ZENER BIAS REGULATOR CHARACTERISTICS (at T_A=25°C, I_Z = 0.1 mA)				MIN.	TYP.	MAX.						
Voltage	V_Z	15	Temp. Coeff. = 3 mV/°C	6.2	6.7	7.9						V
Impedance	Z_Z	–			200	300						Ω

* Temperature-Coefficient; -2.2 mV/°C (at V_{ABC} = 0.54 V, I_{ABC} = 1 μA; -2.1 mV/°C (at V_{ABC} = 0.060 V, I_{ABC} = 10 μA); -1.9 mV/°C (at V_{ABC} = 0.66 V, I_{ABC} = 100 μA)

■ Conditions for Input Offset Voltage and Supply Sensitivity:
(a) Bias current derived from the regulator with an appropriate resistor connected from terminal No. 1 to the bias terminal on the amplifier under test ---
V^+ is reduced to 13 volts for V^+ sensitivity
V^- is reduced to −13 volts for V^- sensitivity

(b) V^+ sensitivity in μV/V = $\frac{\text{Voffset} \cdot \text{Voffset for +13 V and −15 V supplies}}{\text{1 volt}}$

V^- sensitivity in μV/V = $\frac{\text{Voffset} \cdot \text{Voffset for −13 V and +15 V supplies}}{\text{1 volt}}$

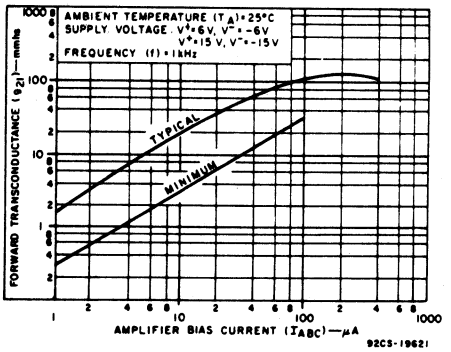


Fig. 10a—Forward transconductance vs. amplifier bias current.

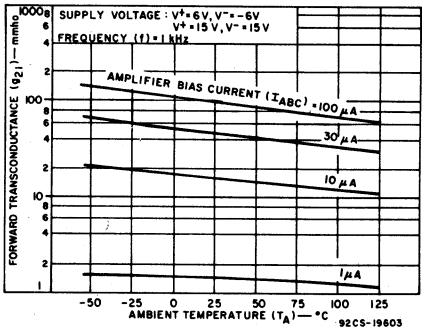


Fig. 10b—Forward transconductance vs. ambient temperature.

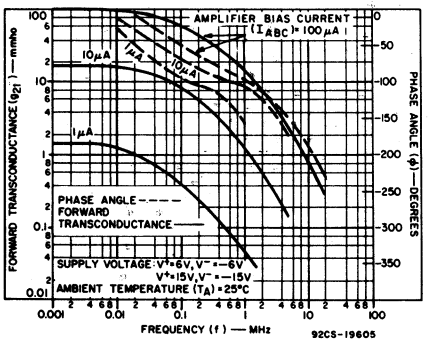


Fig. 11—Forward transconductance vs. frequency.

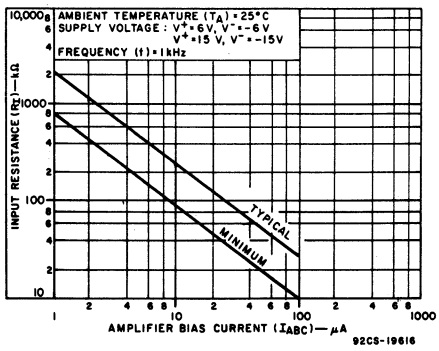
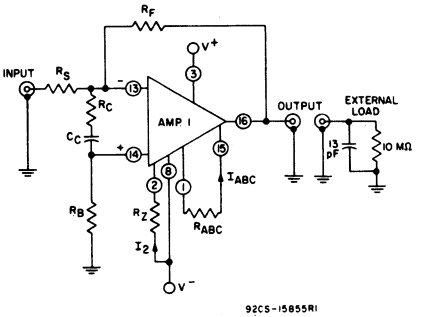


Fig. 12—Input resistance vs. amplifier bias current.



V_Z is measured between terminals 1 and 8.

V_{ABC} is measured between terminals 15 and 8.

$$R_Z = \frac{[(V^+)-(V^-)-0.7]}{I_2}, \quad R_{ABC} = \frac{V_Z \cdot V_{ABC}}{I_{ABC}}$$

Supply Voltage: for both ±6 V and ±15 V.

TYPICAL SLEW RATE TEST CIRCUIT PARAMETERS

I_{ABC}	SLEW RATE	I_2	R_{ABC}	R_S	R_F	R_B	R_C	C_C
μA	V/μs	μA	ohms					μF
100	8	200	62 k	100k	100k	51k	100	0.02
10	1	200	620k	1M	1M	510k	1k	0.005
1	0.1	2	6.2M	10M	10M	5.1M	∞	0

Fig. 13—Slew rate test circuit for amplifier No. 1 of CA3060.

CA3060, CA3060A Types

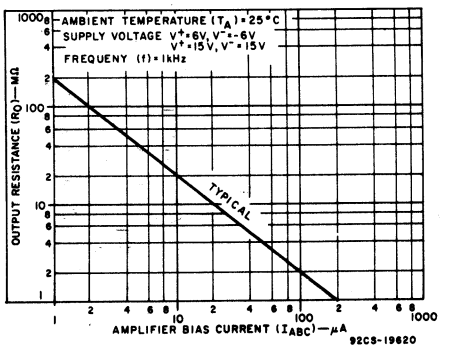


Fig.14—Output resistance vs. amplifier bias current.

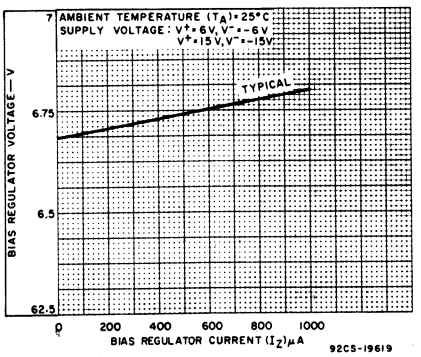


Fig.15—Bias regulator voltage vs. bias regulator current.

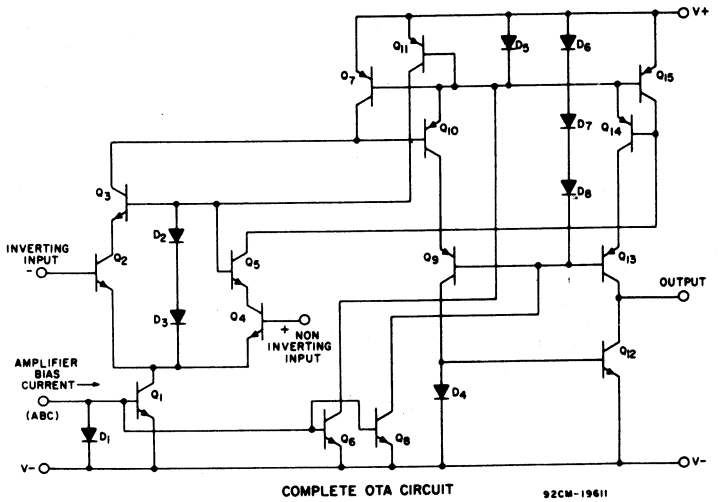


Fig.16 – Complete schematic diagram showing one of the three operational transconductance amplifiers.

OPERATING CONSIDERATIONS

The CA3060 consists of three operational amplifiers similar in form and application to conventional operational amplifiers but sufficiently different from the standard operational amplifier (op-amp) to justify some explanation of their characteristics. The amplifiers incorporated in the CA3060 are best described by the term Operational Transconductance Amplifier (OTA). The characteristics of an ideal OTA are similar to those of an ideal op-amp except that the OTA has an extremely high output impedance. Because of this inherent characteristic the output signal is best defined in terms of current which is proportional to the difference between the voltages of the two input terminals. Thus, the transfer characteristic is best described in terms of transconductance rather than voltage gain. Other than the difference given above, the characteristics tabulated on pages 3 and 4 of this data bulletin are similar to those of any typical op-amp.

The OTA circuitry incorporated in the CA3060 (See Fig. 16) provides the equipment designer with a wider variety of circuit arrangements than does the standard op-amp; because as the curves in the data bulletin indicate, the user may select the optimum circuit conditions for a specific application simply by varying the bias conditions of each amplifier. If low power consumption, low bias, and low offset current, or high input impedance are primary design requirements, then low current operating conditions may be selected. On the other hand, if operation into a moderate load impedance is the primary consideration, then higher levels of bias may be used.

Bias Considerations for Op-Amp Applications

The operational transconductance amplifiers allow the circuit designer to select and control the operating conditions of the circuit merely by the adjustment of the input bias current I_{ABC}. This enables the designer to have complete control over transconductance, peak output current and total power consumption independent of supply voltage.

In addition, the high output impedance makes these amplifiers ideal for applications where current summing is involved.

The design of a typical operational amplifier circuit (See Fig. 17) would proceed as follows:

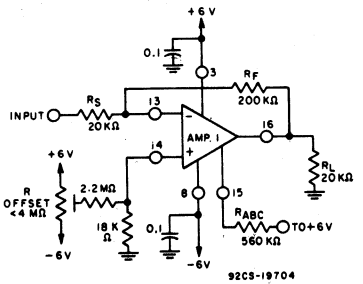


Fig.17—20-dB amplifier using the CA3060.

Circuit Requirements
Closed loop voltage gain = 10 (20 dB)
Offset voltage adjustable to zero
Current drain as low as possible
Supply voltage = ±6 V
Maximum input voltage = ±50 mV
Input resistance = 20 kΩ
Load resistance = 20 kΩ
Device: CA3060

Calculation

1. Required transconductance g_{21}.
   Assume that the open loop gain A_{OL} must be at least ten times the closed loop gain. Therefore, the forward transconductance required is given by

$$g_{21} = A_{OL}/R_L$$

$$= 100/18\ k\Omega$$

$$\cong 5.5\ mmho$$

(R_L = 20 kΩ in parallel with 200 kΩ

≅ 18 kΩ)

2. Selection of suitable amplifier bias current.
   The amplifier bias current is selected from the minimum value curve of transconductance (Fig. 10a) to assure that the amplifier will provide sufficient gain. For the required g_{21} of 5.5 mmho an amplifier bias current I_{ABC} of 20 μA is suitable.

3. Determination of Output Swing Capability.
   For a loop gain of 10 the output swing is ±0.5 V and the peak load current 25 μA. However, the amplifier must also supply the necessary current through the feedback resistor and for R_S = 20 kΩ than R_F = 200 kΩ if A_{OL} = 10. Therefore, the feedback loading = 0.5/200 kΩ = 2.5 μA.

   The total amplifier current output requirements are, therefore, ±27.5 μA. Referring to the data given in Fig. 6a we see that for an amplifier bias current of 20 μA the amplifier output current is ±40 μA. This is obviously adequate and it is not necessary to change the amplifier bias current I_{ABC}.

4. Calculation of bias resistance.
   For minimum supply current drain the amplifier bias current I_{ABC} should be fed directly from the supplies and not from the bias regulator. The value of the resistor R_{ABC} may be directly calculated using Ohm's law.

$$R_{ABC} = \frac{V_{SUP} \cdot V_{ABC}}{I_{ABC}}$$

$$R_{ABC} = \frac{12 - 0.63}{20 \times 10^{-6}}$$

$$= 568.5\ k\Omega \text{ or} \cong 560\ k\Omega$$

5. Calculation of offset adjustment circuit.
   In order to reduce the loading effect of the offset adjustment circuit on the power supply, the offset control should be arranged to provide the necessary offset current. The source resistance of the non-inverting input is made equal to the source resistance of the inverting input.

$$\text{i.e. } \frac{20 \times 200 \times 10^6 \text{ ohms}}{220 \times 10^3} \cong 18\ k\Omega$$

Because the maximum offset voltage is 5 mV and an additional increment due to the offset current (Fig. 4) flowing through the source resistance

(i.e. $200 \times 10^{-9} \times 18 \times 10^3$ volts), therefore,

the Offset Voltage Range = 5 mV + 3.6 mV = ±8.6 mV

The current necessary to provide this offset is

$$\frac{8.6 \times 10^{-3}}{18 \times 10^3} \text{ or } 0.48\ \mu A$$

With a supply voltage of ±6 V, this current can be provided by a 10 MΩ resistor. However, the stability of such a resistor is often questionable and a more realistic value of 2.2 MΩ was used in the final circuit.

OTHER CONSIDERATIONS

Capacitance Effects

The CA3060 is designed to operate at such low power levels that high impedance circuits must be employed. In designing such circuits, particularly feedback amplifiers, stray circuit capacitance must always be considered because of its adverse effect on frequency response and stability. For example a 10-kΩ load with a stray capacitance of 15 pF has a time constant of 1 MHz. Fig. 18 illustrates how a 10-kΩ 15-pF load modifies the frequency characteristic.

CA3060, CA3060A Types

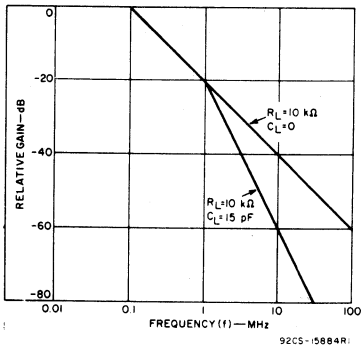


Fig.18—Effect of capacitive loading on frequency response.

Capacitive loading also has an effect on slew rate; because the peak output current is established by the amplifier bias current, I_{ABC} (see Fig. 6a), the maximum slew rate is limited to the maximum rate at which the capacitance can be charged by the I_{OM}. Therefore,

$$SR = dV/dt = I_{OM}/C_L$$

where C_L is the total load capacitance including strays. This relationship is shown graphically in Fig. 19. When measuring slew rate for this data bulletin, care was taken to keep the total capacitive loading to 13 pF.

Phase Compensation

In many applications phase compensation will not be required for the amplifiers of the CA3060. When needed, compensation may easily be accomplished by a simple RC network at the input of the amplifier as shown in Fig. 13. The values given in Fig. 13 provide stable operation for the critical unity gain condition, assuming that capacitive loading on the output is 13 pF or less. Input phase compensation is recommended in order to maintain the highest possible slew rate.

In applications such as integrators, two OTAs may be cascaded to improve current gain. Compensation is best accomplished in this case with a shunt capacitor at the output of the first amplifier. The high gain following compensation assures a high slew rate.

APPLICATIONS

Having determined the operating points of the CA3060 amplifiers, they can now function in the same manner as conventional op-amps, and thus, are well suited for most op-amp applications, including inverting and non-inverting amplifiers, integrators, differentiators, summing amplifiers etc.

TRI-LEVEL COMPARATOR

Tri-level comparator circuits are an ideal application for the CA3060 since it contains the requisite three amplifiers. A tri-level comparator has three adjustable limits. If either the upper or lower limit is exceeded, the appropriate output is activated until the input signal returns to a selected intermediate limit. Tri-level comparators are particularly suited to many industrial control applications.

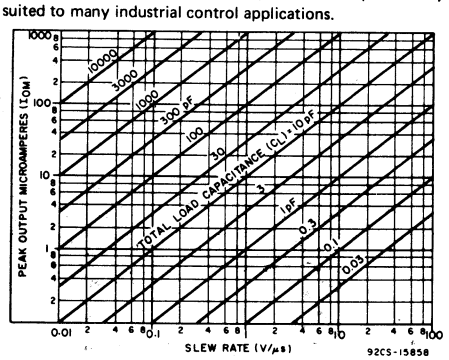


Fig.19—Effect of load capacitance on slew rate.

Circuit Description

Fig. 20 shows the block diagram of a tri-level comparator using the CA3060. Two of the three amplifiers are used to compare the input signal with the upper-limit and lower-limit reference voltages. The third amplifier is used to compare the input signal with a selected value of intermediate-limit reference voltage. By appropriate selection or resistance ratios this intermediate-limit may be set to any voltage between the upper-limit and lower-limit values. The output of the upper-limit and lower-limit comparator sets the corresponding upper or lower-limit flip-flop. The activated flip-flop retains its state until the third comparator (intermediate-limit) in the CA3060 initiates a reset function, thereby indicating that the signal voltage has returned to the intermediate-limit selected. The flip-flops employ two CA3086 transistor-array IC's, with circuitry to provide separate "SET" and "POSITIVE OUTPUT" terminals.

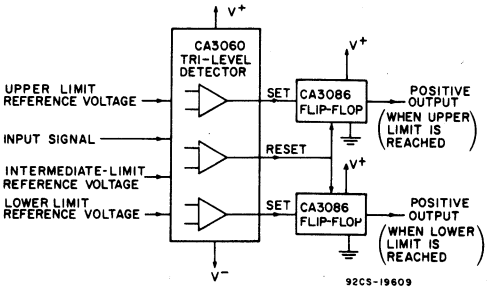


Fig.20—Functional block diagram of a tri-level comparator.

The circuit diagram of a tri-level comparator appears in Fig. 21. Power is provided for the CA3060 via terminals 3 and 8 by ±6-volt supplies and the built-in regulator provides amplifier-bias-current (I_{ABC}) to the three amplifiers via terminal 1. Lower-limit and upper-limit reference voltages are selected by appropriate adjustment of potentiometers R1 and R2, respectively. When resistors R3 and R4 are equal in value (as shown), the intermediate-limit reference voltage is automatically established at a value midway between the lower-limit and upper-limit values. Appropriate variation of resistors R3 and R4 permits selection of other values of intermediate-limit voltages. Input signal (E_S) is applied to the three comparators via terminals 5, 12, and 14. The "SET" output lines trigger the appropriate flip-flop whenever the input signal reaches a limit value. When the input signal returns to an intermediate-value, the common flip-flop "RESET" line is energized. The loads in the circuits, shown in Fig. 21 are 5-V, 25-mA lamps.

Active Filters — Using the CA3060 as a Gyrator

The high output impedance of the OTAs makes the CA3060 ideally suited for use as a gyrator in active filter applications. Fig. 22 shows two OTAs of the CA3060 connected as a gyrator in an active filter circuit. The OTAs in this circuit can make a 3-μF capacitor function as a floating 10-kilohenry inductor across Terminals A and B. The measured Q of 13 (at a frequency of 1 Hz) of this inductor compares favorably with a calculated Q of 16. The 20-kilohm to 2-megohm attenuators in this circuit extend the dynamic range of the OTA by a factor of 100. The 100-kilohm potentiometer, across V+ and V⁻, tunes the inductor by varying the g_{21} of the OTAs, thereby changing the gyration resistance.

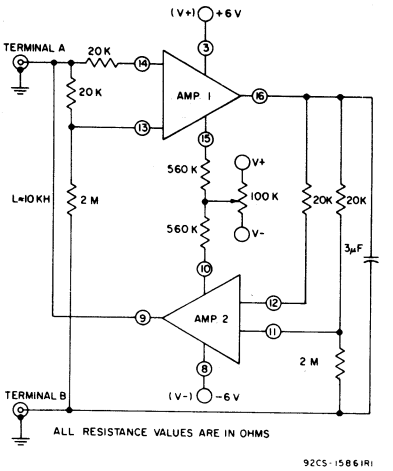


Fig.22—Two operational transconductance amplifiers of the CA3060 connected as a gyrator in an active filter circuit.

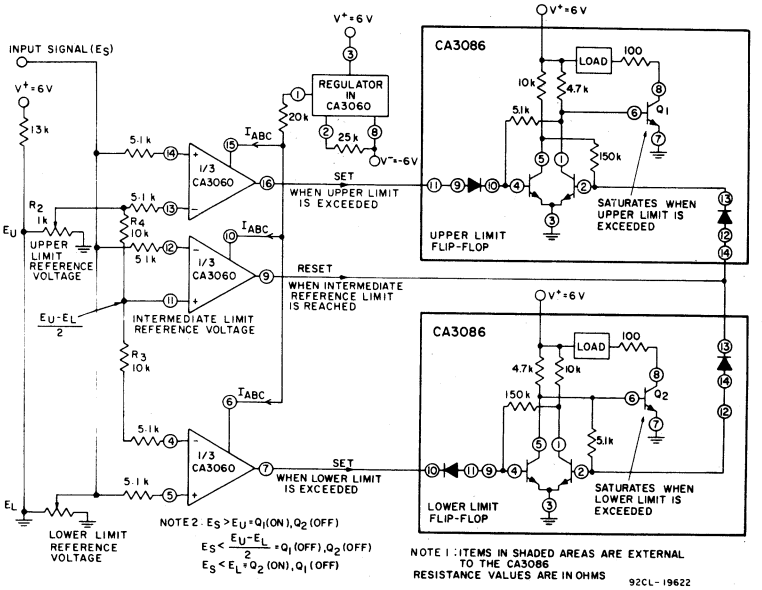


Fig.21—Tri-level comparator circuit.

CA3060, CA3060A Types

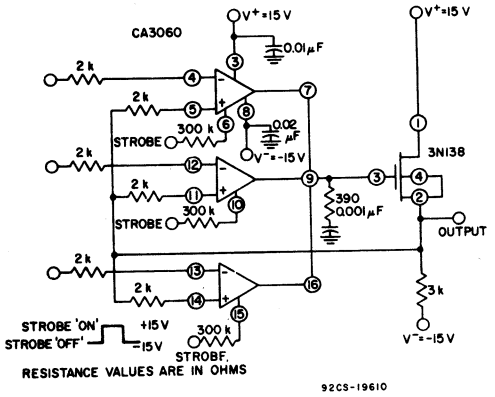


Fig.23—Three-channel multiplexer.

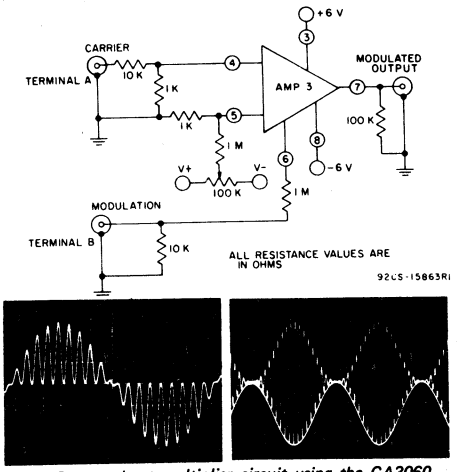


Fig.24—Two-quadrant multiplier circuit using the CA3060 with associated waveforms.

THREE CHANNEL MULTIPLEXER

Fig. 23 shows a schematic of a three channel multiplexer using a single CA3060 and a 3N138 MOS/FET as a buffer and power amplifier.

When the CA3060 is connected as a high-input impedance voltage follower, and strobe "ON," each amplifier is activated and the output swings to the level of the input of that amplifier. The cascade arrangement of each CA3060 amplifier with the MOS/FET provides an open loop voltage gain in excess of 100 dB, thus assuring excellent accuracy in the voltage follower mode with 100% feedback.

Operation at ±6 volts is also possible with several minor changes. First, the resistance in series with amplifier bias current (I_{ABC}) terminal of each amplifier should be decreased to maintain 100 μA of strobe—"ON" current at this lower supply voltage. Second, the drain resistance for the MOS/FET should be decreased to maintain the same value of source current. The low cost dual-gate protected MOS/FET, RCA-40841, may be used when operating at the low supply voltage.

The phase compensation network consists of a single 390Ω resistor and a 1000-pF capacitor, located at the interface of the CA3060 output and the MOS/FET gate. The bandwidth of the system is 1.5 MHz and the slew rate is 0.3 volts/μsec. The system slew rate is directly proportional to the value of the phase compensation capacitor. Thus, with higher gain settings where lower values of phase compensation capacitors are possible, the slew rate is proportionally increased.

NON LINEAR APPLICATIONS

AM Modulator (Two-Quadrant Multiplier)

Fig. 24 shows Amplifier No. 3 of the CA3060 used in an AM modulator or 2-quadrant multiplier circuit. When modulation is applied to the amplifier bias input, Terminal B, and the carrier frequency to the differential input, Terminal A, the waveform, shown in Fig. 24, is obtained. Fig. 24 is a result of adjusting the input offset control to balance the circuit so that no modulation can occur at the output without a carrier input. The linearity of the modulator is indicated by the solid trace of the superimposed modulating frequency. The maximum depth of modulation is determined by the ratio of the peak input modulating voltage to V^-.

The two-quadrant multiplier characteristic of this modulator is easily seen if modulation and carrier are reversed as shown in Fig. 24. The polarity of the output must follow that of the differential input; therefore, the output is positive only during, the positive half cycle of the modulation and negative only in the second half cycle. Note, that both the input and output signals are referenced to ground. The output signal is zero when either the differential input or I_{ABC} are zero.

Four-Quadrant Multiplier

The CA3060 is also useful as a four-quadrant multiplier. A block diagram of such a multiplier, utilizing Amplifier Nos. 1, 2, and 3, is shown in Fig. 25 and a typical circuit is shown in Fig. 26. The multiplier consists of a single CA3060 and, as in the two-quadrant multiplier, exhibits no level shift between input and output. In Fig. 25, Amplifier No. 1 is connected as an inverting amplifier for the X-input signal. The output current of Amplifier No. 1 is calculated as follows:

$$I_O(1) = [-V_X]\ [g_{21}(1)] \qquad \text{(Eq.3)}$$

Ampl. No. 2 is a non-inverting amplifier so that

$$I_O(2) = [+V_X]\ [g_{21}(2)] \qquad \text{(Eq. 4)}$$

Because the amplifier output impedances are high, the load current is the sum of the two output currents, for an output voltage

$$V_O = V_X R_L\ [g_{21}(2) - g_{21}(1)] \qquad \text{(Eq. 5)}$$

The transconductance is approximately proportional to the amplifier bias current; therefore, by varying the bias current the g_{21} is also controlled. Amplifier No. 2 bias current is proportional to the Y-input signal and is expressed as

$$I_{ABC(2)} \approx \frac{(V\text{-}) + V_Y}{R_1} \qquad \text{(Eq. 6)}$$

Hence,

$$g_{21}(2) \approx k\ [\,(V\text{-}) + V_Y\,]. \qquad \text{(Eq. 7)}$$

Bias for Amplifier No. 1 is derived from the output of Amplifier No. 3 which is connected as a unity-gain inverting amplifier. $I_{ABC(1)}$, therefore, varies inversely with V_Y. And by the same reasoning as above

$$g_{21}(1) \approx k\ [(V\text{-}) - V_Y]. \qquad \text{(Eq. 8)}$$

Combining equation 5, 7, and 8 yields:

$$V_O \approx V_X \cdot k \cdot R_L \left|\{(V\text{-}) + V_Y] - [(V\text{-}) - V_Y]\right| \text{ or}$$

$$V_O \approx 2\,k\,R_L\,V_X\,V_Y$$

Fig. 26 shows the actual circuit including all the adjustments associated with differential input and an adjustment for equalizing the gains of Amplifiers No. 1 and No. 2. Adjustment of the circuit is quite simple. With both the X and Y voltages at zero, connect Terminal 10 to Terminal 8. This procedure disables Amplifier No. 2 and permits adjusting the offset voltage of Amplifier No. 1 to zero by means of the 100-kΩ potentiometer. Next, remove the short between Terminals 10 and 8 and connect Terminal 15 to Terminal 8. This step disables Amplifier No. 1 and permits Amplifier No. 2 to be zeroed with the other potentiometer. With AC signals on both the X and Y input, R3 and R11 are adjusted for symmetrical output signals. Fig. 27 shows the output waveform with the multiplier adjusted. The voltage waveform in Fig. 27a shows suppressed carrier modulation of 1-kHz carrier with a triangular wave.

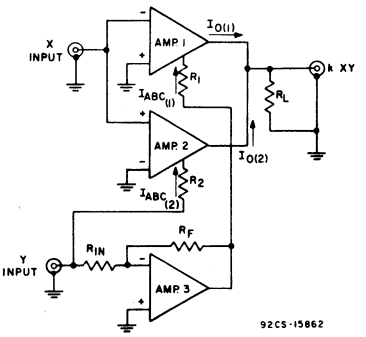


Fig.25—Four-quadrant multiplier using the CA3060.

Figures 27b and 27c, respectively, show the squaring of a triangular wave and a sine wave. Notice that in both cases the outputs are always positive and return to zero after each cycle.

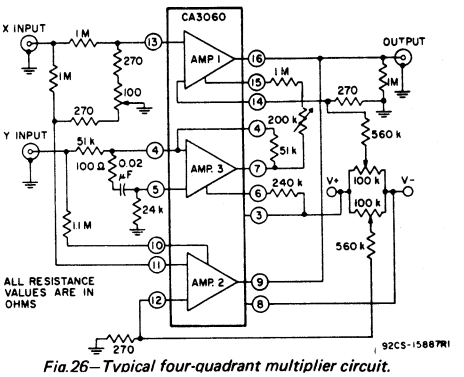


Fig.26—Typical four-quadrant multiplier circuit.

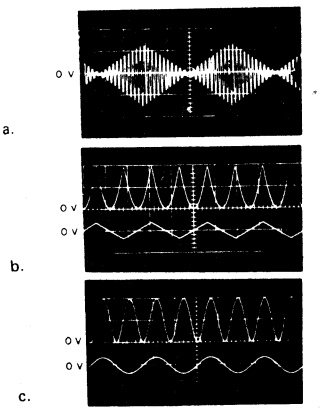


Fig.27—Voltage waveforms of four-quadrant multiplier circuit.

CA3062

Photo Detector and Power Amplifier

For Photoelectric Control Applications

Applications

- Counters
- Sorting
- Level controls
- Inspection
- Intrusion alarms
- Position sensor
- Edge monitoring
- Isolators
- **See ICAN-6538, "Applications of the RCA-CA3062 IC Photodetector and Power Amplifier in Switching Circuits"**

Features

- **100 mA output-current capability – can drive a relay or thyristor directly**
- **5 to 15 volt dc supply voltage**
- **Compact – complete system in a TO-5 style package**

The CA3062* is an integrated circuit consisting of a photosensitive section, an amplifier, and a pair of high-current output transistors on a single monolithic chip.

The photosensitive section consists of Darlington pairs and affords high sensitivity. The power amplifier has a differential configuration which provides complementing outputs in response to a light input – normally "ON" and normally "OFF". The separate photodetector, amplifier, and high-current switch provide flexibility of circuit arrangement. This feature plus the high current capability of the output section, can now provide the user with a complete system particularly useful in photoelectric control applications utilizing IR emitters and visible-light sources.

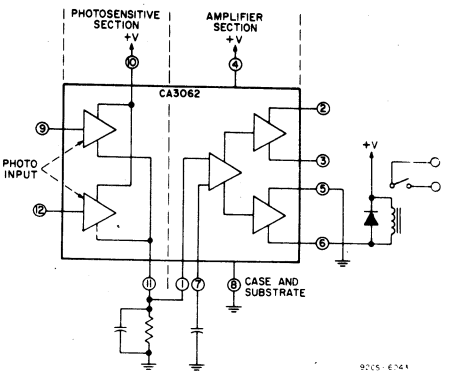


Fig. 1 - Light operated relay using CA3062.

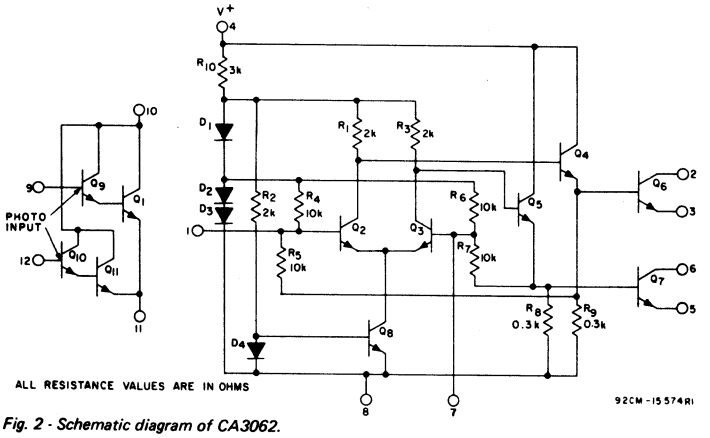


Fig. 2 - Schematic diagram of CA3062.

ABSOLUTE-MAXIMUM RATINGS

DISSIPATION:

Up to T_A = 55°C	700 mW
Above T_A = 55°C	Derate linearly 5.6 mW/°C
At Case Temperature (T_C) ≤ 55°C	1.5 W
Above T_C = 55°C	Derate linearly 16 mW/°C

TEMPERATURE RANGE:

Operating	-55°C to +125°C
Storage	-65°C to +150°C

LEAD TEMPERATURE (During soldering):

At distance ≥ 1/32 in (3.17 mm) from seating plane for 10 s max	+300°C

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 3 is +15 to 0 volts.

TERMINAL No.	10	11	12	1	2	3	4	5	6	7	8
9	0 -9	+2 -5	*	*	*	*	*	*	*	*	*
10		+9 0	+9 0	*	*	*	*	*	*	*	+15 0
11			+5 -2	*	*	*	*	*	*	*	*
12				*	*	*	*	*	*	*	*
1					*	*	*	*	*	+5 -5	+3 -3
2						+15 0	*	*	*	*	+15 0
3							*	*	*	*	+5 0
4								*	*	*	+9 0
5									0 -15	*	+5 0
6										*	+15 0
7											+3 -3
8	Reference Substrate and Case										

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

Maximum Current Ratings

TERMINAL No.	I_{IN} mA	I_{OUT} mA
9	1	0.1
10	5	0.1
11	0.1	5
12	1	0.1
1	1	0.1
2	100	0.1
3	0.1	100
4	10	1
5	0.1	100
6	100	0.1
7	1	0.1
8	1	10

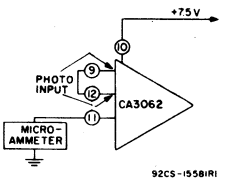


Fig. 3 - Test circuit for photocurrent and typical spectral response of photosensitive Darlington unit.

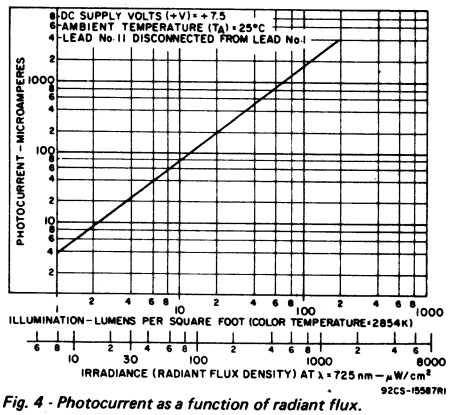


Fig. 4 - Photocurrent as a function of radiant flux.

CA3062

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	MEASUREMENT TERMINAL Nos.	TEST CIRCUIT FIG.	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
STATIC CHARACTERISTICS								
Photo Darlington Section: Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	E = 0 lumens/ft^2, I_C = 1 mA	10-11	–	10	–	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 0.1 mA, E = 0	9-11, 12-11	–	10	–	–	V
Dark Current	I_{DARK}	V_{CE} = 7.5 V, E = 0	10	3	–	0.1	30	μA
Photo Current	I_P	V_{CE} = 7.5 V, E = 8 lumens/ft^2	10	3	–	60	–	μA
Wavelength of Max. Sensitivity	λ max.			3	–	725	–	Note2 nm
Relative Angular Sensitivity				–	–	–	–	–
Area of Each Photo Transistor				–		1.3 x 10^{-4} cm^2		
Amplifier Section Output Transistor: Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO\,6}$, $V_{(BR)CEO\,7}$	I_C = 1 mA	2-3, 6-5	–	15	–	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO\,6}$, $V_{(BR)EBO\,7}$	I_E = 1 mA	3-8, 6-8	–	5	–	–	V
DC Supply Current	I_{SUPPLY}	V_4 = 7.5 V	4	–	–	5.5	10	mA
Sensitivity: Illumination, For Normal "OFF" Output	E_{ON}	Set light input for I_6 = 70 mA	6	7, 15, 17	–	8	70	Notes 1, 3 lumens per ft^2
For Normal "ON" Output	E_{OFF}	Set light input for I_2 = 5 mA	2	7, 15, 17	–	10	–	Notes 1, 3 lumens per ft^2
DYNAMIC CHARACTERISTICS								
Overall Response Time: Turn-On Time	t_{on}	E = 700 μW/cm^2 at λ = 930 nm	—	12	–	38	–	μs
Rise Time	t_r			12	–	125	–	μs
Turn-Off Time	t_{off}			12	–	43	–	μs
Fall Time	t_f			12	–	20	–	μs

NOTES

(1) Tungsten filament light source at a color temperature of 2854K.
(2) One (1) nanometer = 10 Angstrom units.
(3) A radiant flux density of 7.5 μW/cm^2 at 725 nm produces the same photocurrent as 1 lumen/ft^2 from a tungsten filament lamp at a color temperature of 2854K.

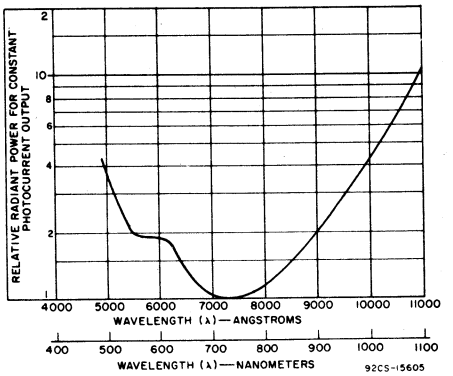


Fig. 5 - Typical spectral response of photosensitive Darlington unit.

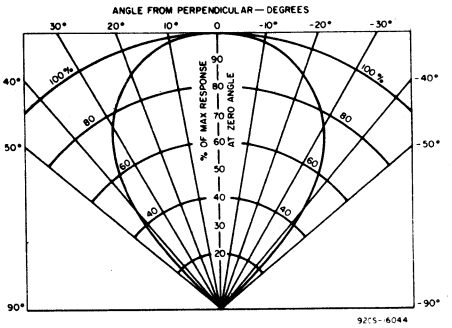


Fig. 6 - Relative angular sensitivity.

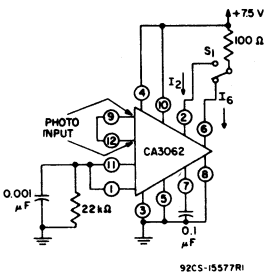


Fig. 7 - Test circuit for sensitivity and dc current measurement.

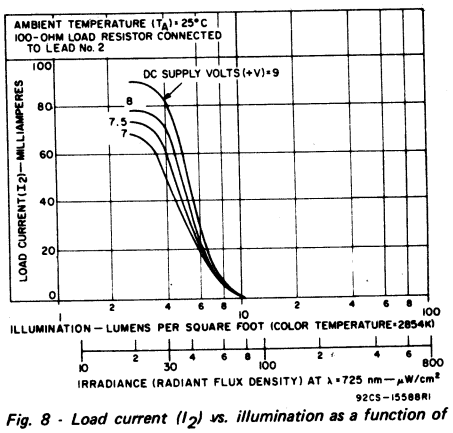


Fig. 8 - Load current (I_2) vs. illumination as a function of supply volts.

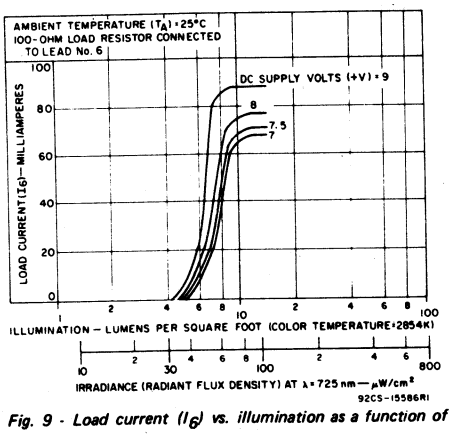


Fig. 9 - Load current (I_6) vs. illumination as a function of supply volts.

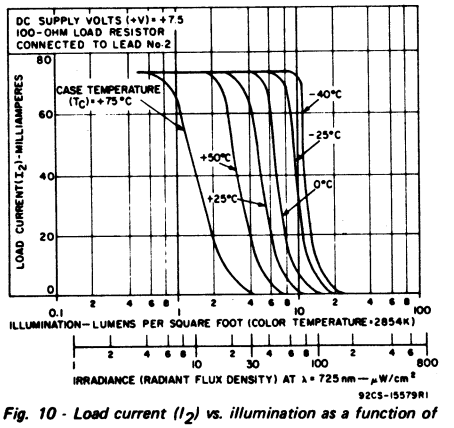


Fig. 10 - Load current (I_2) vs. illumination as a function of case temperature.

CA3062

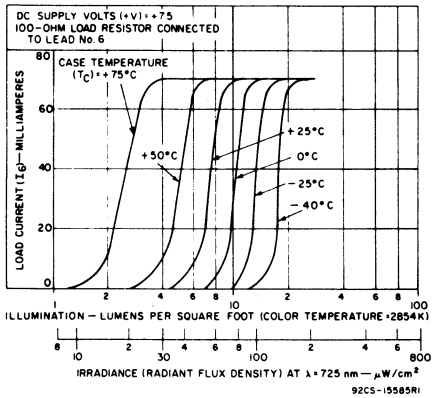


Fig. 11 - Load current (I_E) vs. illumination as a function of case temperature.

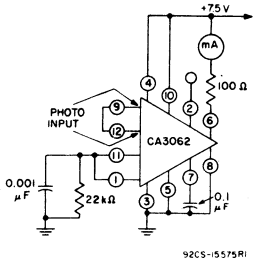


Fig. 12 - Response time test circuit.

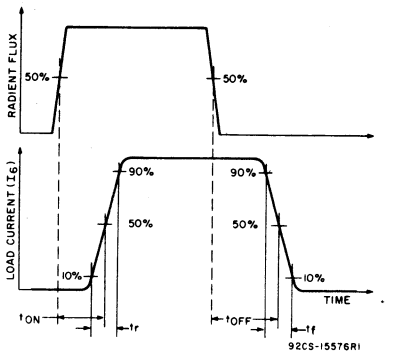


Fig. 13 - Waveforms for measurement of response time.

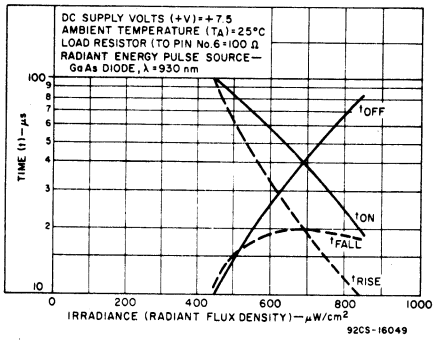


Fig. 14 - Response time as a function of radiant flux density.

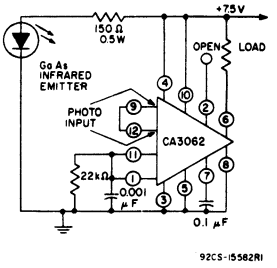


Fig. 15 - Circuit diagram for "ON-OFF" photoelectric control applications.

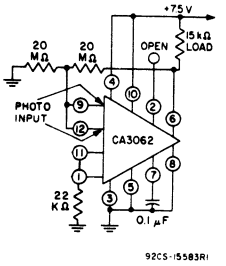


Fig. 16 - Circuit diagram for linear output photoelectric applications.

OPERATING CONSIDERATIONS

Switching Service

The CA3062 is primarily intended to provide "ON-OFF" output in response to a light signal. Optimum performance of this device is achieved when the output transistors are operated at values of load current sufficient to saturate the device in the "ON" state. Operation of the CA3062 at values of load current between the condition of no load current and saturation will cause substantial power to be dissipated in the silicon chip. This condition of operation is therefore not recommended because the heat rise in the silicon chip induced by the increased power dissipation causes the load current to shift in the same direction as though additional illumination were applied to the CA3062, a condition which will substantially alter the switching characteristics of the device.

The signal voltages at the input terminals (terminal No. 1 and No. 7) must not exceed 3 volts, because any increase in the signal voltage beyond the value specified will cause both output transistors to be turned "ON". In the circuit shown in Fig. 7, this condition will occur for values of illumination greater than 60 lumens/ft ^{2}. This adverse operating condition can be avoided by either limiting the maximum illumination or by clamping the input so that the voltage does not exceed 3 volts.

Linear Service

The CA3062 can be connected as shown in Fig. 16 to give a linear output. The value of the load resistor should be greater than 1000 ohms in order to limit the power dissipation and thus minimize the heating effects. Because of the many possible variations in circuit configurations, the CA3062 has not been characterized for linear service applications. A guide-line circuit for this class of service is shown in Fig. 16.

Specific inquiries for use of the CA3062 in this type of service should be addressed to your local RCA Field Technical Representative.

Precautions

Because of the high amplification of the CA3062, care should be taken, when wiring, to keep all lead lengths as short as possible. A recommended breadboard layout is shown in Fig. 17.

If the CA3062 is operated with an inductive load impedance, such as a relay, it is recommended that a diode be connected across the load to absorb the energy of the pulse voltages generated during switching.

Many of the graphs are shown with two sets of abscissa values for light energy input, one expressed in illumination values (lumens/sq. ft.) and the other in irradiance values (μW/sq. cm.)

Correlation between these two sets of abscissa values is accomplished by having the light source operating at the maximum sensitivity wavelength of the CA3062. See Notes on page three.

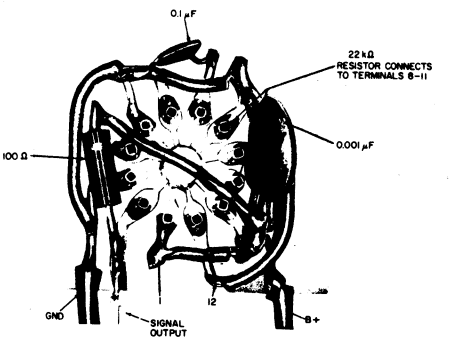


Fig. 17 - Breadboard layout of test circuit, shown in Fig. 7 for the CA3062.

CA3064, CA3064E

TV Automatic Fine Tuning Circuit

RCA-CA3064 and CA3064E represent the third generation of integrated circuits designed primarily for AFC (Automatic-Frequency-Control) applications. They provide all of the signal-processing components needed (with the exception of the tuned-phase-detector transformer) to derive the AFT correction signals from the output of the video-if amplifier. The CA3064 is supplied in the 10-formed-lead TO-5 style package, and the CA3064E in the 14-lead dual-in-line plastic package. Both types operate over the temperature range of −55 to +125°C.

The CA3064 and CA3064E are functionally similar to the CA3044 and CA3044V1 but embody a higher-gain input amplifier which provides a 20-dB improvement in sensitivity. The increased sensitivity extends the application of a proven AFT system to the low-level if-amplifier stages in TV receivers.

Because the CA3064 and CA3064E are functionally similar to the CA3044 and CA3044V1, refer to Application Note ICAN-5831, "Application of the RCA CA3044 and CA3044V1 Integrated Circuits in Automatic Fine-Tuning Systems" for general application information.

Features:

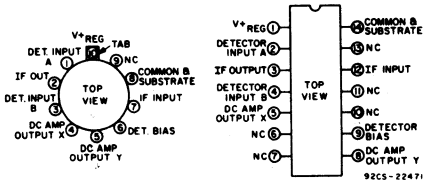
- **Cascode type high-gain amplifier (18 mV input for rated output)**
- **Internal voltage regulator**
- **Differential detector**
- **For use with either color or monochrome**
- **Differential amplifier**
- **Bipolar outputs**
- **Wide operating-temperature range; −55 to +125°C**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DEVICE DISSIPATION:
Up to T_A = 25°C . . . . . 700 mW
Above T_A = 25°C . . . . . derate linearly 5.6 mW/°C

AMBIENT TEMPERATURE RANGE:
Operating . . . . . −55 to +125°C
Storage . . . . . −65 to +150°C

LEAD TEMPERATURE (During Soldering):
At distance 1/16" ± 1/32" (1.59 mm ± 0.79 mm) from case for 10 s max.. . . . . 265°C



(a) CA3064 *(b) CA3064E*

Fig.2 – Terminal assignment diagrams.

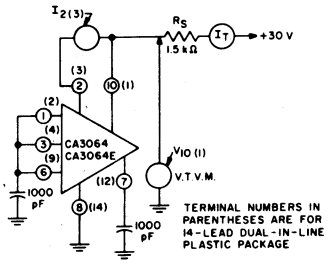


Fig. 3 – Test setup: Measurement of total device dissipation, zener regulating voltage, quiescent operating current at terminal 2 (3).

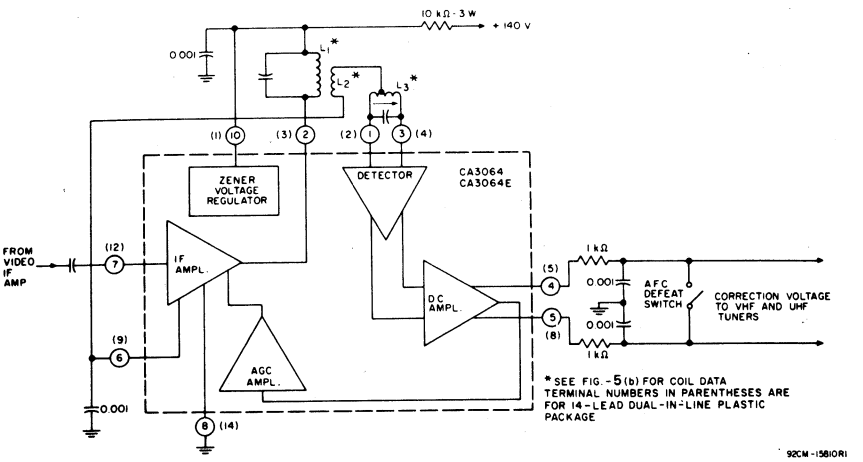


Fig.1 – Block diagram of typical operating circuit utilizing the CA3064 and CA3064E.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CIRCUITS FIG.	TEST CONDITIONS		LIMITS CA3064, CA3064E MIN.	TYP.	MAX.	UNITS	CHARACTERISTIC CURVES FIG.
STATIC CHARACTERISTICS									
Device Dissipation	P_D	3	V^+ = 30V, R_S = 1.5kΩ	T_A −25°C	-	135	150	mW	-
				+25°C	130	140	150		-
				+85°C	-	145	150		-
Current Drain at 10.5 Volts	I_T	3	$V_{10(1)}$ = 10.5 V		4	6.5	9.5	mA	-
Zener Regulated Voltage – DC Supply Voltage at terminal 10(1)*	$V_{10(1)}$	3	V^+ = 30 V, R_S = 1.5 kΩ		10.9	11.8	12.8	V	-
Quiescent Operating Current into Terminal 2(3)	$I_{2(3)}$	3			1	2	4	mA	-
Quiescent Operating Voltage at Terminal 4(5)	$V_{4(5)}$	-			5	6.9	8	V	-
Quiescent Operating Voltage at Terminal 5(8)	$V_{5(8)}$	-			5	6.9	8	V	-
Output Offset Voltage between Terminals 4 and 5(5 and 8)	V_{4-5} (5-8)	-			-1	0	1	V	-
DYNAMIC CHARACTERISTICS (AS RF AMPLIFIER IN TO-5 STYLE PACKAGE)									
Input Voltage Sensitivity	V_I sensitivity	5	V^+ = +30 V, V_I = 18 mV		Correction Voltage Output as shown in table below.				
Input Admittance	y_{11}	-	f = 45.75 MHz, V^+ = 30 V, R_S = 1.5 kΩ		-	0.41 + j1.0	-	mmho	-
Reverse Transfer Admittance	y_{12}	-			-	0 +j3.4	-	μmho	-
Forward Transfer Admittance	y_{21}	-			-	24.5 - j29	-	mmho	-
Output Admittance	y_{22}	-			-	0.04 + j0.9	-	mmho	-
OUTPUT vs FREQUENCY DEVIATION - AFC									
Correction-Control Voltage at Terminal 4(5)	V corr. 4(5)	5	V^+ = +30 V, V_I = 18 mV RMS, f_o = MHz as indicated		% of V_{10} (1)		% of V_{10} (1)	V	6,7
			45.750 - 0.030		85	-	-	V	
			45.750 + 0.030		-	-	25	V	
			45.750 - 0.900		80	-	-	V	7
			45.750 + 0.900		-	-	35	V	
			45.750 - 1.500			-	80	V	
			45.750 + 1.500		35	-		V	
Correction-Control Voltage at Terminal 5(8)	V corr. 5(8)	5	45.750 - 0.030		-	-	25	V	6,7
			45.750 + 0.030		85	-	-	V	
			45.750 - 0.900		-	-	35	V	7
			45.750 + 0.900		80	-	-	V	
			45.750 - 1.500		35	-	-	V	
			45.750 + 1.500		-	-	80	V	

* Terminal numbers in parentheses are for 14-lead dual-in-line plastic package.

CA3064, CA3064E

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 (3) and horizontal terminal 6 (9) is +20 to 0 volts. Terminal nos. in parentheses are for the 14-lead dual-in-line plastic package.

TERMINAL No.	9(6,7,10,11,13)	10 (1)	1 (2)	2 (3)	3 (4)	4 (5)	5 (8)	6 (9)	7 (12)	8 (14)
9(6,7,♦10,11,13)	← NO INTERNAL CONNECTION →									
10 (1)			+12 0	+10 -10	+12 0	+12 0	+12 0	+10 0	+20 0	▲
1 (2)				*	+10 -10	*	*	+5 -5	*	+5 -6
2 (3)					*	*	*	+20 0	*	+20 0
3 (4)						*	*	+5 -6	*	+5 -6
4 (5)							*	*	*	+12 0
5 (8)								*	*	+12 0
6 (9)									+5 -2	+2 0
7 (12)										+2 -10
8 (14)										REF.SUBSTRATE & CASE■

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
9(6,7,10,11,13)	-	-
10 (1)	50	50
1 (2)	1	0.1
2 (3)	20	20
3 (4)	1	0.1
4 (5)	5	5
5 (8)	5	5
6 (9)	5	5
7 (12)	1	1
8 (14)	50	50

▲ Terminal number 10 (1) may be connected to any positive voltage source greater than the internal zener regulating voltage through a suitable dropping resistor — provided the dissipation rating is not exceeded.

■ This terminal should be connected to the most negative potential of the complete circuit.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

♦ It is recommended that unused terminals 6,7,10,11, and 13 on the 14-lead dual-in-line-plastic package and terminal 9 on the TO-5 package be grounded to act as shields.

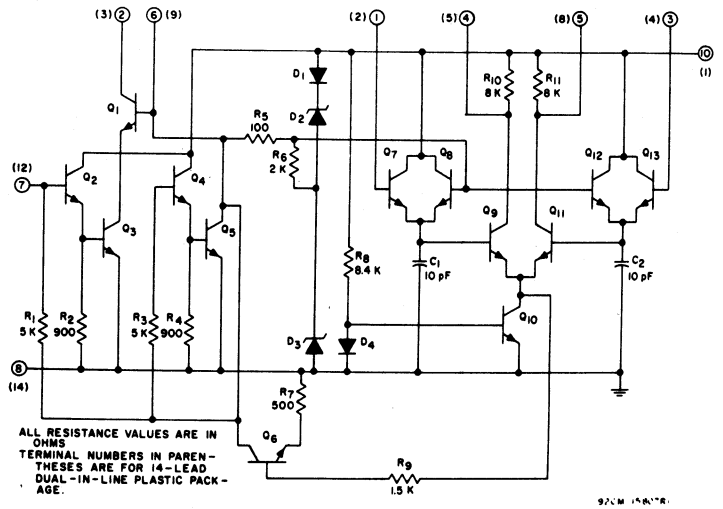
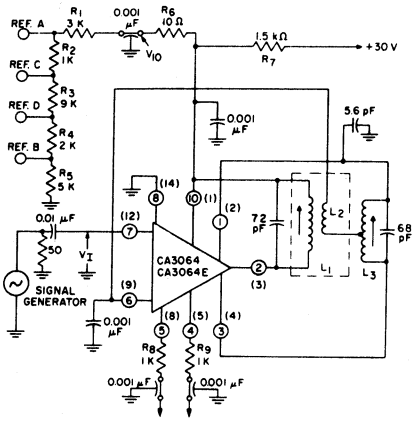


Fig.4 — Schematic diagram for CA3064 and CA3064E.



L_1 IS ALIGNED FOR SYMMETRICAL BANDWIDTH ON EITHER SIDE OF 45.750 MHz
L_2 TERTIARY WINDING WOUND ON L_1 COIL FORM
L_3 IS ALIGNED FOR ZERO DIFFERENTIAL OUTPUT BETWEEN TERMINALS 4 AND 5 AT f_o = 45.750 MHz
* FOR COIL CONSTRUCTION DATA, SEE FIG.4(b).

REFERENCE VOLTAGE PERCENTAGES	
Ref. A	85% of $V_{10(1)}$
Ref. B	25% of $V_{10(1)}$
Ref. C	80% of $V_{10(1)}$
Ref. D	35% of $V_{10(1)}$

Coil	RCA Distributor Part No.
(L_1, L_2)	122 213
L_3	122 203

Fig.5 (a) — Correction voltage test circuit for CA3064 and CA3064E.

COIL DATA FOR DISCRIMINATOR WINDINGS

L_1 — Discriminator Primary: 3-1/6 turns; #20 Enamel-covered wire — close-wound, at bottom of coil form. Inductance of L_1 = 0.165 μH; Q_o = 120 at f_o = 45.75 MHz. Start winding at terminal #6; finish at Terminal #1. See Notes below.

L_2 — Tertiary Windings: 2-1/6 turns; #20 Enamel-covered wire — close wound over bottom end of L_1. Start winding at Terminal #3; finish at Terminal #4. See Notes below.

L_3 — Discriminator Secondary: 3-1/2 turns; center-tapped, space wound at bottom of coil form. Inductance of L_3 = 0.180 μH; Q_o = 150 at f_o = 45.75 MHz. Start winding at Terminal #2; finish at Terminal #5; connect center tap to Terminal #7. See Notes below.

Notes:
1. Coil Forms; Cylindrical; –0.30" Dia. max.
2. Tuning Core: 0.250" Dia. x 0.37" Length.
   : Material: Carbinal J or equivalent
3. Coil Form Base: See drawing below.
4. End of coil nearest terminal board to be designated the winding start end.

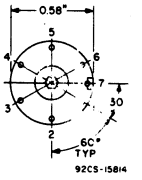


Fig.5 (b) Coil form base terminal diagram.

CA3065

IF AMPLIFIER-LIMITER, FM DETECTOR, ELECTRONIC ATTENUATOR, AUDIO DRIVER

For Television Sound-System Applications

FEATURES:

- Electronic attenuator - replaces conventional volume control
- Differential peak detector - requires one single tuned coil
- Internal Zener diode regulated supply
- Inherent high stability
- Excellent AM rejection - 50 dB typ. at 4.5 MHz
- Low harmonic distortion
- High sensitivity - 200 μV limiting (knee) at 4.5 MHz
- Audio drive capability - 6 mA p-p
- Undistorted audio output voltage - 7 V p-p

The RCA CA3065 Television Sound System is a monolithic integrated circuit which combines a multi-stage IF amplifier limiter, an FM detector, an electronic attenuator, a zener diode regulated power supply, and an audio amplifier-driver that is designed to directly drive an npn power transistor or high-transconductance tube. Because the circuit is so inclusive, a minimum number of external components is required. A block diagram of the integrated circuit television sound system is shown in Fig. 1.

The CA3065 with its advanced circuit design provides a high-performance multistage subsystem for the sound system of a television receiver. A particular feature of the CA3065 is the electronic attenuator which performs the conventional volume control function. Volume control is accomplished when the bias levels in the attenuator are changed by means of a variable resistor connected between Terminal 6 and ground (attenuation in excess of 60 dB is attained). Because no audio signal is present in this control, hum or noise pickup can be bypassed. In most cases, only a single unshielded wire is required between the IF board and the variable resistor (volume control).

The CA3065 utilizes a 14-lead dual-in-line plastic package with leads specially formed to facilitate automatic insertion of the device into suitably punched printed-circuit boards.

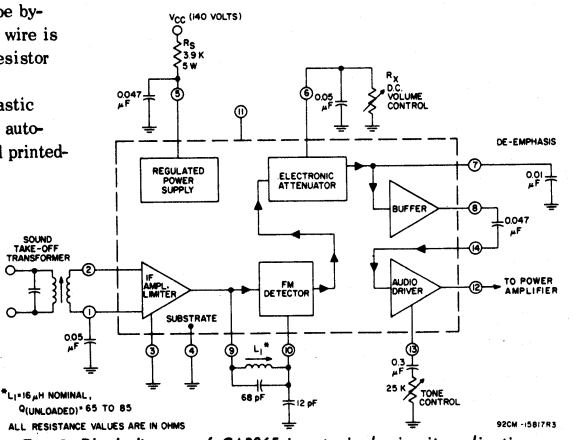


Fig. 1 - Block diagram of CA3065 in a typical circuit application.

MAXIMUM RATINGS, *Absolute Maximum Values*, at T_A = 25° C

Input Signal Voltage (between Terminals 1 and 2)	±3	V
Power Supply Current (Terminal 5)	50	mA
Power Dissipation:		
Up to T_A = 25° C	850	mW
Above T_A = 25° C	Derate linearly 6.67	mW/°C
Ambient Temperature Range:		
Operating	- 40 to + 85	°C
Storage	- 65 to + 150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265	°C

MAXIMUM VOLTAGE RATINGS at T_A = 25° C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 9 with respect to terminal 3 is 0 to +4 volts.

TERMINAL No.	4	5	6	7	8	9	10	11	12	13	14	1	2	3
4		SUBSTRATE CONNECTION – ALWAYS CONNECT TO TERMINAL 3												
5			+13 0	+13 0	+13 0	*	*	INTERNAL CONNECTION DO NOT USE	+13 0	+13 0	*	*	*	NOTE 1
6				*	*	*	*		*	*	*	*	*	+13 −5
7					+1 −4	*	*		*	*	*	*	*	+13 0
8						*	*		*	*	*	*	*	*
9							*		*	*	*	*	*	+4 0
10									*	*	*	*	*	+4 −5
11									INTERNAL CONNECTION DO NOT USE					
12										+4 −1	*	*	*	*
13											*	*	*	*
14												*	*	+3 −5
1													+5 −5	+5 −5
2														+4 −5
3														

Note 1: Terminal No. 5 may be connected to any positive voltage through a suitable resistor provided that the current and dissipation ratings of the CA3065 are not exceeded.

*Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if specified limits between all other terminals are not exceeded.

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
4	SUBSTRATE: CONNECT TO TERMINAL 3	
5	50	1
6	1	1
7	1	1
8	0.5	6
9	1	1
10	1	0.1
11	INT. CONN. DO NOT USE	
12	0.5	6
13	1	2
14	1	0.1
1	1	0.1
2	1	0.1
3	0.1	50

CA3065

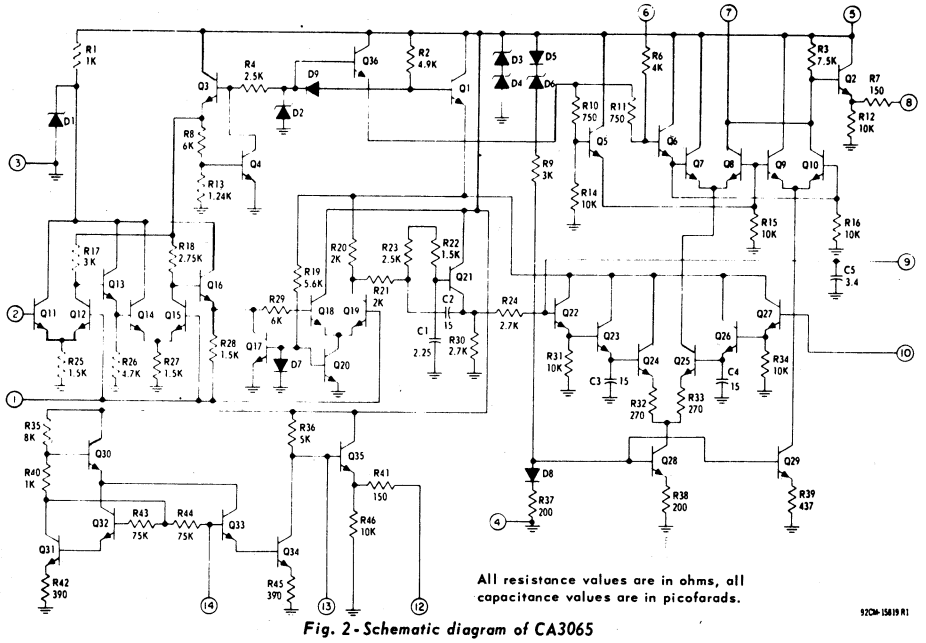


Fig. 2 - Schematic diagram of CA3065

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ±30%.

RCA reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

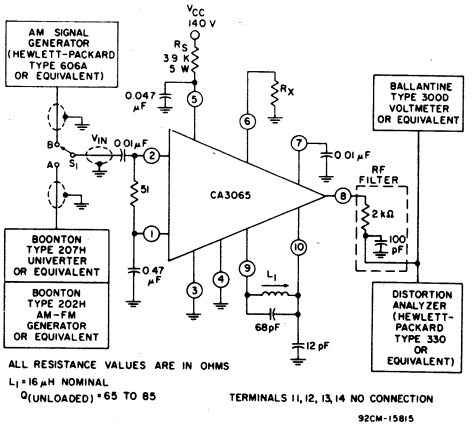


Fig. 3 - Input limiting voltage, AM rejection, recovered audio, total harmonic distortion, maximum attenuation, maximum "play-through" test circuit.

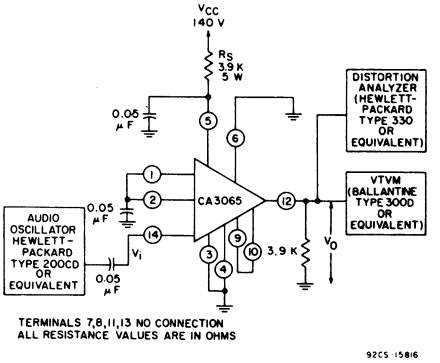
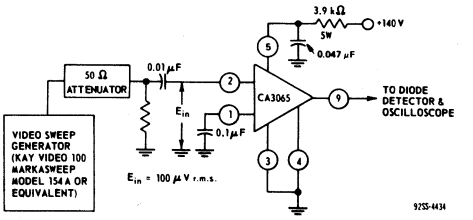


Fig. 4 - Audio voltage gain (undistorted output) test circuit.

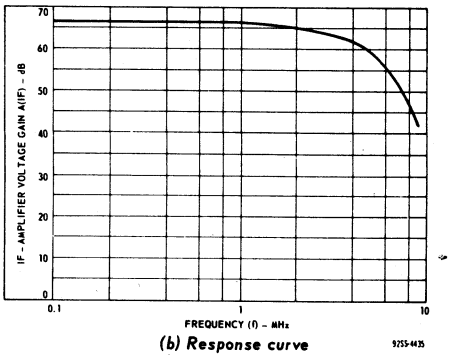
ELECTRICAL CHARACTERISTICS *at T_A = 25° C, V_{CC} = +140 V applied to Terminal 5 through R_S = 3.9 kΩ, and DC Volume Control (R_X) = 0 unless otherwise indicated.*

CHARACTERISTIC	SYMBOL	SPECIAL TEST CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Static Characteristics						
Zener Regulating Voltage Terminal No. 5	V_5		10.3	11.2	12.2	V
Current into Terminal 5	I_5	Connect Terminal 5 to +9 V	10	16	24	mA
Total Device Dissipation	P_T		343	370	400	mW
Terminal Voltages: 1	V_1		–	2	–	V
6	V_6		–	4.8	–	
7	V_7		–	6.1	–	
9	V_9		–	3.7	–	
12	V_{12}		4	5.1	5.8	
Dynamic Characteristics						
IF AMPLIFIER Input Limiting Voltage (at −3 dB point)	$V_{i(lim)}$	f_0 = 4.5 MHz, f_m = 400 Hz, Deviation = ±25 kHz,	–	200	400	μV
AM Rejection	AMR	Amplitude Modulation 30% f = 4.5 MHz	40	50	–	dB
Transconductance Magnitude	$\|G_m\|(IF)$	f = 4.5 MHz IF Input Terminals: 2, 1	–	500	–	mmho
Phase Angle	$\theta(IF)$	IF Output Terminals: 9, 3	–	46	–	degrees
Feedback Capacitance	C_{fb}	f = 1 MHz; Terminals 2 and 9	–	0.02	–	pF
Input Impedance Components: Parallel Input Resistance	$R_i(IF)$	Measured between Terminal Nos. 1 and 2	–	17	–	kΩ
Parallel Input Capacitance	$C_i(IF)$	f = 4.5 MHz	–	4	–	pF
Output Impedance Components: Parallel Output Resistance	$R_0(IF)$	Measured between Terminal No. 9 and gnd	–	3.25	–	kΩ
Parallel Output Capacitance	$C_0(IF)$	f = 4.5 MHz	–	7.5	–	pF
DETECTOR Recovered AF Voltage	$V_0(af)$	f = 4.5 MHz; V_i = 100 mV f = ±25 kHz fm = 400 Hz	0.5	0.75	–	V(rms)
Total Harmonic Distortion	THD		–	0.9	2	%
Output Resistance: Terminal 7	R_0		–	7.5	–	kΩ
Terminal 8			–	300	–	Ω
ATTENUATOR Max. Attenuation	–	See Fig. 7 R_X = ∞	60	80	–	dB
Max. "Play-through" Voltage*	–	R_X = ∞	–	0.075	1	mV
AUDIO AMPLIFIER Voltage Gain	A(af)	V_i = 0.1 V(rms), f = 400 Hz	17.5	20	–	dB
Total Harmonic Distortion	THD	V_O = 2 V(rms), f = 400 Hz	–	1.5	–	%
Undistorted Output Voltage	–	THD = 5%, f = 400 Hz	2	2.5	–	V(rms)
Input Resistance	$R_i(af)$	f = 400 Hz	–	70	–	kΩ
Output Resistance	$R_0(af)$	f = 400 Hz	–	270	–	Ω

*"Playthrough" voltage is the unwanted signal, measured at Terminal 8, when the volume control is set for minimum output.



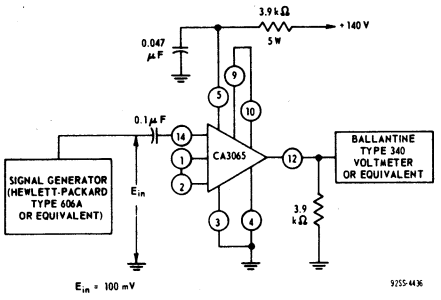
(a) Test circuit



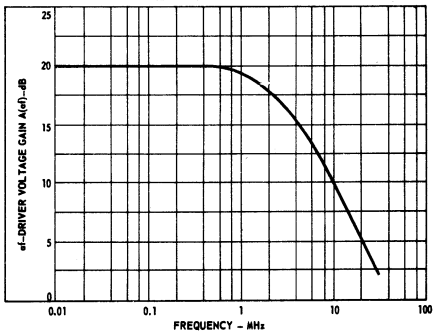
(b) Response curve

Fig. 5 - Frequency response of IF-amplifier section of CA3065

CA3065



(a) Test circuit



(b) Response curve

Fig. 6 - Frequency response of af-amplifier section of CA3065

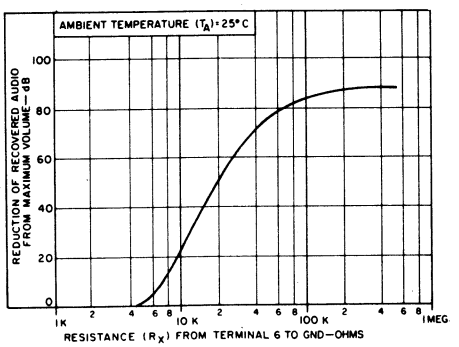
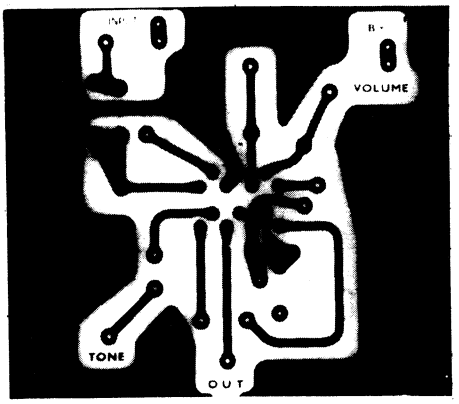
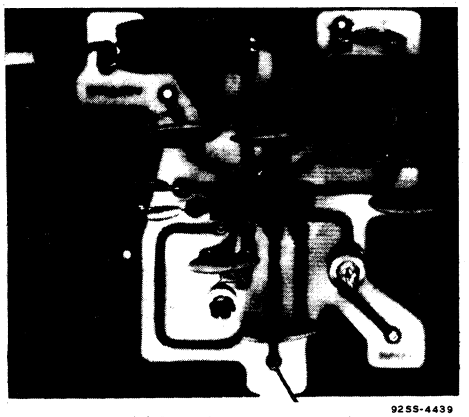


Fig. 7 - Gain reduction vs. resistance (terminal 6 to gnd)



*(a) Printed circuit board – bottom view**



*(b) Parts layout – top view**

Fig. 8 - Recommended parts layout for TV receiver sound strip using CA3065.

* A 200 mil square grid was used in the layout of passive components on the printed circuit board. The Quad-in-line formed leads conform to a standard grid spacing of 100 mil centers.

OPERATING CONSIDERATIONS

The CA3065 may be used to drive a video output transistor or a high-transconductance output tube.

As in all TV receivers, precaution should be taken to prevent destruction of the CA3065 in the event of cascade arcs originating in the picture tube or in the output tube. In the case of arcing in the output tube a resistor of 150 k in series with terminal No. 12 and the grid of the tube is usually sufficient protection.

To prevent damage from picture tube arcs, a careful analysis of board layout and coupling modes (electrostatic or magnetic) may be necessary to suggest alternate layouts or appropriate locations for the placement of spark gaps to absorb the high energy discharge.

CA3066, CA3067

Television Chroma System

The RCA CA3066 and CA3067 are monolithic silicon integrated circuits that constitute a complete chroma system for color television receivers. The CA3066 provides subcarrier regeneration and total chroma signal processing prior to demodulation; the CA3067 performs the demodulation and tint control functions. Each device utilizes a 16-lead quad-in-line plastic package.

CA3066 CHROMA SIGNAL PROCESSOR

The CA3066 contains substantially all the color processing circuitry exclusive of the tint control and demodulating circuits. The chroma amplifier sections of the CA3066 consist of the chroma and bandpass amplifiers. The chroma amplifier receives the chroma input signal at terminal No. 1. This amplifier is gain controlled by the automatic chroma control (ACC) detector-amplifier. The chroma signal is internally coupled from the output of the chroma amplifier to the input of the chroma bandpass amplifier and burst separator amplifier. The horizontal keying pulse (+8V) is used to gate the burst portion of the chroma signal from the input of the bandpass amplifier to the input of the burst separator amplifier. The bandpass amplifier is gain controlled by the dc chroma gain control and can also be controlled by the killer detector-amplifier. The bandpass amplifier output is internally coupled to the chroma output amplifier stage of the CA3066. The coils of the chroma amplifier and the bandpass amplifier are stagger-tuned to provide a combined typical bandpass of 3.08 to 4.08 MHz. The burst separator amplifier injects the burst signal into the 3.58 MHz oscillator. The oscillator amplitude is dependent on the terminal No. 9 impedance to ground and is also responsive to the burst signal amplitude at terminal No. 11. The ACC detector and killer detector sense the burst level or absence of burst, respectively, by monitoring the oscillators response to the burst injection level. The thresholds for the ACC and killer are independently adjusted by resistors R2 and R1 at terminals No. 9 and No. 4, respectively. The chroma output is at terminal No. 14 and the oscillator output is at terminal No. 8. Terminal No. 6 is a zener diode for use as a regulated voltage reference at 11.9 volts. When the zener reference element is not used, the power supply voltage should be maintained at 11.2 ± 0.5 volts.

System Features

CA3066
CHROMA SIGNAL PROCESSOR

- Complete Color Sync Circuit
- Blanked Chroma Amplifier
- Chroma Band-Pass Amplifier
- Low Output Impedance Chroma Driver
- ACC Detector-Amplifier
- Killer Detector-Amplifier
- DC Chroma Gain Control
- Zener Diode for Regulated Voltage Reference
- Short-Circuit Protection on All Terminals

CA3067
CHROMA DEMODULATOR

- Balanced Chroma Demodulators
- Color Difference Matrix
- DC Tint Control
- Three Low Output Impedance Drivers for Direct Coupling
- Reference Subcarrier Limiter
- Zener Diode for Regulated Voltage Reference
- Internal RF Filtering

CA3066

ELECTRICAL CHARACTERISTICS at T_A = 25°C and V^+ = 11.2 V

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST FIG. AND CURVES
Static Characteristics							
Voltages:							
ACC Reference	V_2		–	0.5	–		
Burst-Chroma Ampl. Bias Current Term.	V_3		–	2.9	–		
Killer Reference	V_4		–	1.0	–		
Zener Reg. Reference	V_6		10.6	11.9	12.6	V	2
Oscillator Input	V_7		–	1.4	–		
Oscillator Output	V_8		–	2.35	–		
Balance (ACC Control)	V_9		–	1.65	–		
Chroma Output	V_{14}		–	4.6	–		
Currents:							
Total Supply	I_5		14	24	33		
Burst Separator Output	I_{11}	S_1 Closed	–	6.5	–	mA	
Band-Pass Ampl. Output	I_{13}		–	4.8	–		
Chroma Ampl. Output	I_{16}		–	1.27	–		
Dynamic Characteristics							
Oscillator Output	v_8	v_1 = 0 v_{p-p} v_1 = 1.25 v_{p-p}	0.8 –	1.2 2.5	– 3.5	v_{p-p}	4
Chroma Output:							
100%	v_{14}	v_1 = 1.25 v_{p-p}	0.5	1.0	–	v_{p-p}	3, 4
Killed		v_1 = 0.025 v_{p-p}	–	–	12		
ACC Detector Output	v_2	v_1 = 1.25 v_{p-p}	–	0.9	–	V	4
Small-Signal Input Resistance (Term. No.1)	r_i		–	50	–	kΩ	–
Small-Signal Input Capacitance (Term. No.1)	c_i		–	2.4	–	pF	
Small-Signal Output Impedance (Term. No.14)	r_o		–	250	–	Ω	

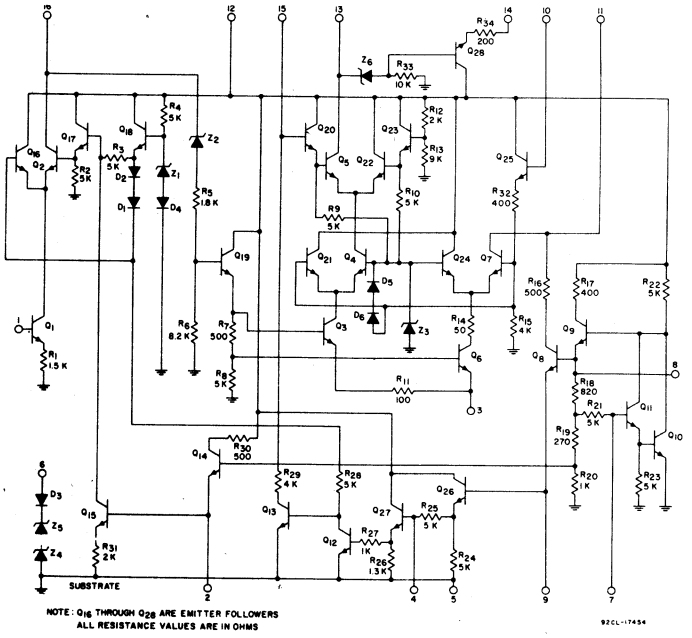


Fig. 1 - CA3066 schematic diagram.

CA3066

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

Supply Voltages and Currents (see charts below)

Device Dissipation:
Up to T_A = 70°C . . . . . 600 mW
Above T_A = 70°C . . . . derate linearly 7.7 mW/°C

Ambient Temperature Range:
Operating . . . . . –40 to +85 °C
Storage . . . . . –65 to +150 °C

Lead Temperature (During soldering for 10s max. at not less than 1/32" from package) . . . +265 °C

Voltage with respect to Terminal No. 5.

Terminal No.	$V_{min.}$ (volts)	$V_{max.}$ (volts)
6	See Note N1	
7	–	–
8	–	–
9	—	–
10	–5.0	N2
11	0.0	18.0
12	0.0	12.0
13	0.0	15.0
14	–	–
15	0.0	N2
16	0.0	15.0
1	–5.0	5.0
2	–	–
3	–	–
4	–	–

Current

Terminal No.	I_I mA	I_O mA
6	20	0.1
7	5	0.1
8	1	2
9	0.1	2
10	1	0.1
11	10	1
12	50	1
13	10	1
14	0.1	6
15	3	1
16	6	1
1	1	0.1
2	0.1	2
3	0.1	20
4	1	1

N1 Terminal No. 6 is connected to a zener reference element, that, if used, should be biased by a positive voltage through a resistor that limits the current to a value which is less than the maximum current rating of terminal No. 6.

N2 The upper voltage limit cannot exceed the power supply input voltage at terminal 12.

CA3066, CA3067

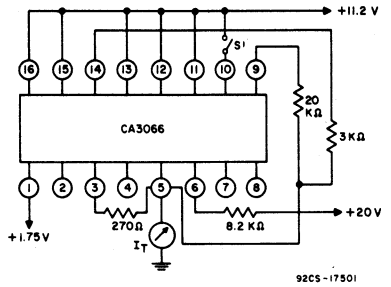


Fig. 2 - Static characteristics test circuit for CA3066.

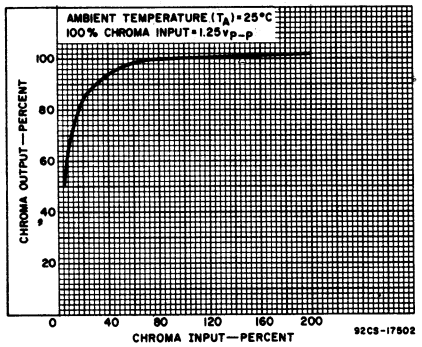


Fig. 3 - Typical ACC characteristic of chroma output vs chroma input for CA3066.

CA3067 CHROMA DEMODULATOR

The CA3067 contains the separate functional systems of a dc tint control and a demodulator. The phase shift of the tint amplifier system is accomplished by functional control of the fixed phase signal from the CA3066 oscillator output. This regenerated reference subcarrier is applied to terminal No. 3 and driven differentially into phase shift circuits. The tint adjustment controls the vector addition of phase shifted signals after which a limiting amplifier removes any remaining amplitude modulation. The output of the tint amplifier at terminal No. 1 is phase separated for the required reference subcarrier phase at terminal No. 6 and No. 12 (terminal No. 12 lags terminal No. 6 by approximately 76°). These terminals are inputs to the demodulator drive amplifiers. The demodulators consist of two sets of balanced detectors which receive their reference subcarrier from the demodulator drive amplifiers. The chroma signal input from the CA3066 is applied to terminal No. 14. The chroma signal differentially drives the demodulators. The demodulation components are matrixed and dc-shifted in voltage to give R–Y, G–Y, and B–Y color difference components with close dc balance and proper amplitude ratios. The output amplifiers of the CA3067 are specially designed to meet the low-impedance driving source requirements of the high-level color output amplifiers. A special feature of the CA3067 is R–C filtering of high frequency demodulation components. Terminal No. 4 is a zener diode for use as a regulated voltage reference at 11.9V. When the zener reference element is not used, the power supply should be maintained at +11.2 ±0.5 volts.

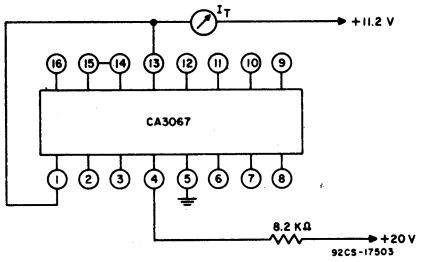


Fig. 5 - Static characteristics test circuit for CA3067.

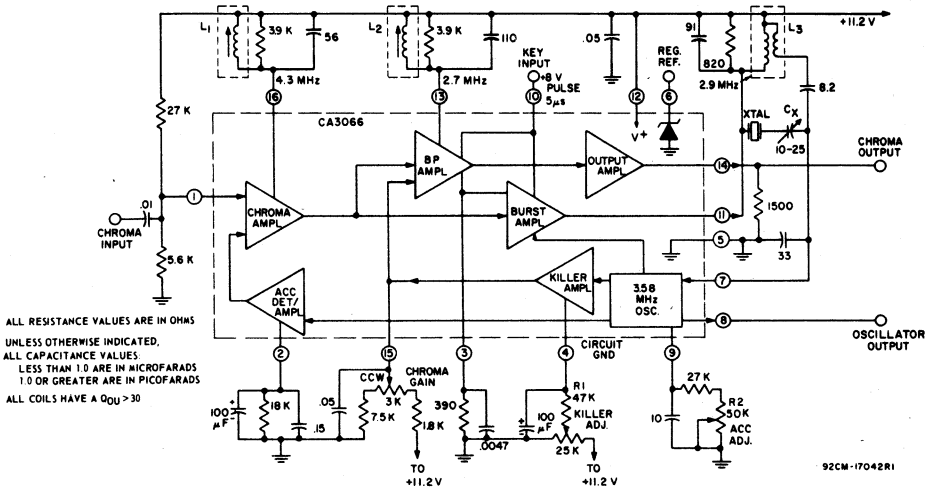


Fig. 4 - Dynamic characteristics test circuit for CA3066.

DYNAMIC CHARACTERISTICS TEST PROCEDURE

Steps 1, 2, and 3 are performed with no Chroma input ($v_1 = 0$)

1. Adjust ACC potentiometer for $V_2 = +0.65V$.
2. Adjust Killer potentiometer for $V_4 = +1.2V$.
3. Adjust capacitor C_x (crystal trimmer) so that frequency of oscillator is 3.579545 MHz.
4. Unless otherwise noted, the chroma gain control is at maximum gain (fully clockwise).
5. The chroma input test signal is a 52.5 μs "line" at subcarrier frequency, and 10 cycles of burst at 46.5% of the "line" amplitude. The chroma input (v_1) is in peak-to-peak volts of "line" amplitude.
6. The chroma output (v_{14}) is the same as the chroma input (v_1) except that the burst is removed and keying overshoot occurs in the retrace period. The chroma output is in peak-to-peak volts of "line" amplitude.
7. The oscillator output (v_8) is the CW output at terminal No. 8 and is in peak-to-peak volts. Some modulation of oscillation dampening between burst injection is visible.

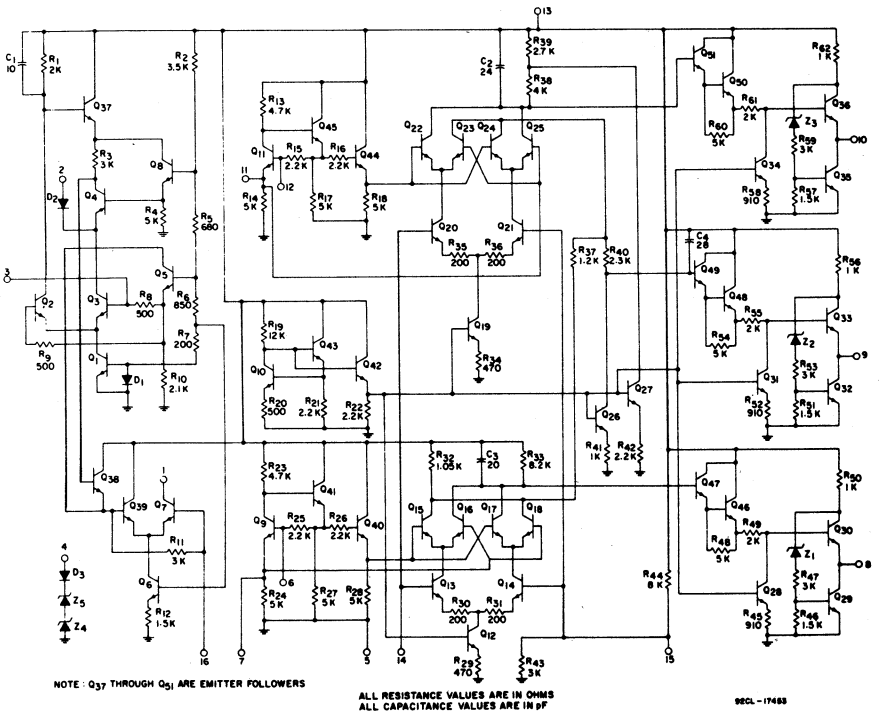


Fig. 6 - CA3067 schematic diagram.

CA3066, CA3067

ELECTRICAL CHARACTERISTICS at T_A = 25°C and V^+ = 11.2 V

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST FIG. AND CURVES
Static Characteristics							
Voltages:							
Tint Control Input	V_2	I_2 = 0.25 mA	–	3.5	–		
Reference Subcarrier	V_3		–	2.1	–		
Zener Regulator Ref.	V_4		10.6	11.9	12.6	V	9
B–Y, R–Y Oscillator Ref. Inputs	V_6, V_{12}		–	5.7	–		
Balance (B–Y, R–Y)	V_7, V_{11}		–	5.0	–		
B–Y, G–Y, R–Y Outputs	V_8, 9, 10		4.2	5.0	5.8		9, 11, 12
Difference Outputs*	ΔV_8, ΔV_9, ΔV_{10}		–0.3	–	0.3		
Chroma Inputs	V_{14}, V_{15}		–	3.0	–		9
Tint Ampl. Balance	V_{16}		–	4.7	–		
Currents:							
Tint Ampl. Output (min.)	I_1(min.)	V_{16} = 8 V	0.16	0.37	–	mA	
Total Supply	$I_1 + I_{13}$		15	24	33		
Dynamic Characteristics							
Tint Amplifier Output Sensitivity	V_1	V_3 = 7 mV (RMS)	160	250	–	mV (RMS)	
Limiting Knee		V_3 = 35mV (RMS)	–	300	–		
Limiting		V_3 = 350mV (RMS)	–	–	380		
Tint Ampl. Phase Ref.▲	ϕ_6	V_3 = 70mV (RMS)	185	220	235	deg.	
Tint Ampl. Phase Shift‡	$\Delta\phi_6$	V_3 = 70mV (RMS)	90	105	–	deg.	
Demodulated Chroma Output:							
R–Y	V_{10}	V_3 = 70mV (RMS) V_{14} = 35mV (RMS)	150	250	–	$V_{(RMS)}$	
Ratio of G–Y to R–Y	V_9/V_{10}		0.28	0.36	0.44		
Ratio of B–Y to R–Y	V_8/V_{10}		1.0	1.2	1.4		
Color Difference Output BW at 3.3 dB	$BW_{Diff.}$		450	550	–	kHz	10
Color Difference Outputs (max. input signals):							
R–Y	v_{10}	V_3 = 70mV (RMS) V_{14} = 212mV (RMS)	–	3.0	–	v_{p-p}	
G–Y	v_9		–	1.1	–		
B–Y	v_8		–	3.6	–		
Small Signal Input Resistance Terminal No. 3	r_i		–	550	–	Ω	
Terminal Nos. 6 & 12			–	22	–		
Small Signal Output Resistance Terminal Nos. 8, 9, & 10	r_o		–	5	–		

$$*\Delta V_8 = V_8 - \left(\frac{V_8 + V_9 + V_{10}}{3}\right), \Delta V_9 = V_9 - \left(\frac{V_8 + V_9 + V_{10}}{3}\right), \Delta V_{10} = V_{10} - \left(\frac{V_8 + V_9 + V_{10}}{3}\right)$$

▲ Terminal No. 3 is phase reference
‡ read phase shift as tint control is varied

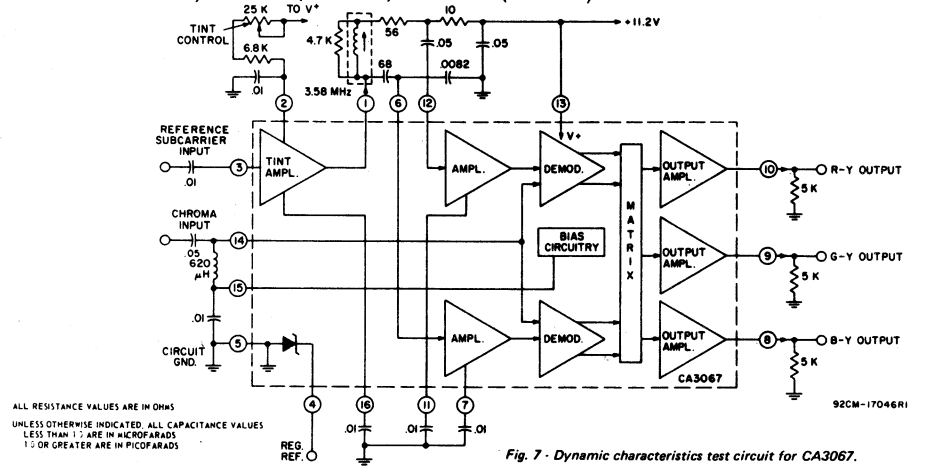


Fig. 7 - Dynamic characteristics test circuit for CA3067.

DYNAMIC CHARACTERISTICS TEST PROCEDURE

1. The reference subcarrier input (v_3) is a 3.58 MHz CW signal from a 50Ω source.
2. The chroma input (v_{14}) is a 3.53 MHz CW signal from a 50Ω source.
3. Phase and amplitude at terminal Nos. 1, 3, 6 and 12 are measured with a vector voltmeter (HP8405A or equivalent).
4. Signals at terminal Nos. 8, 9, and 10 are measured with an ac voltmeter (HP400E or equivalent) or an oscilloscope.
5. Unless otherwise noted the Tint control is at maximum resistance.

CA3067

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

Supply Voltages and Currents (see charts below)
Device Dissipation:
Up to T_A = 70°C . . . . . 600 mW
Above T_A = 70°C . . . . derate linearly 7.7 mW/°C
Ambient Temperature Range:
Operating . . . . . –40 to +85 °C
Storage . . . . . –65 to +150 °C
Lead Temperature (During soldering for 10s max. at not less than 1/32" from package) . . . +265 °C

Voltage with respect to Terminal No. 5

Terminal No.	$V_{min.}$ (volts)	$V_{max.}$ (volts)
6	0	N2
7	0	N2
8	0	N2
9	0	N2
10	0	N2
11	0	N2
12	0	N2
13	0	12
14	–3	N2
15	0	N2
16	N3	N3
1	0	15
2	0	N2
3	0	5
4	N1	

Current

Terminal No.	I_i (mA)	I_o (mA)
6	3	3
7	3	3
8	20	20
9	20	20
10	20	20
11	3	3
12	3	3
13	50	1
14	1	0.1
15	6	2
16	N3	N3
1	3	3
2	3	0.1
3	3	3
4	20	0.1

N1 Terminal No. 4 is connected to a zener reference element, that, if used, should be biased by a positive voltage through a resistor that limits the current to a value which is less than the maximum current rating of terminal No. 4.
N2 The upper voltage limit cannot exceed the power supply input voltage at terminal 13.
N3 Terminal No. 16 should be bypassed for normal operation.

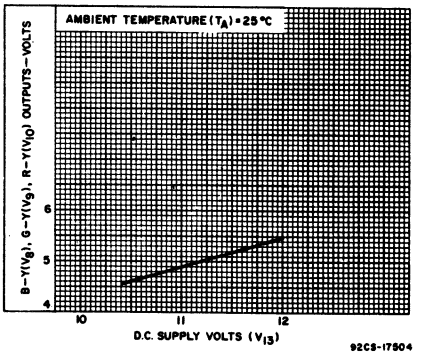


Fig. 8 - DC voltage at color-difference outputs vs supply voltage for CA3067.

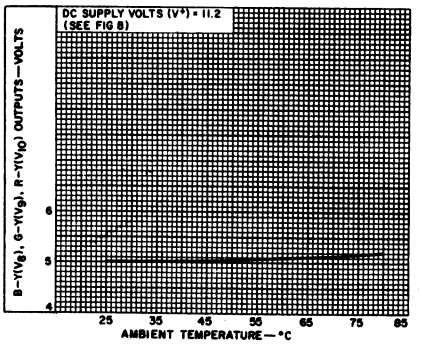


Fig. 9 - Temperature drift of DC voltage at color-difference outputs for CA3067.

CA3068

Television Video IF System

RCA-CA3068 is a monolithic integrated circuit that incorporates an entire video TV-IF subsystem on a single chip. Innovations in integrated circuit design, in addition to the many active devices and closely matched components utilized in the circuit, make the CA3068 ideally suited for use in color and black-and-white TV receivers.

The primary functions performed by the IF subsystem are video IF amplification, linear detection, video output amplification, AGC from a keyed supply, AGC delay for tuner, sound carrier detection, sound carrier amplification, and a buffered AFT output. The advanced circuit design of the CA3068 also includes secondary functions for improved noise immunity and minimal airplane flutter. An isolated zener reference diode, incorporated in the IC, provides a convenient and economical means for controlling the regulated voltage supply. The inherent wide bandwidth capability (10-70 MHz) and high overall gain (87 dB) make the CA3068 suitable for other AM IF applications whose frequencies range within this bandwidth.

The CA3068 utilizes a unique 20-lead quad-in-line plastic package. This package also includes a wrap-around shield that serves to minimize interlead capacitances.

FEATURES:

- High-gain wide-band IF amplifier: 75 dB typ. at 45 MHz
- Gain reduction with excellent stability: 50 dB typ. at 45 MHz
- Video detector with linear characteristics
- Video amplifier: 12 dB gain
- Impulse noise limiter
- Keyed AGC with noise immunity circuits
- Delayed AGC for tuner
- Buffered AFT output
- Separate sound IF intercarrier amplification
- Sound carrier detector
- 4.5 MHz sound carrier amplifier
- Isolated zener reference diode for regulated voltage supply
- See ICAN-6303, "A Single IC for the Complete PIX-IF System in TV Receivers" for Schematic Diagram

MAXIMUM RATINGS, *Absolute Maximum Values, at* $T_A = 25°C$

DC Supply Voltage:		
Between Terminals 15 and 5*	14.3	V
Terminal 7 (Collector to ground)	20	V
Terminal 9 (Collector to ground)	20	V
DC Current (into Terminal 18)	2	mA
Device Dissipation:		
Up to $T_A = 60°C$	600	mW
Above $T_A = 60°C$	derate linearly 6.7 mW/°C	
Ambient Temperature Range:		
Operating	−40 to +85	°C
Storage	− 65 to +150	°C
Lead Temperature (During soldering):		
At distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265	°C

* This rating does not apply when using the internal zener reference in conjunction with the pass transistor.

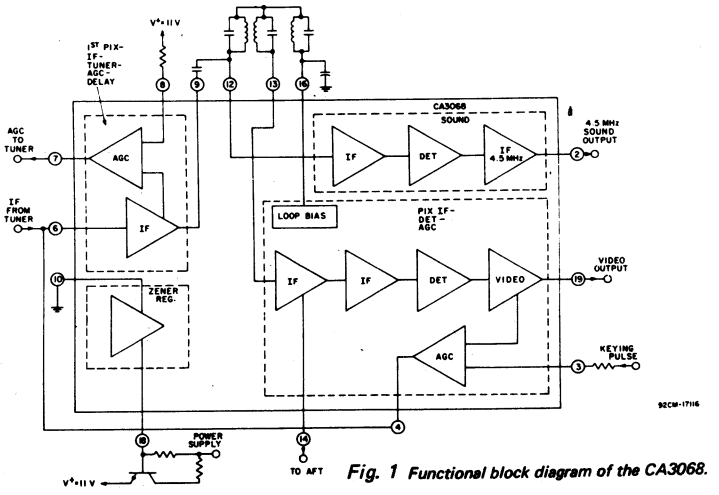


Fig. 1 Functional block diagram of the CA3068.

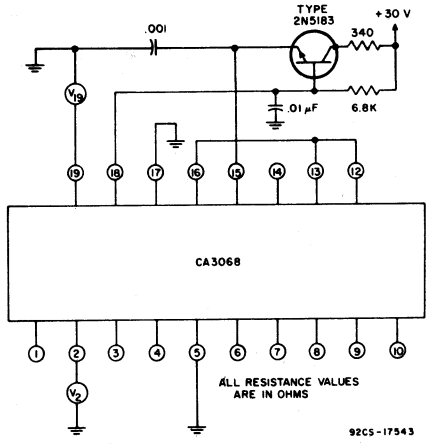
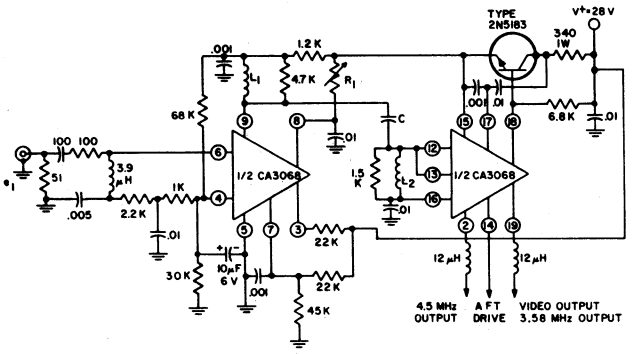
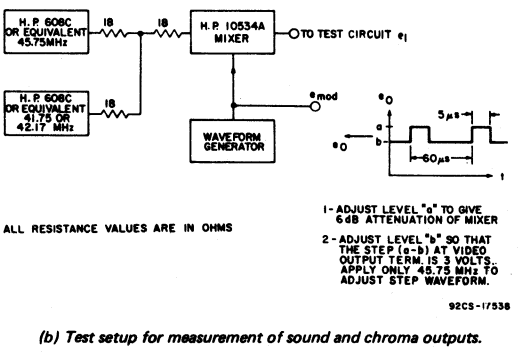


Fig. 2 – Test circuit for measurement of white level (V_{19}) and terminal 2 voltage (V_2).



(a) Test setup for measurement of video sensitivity, sync. tip level, delay bias, AFT drive voltage.



(b) Test setup for measurement of sound and chroma outputs.

Fig. 3 – Typical dynamic test circuit diagrams.

CA3068

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Static (DC) Characteristics						
Quiescent Circuit Current	I_{15}	–	15	–	45	mA
DC Voltages:						
Terminal 2 (Sound)	V_2	–	–	6	–	V
Terminal 3 (Keying Input)	V_3	–	6.4	–	10	V
Terminal 7 (1) (AGC)	V_7	–	16	–	21	V
Terminal 7 (2) (AGC)	V_7	–	–	1	–	V
Terminal 8 (AGC Delay)	V_8	–	–	4	–	V
Terminal 9 (Cascode Collector)	V_9	–	–	8.5	–	V
Terminal 16 (Bias)	V_{16}	–	1.1	–	2.3	V
Terminal 18 (Zener)	V_{18}	$V_5 = V_{17} = 0$ V, $I_{18} = 1$ mA	10.6	11.9	13.2	V
Terminal 19 (White Level)	V_{19}	–	6	–	10	V
Dynamic Characteristics						
Video Sensitivity	e_I	f_O = 45.75 MHz, Mod. (AM) = 85% at 400 Hz; Adjust e_I for 4 V_{p-p} at Term. 19	40	100	200	μV
Sync. Tip Level Voltage	V_{19}	f_O = 45.75 MHz, e_I(CW) = 10 mV	0.4	0.8	1.6	V
Automatic Fine Tuning (AFT) Drive Level Voltage	V_{14}		–	15	–	mV
Delay Bias Voltage:	V_7					
At e_I = 10 mV		f_O = 45.75 MHz, e_I(CW) = 20 mV;	16	–	–	V
At e_I = 30 mV		Adjust R_1 for V_7 = 14 V	0.5	–	2	V
3.58 MHz Chroma Output Voltage	V_{19}	f_O = 45.75 MHz, e_I(step mod.) = 10 mV; f_1 = 42.17 MHz, e_I(step mod.) = 3.33 mV	0.5	0.8	–	V
4.5-MHz Sound Output Voltage	V_2	f_O = 45.75 MHz, e_I(step mod.) = 10 mV; f_2 = 41.25 MHz, e_I(step mod.) = 2.5 mV	50	200	–	mV
Parallel Input Impedance:						
Resistance at Term. 6	R_{I-6}	f_O = 45.75 MHz Impedance and Admittance measured at bias conditions as developed by circuit shown in Fig. 7	4	–	–	kΩ
Capacitance at Term. 6	C_{I-6}		–	2	–	pF
Resistance at Term. 12	R_{I-12}		–	4.5	–	kΩ
Capacitance at Term. 12	C_{I-12}		–	4	–	pF
Resistance at Term. 13	R_{I-13}		–	5	–	kΩ
Capacitance at Term. 13	C_{I-13}		–	4	–	pF
Parallel Output Impedance:						
Resistance at Term. 9	R_{O-9}		30	–	–	kΩ
Capacitance at Term. 9	C_{O-9}		–	3	–	pF
Cascode Transfer Characteristics: Magnitude of Forward Transadmittance	$\lvert Y_f \rvert$		–	50	–	mmho
Reverse Transfer Capacitance	C_r		–	0.001	–	pF

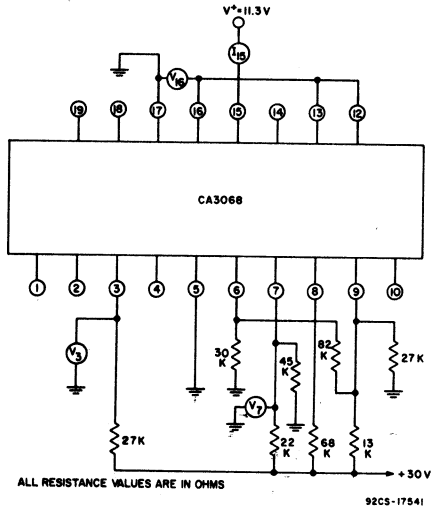


Fig. 4 – Test circuit for measurement of quiescent current (I_{15}), keying terminal voltage (V_3), bias voltage (V_{16}), AGC terminal voltage 1 (V_7), and cascode collector voltage (V_9)

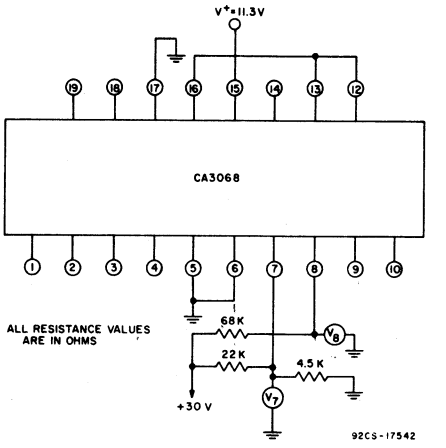


Fig. 5 – Test circuit for measurement of AGC terminal voltage 2 (V_7) and terminal 8 voltage (V_8).