CA3070, CA3071, CA3072

Television Chroma System

The RCA CA3070, CA3071, and CA3072 are monolithic silicon integrated circuits that constitute a complete chroma system for color television receivers. The CA3070 is a complete subcarrier regeneration system featuring a new concept of phase control applied to the oscillator circuit. The CA3071 is a chroma amplifier system and the CA3072 performs the demodulation function.

The CA3070 utilizes the 16-lead plastic dual-in-line package; the CA3071 and CA3072 are supplied 14-lead plastic dual-in-line packages.

SYSTEM FEATURES

CA3070

- Voltage Controlled Oscillator
- Keyed APC & ACC Detectors
- DC Hue Control
- Shunt Regulator

CA3071

- ACC Controlled Chroma Amplifier
- DC Chroma Gain Control
- Color Killer
- Amplifier Short-Circuit Protection

CA3072

- Synchronous Detector with Color Difference Matrix
- Emitter-Follower Output Amplifiers with Short-Circuit Protection

CA3070 Chroma Signal Processor

The CA3070 is a complete subcarrier regeneration system with automatic phase control applied to the oscillator. An amplified chroma signal from the CA3071 is applied to terminals No. 13 and No. 14, which are the automatic phase control (APC) and the automatic chroma control (ACC) inputs. APC and ACC detection is keyed by the horizontal pulse which also inhibits the oscillator output amplifier during the burst interval.

The ACC system uses a synchronous detector to develop a correction voltage at the differential output terminal Nos. 15 & 16. This control signal is applied to the input terminal Nos. 1 & 14 of the CA3071. The APC system also uses a synchronous detector. The APC error voltage is internally coupled to the 3.58 MHz oscillator at balance; the phase of the signal at terminal No. 13 is in quadrature with the oscillator.

To accomplish phasing requirements, an RC phase shift network is used between the chroma input and terminal Nos. 13 and 14. The feedback loop of the oscillator is from terminal Nos. 7 and 8 back to No. 6. The same oscillator signal is available at terminal Nos. 7 and 8, but the dc output of the APC detector controls the relative signal levels at terminal Nos. 7 or 8. Because the output at terminal No. 8 is shifted in phase compared to the output at terminal No. 7, which is applied directly to the crystal circuit, control of the relative amplitudes at terminal Nos. 7 and 8 alters the phase in the feedback loop, thereby changing the frequency of the crystal oscillator. Balance adjustments of dc offsets are provided to establish an initial no-signal offset control in the ACC output, and a no-signal, on-frequency adjustment through the APC detector-amplifier circuit which controls the oscillator frequency. The oscillator output stage is differentially controlled at terminal Nos. 2 and 3 by the hue control input to terminal No. 1. The hue phase shift is accomplished by the external R, L, and C components that couple the oscillator output to the demodulator input terminals. The CA3070 includes a shunt regulator to establish a 12-volt dc supply.

Maximum Voltage and Current Ratings at T_A = +25°C

Voltage▲			Current		
Terminal No.	Min. Volts	Max. Volts	Terminal No.	I_I mA	I_O mA
1	0	*	1	20	1
2	0	+16	2	–	–
3	0	+16	3	–	–
4	–5	N2	4	20	1
6	–	–	10	N3	1
7	–	–	11	–	–
8	–	–	12	–	–
10	0	N3	13	20	1
11	0	N1	14	20	1
12	0	N1			
13	0	N1			
14	0	N1			
15	0	+16			
16	0	+16			

▲ With respect to terminal No.5 and with terminal No. 10 connected through 470Ω to +24 V.

N1 Regulated voltage at terminal No. 10.

N2 Controlled by max. input current.

N3 Limited by dissipation.

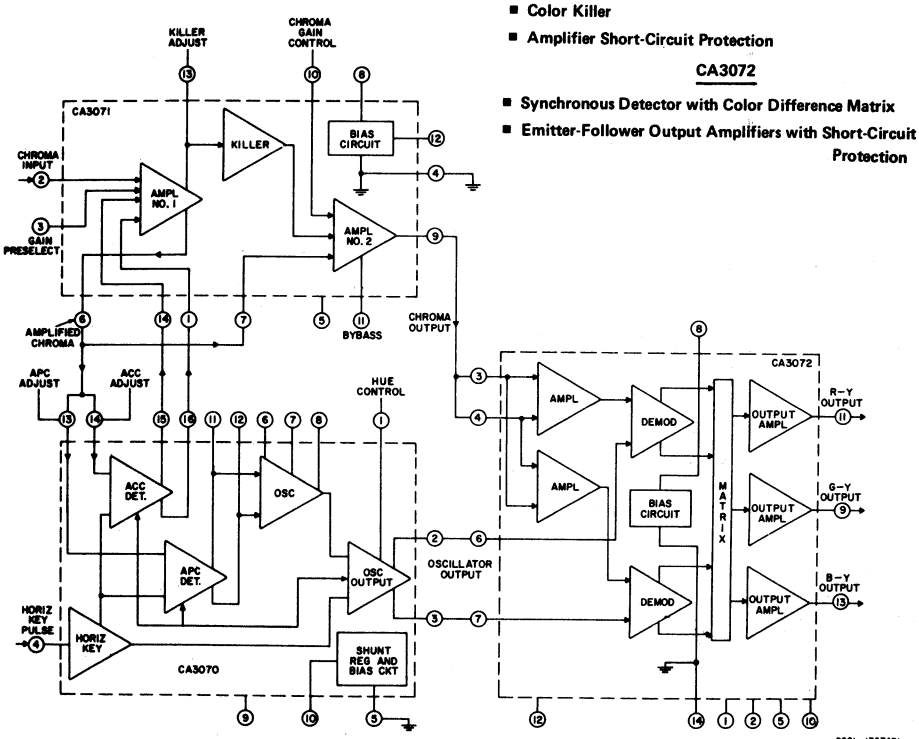


Fig. 1 – Simplified block diagram of TV chroma system.

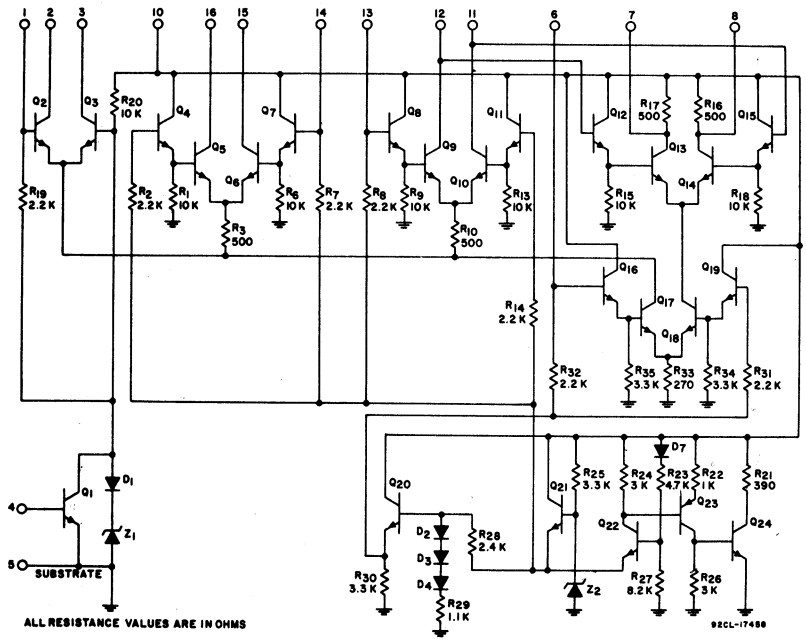


Fig. 2 – Schematic diagram CA3070.

CA3070, CA3071, CA3072

MAXIMUM RATINGS, *Absolute Maximum-Values at T_A = 25°C*

Device Dissipation:
- Up to T_A = +70°C ..... 530 mW
- Above T_A = +70°C ... Derate Linearly at 6.7 mW/°C

Ambient Temperature Range:
- Operating ..... −40 to +85 °C
- Storage ..... −65 to +150 °C

Lead Temperature (During Soldering):
- At distance 1/32 in. (3.17 mm) from seating plane for 10 s max. ..... +265 °C

ELECTRICAL CHARACTERISTICS, at T_A = 25°C and V^+ = +24 V unless otherwise specified

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS CA3070 MIN.	LIMITS CA3070 TYP.	LIMITS CA3070 MAX.	UNITS	TEST CIRCUITS FIG.
Static Characteristics							
Voltage:							
Hue Control	V_1	Switch in position 2	6.9	7.7	8.6	V	3c
Oscillator Input	V_6		–	2.8	–	V	3a
APC Input	V_{13}		–	6.5	–	V	3a
Regulator	V_{10}	V^+ = 21 V	11	12.3	13.5	V	3a
Regulator Change	V_{10}	V^+ = 27 V	−0.2	–	+0.2	V	3a
Horizontal Key Input	V_4	I_4 = −10 μA	5	—	—	V	3a
Currents:							
Oscillator Output	I_2		–	5.8	–	mA	3c
APC Output	I_{11}, I_{12}		–	1.45	—	mA	3b
ACC Output	I_{15}, I_{16}		–	1.45	–	mA	3b
Dynamic Characteristics							
Oscillator Outputs:							
Terminal No. 2	V_2	S_1 in position 1	0.75	1.0	–	V_{p-p}	4
Terminal No. 3	V_3	S_1 in position 2	0.75	1.0	–	V_{p-p}	4
ACC Detected Output	V_{16}−V_{15}	S_1 in position 1	115	150	–	mV	4
Oscillator Pull-In Range	–		–	±400	–	Hz	4

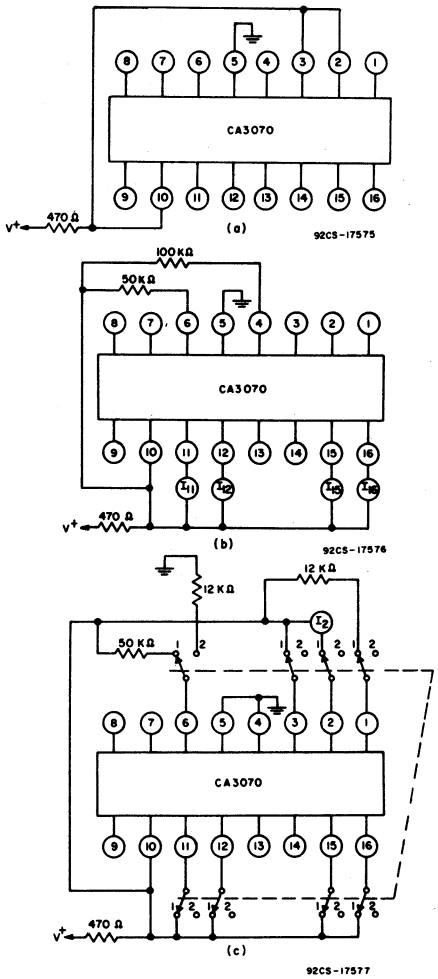
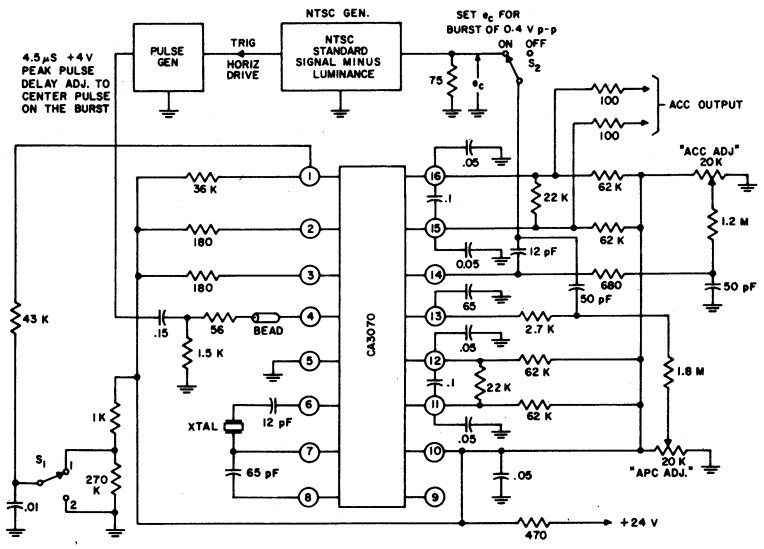


Fig. 3 – Static characteristics test circuits.



NOTES:
1. ALL RESISTANCES IN OHMS.
2. UNLESS OTHERWISE SPECIFIED ALL CAPACITANCES ARE IN MICROFARADS.
3. V_2 & V_3 MEAS'D WITH LOW-CAPACITY SCOPE PROBE ≤ 20 pF.

92CM-17578R1

Fig. 4 – CA3070 Dynamic test circuit.

Dynamic Test Initial Adjustments

1. APC ADJUST: With S2 in "OFF" position adjust the "APC ADJ" potentiometer to set oscillator frequency at 3.579545 MHz ±25 Hz. With S1 in position 1 measure frequency at terminal No. 2 output, using crystal probe shown in Fig. 6.
2. ACC ADJUST: With S2 in "OFF" position adjust "ACC ADJ" potentiometer to give an ACC output reading of 0 ±2 mV.

Procedure to Pull-in Range Measurement

1. Set S1 in position 1 and connect the crystal probe to terminal No. 2.
2. Turn S2 to "OFF" and set "APC ADJ." arm to ground.
3. Turn S2 to "ON" and gradually adjust "APC ADJ" until oscillator "locks" as witnessed by a sharp increase in ACC output voltage between terminal Nos. 15 and 16.
4. Turn S2 to "OFF" and adjust capacitor Cp of crystal probe for maximum deflection on Ballantine Meter.
5. Switch Ballantine meter to "Amplifier" position and read oscillator frequency on counter.
6. Repeat steps 2 – 5 with "APC ADJ" arm set to terminal No. 10 instead of to ground.

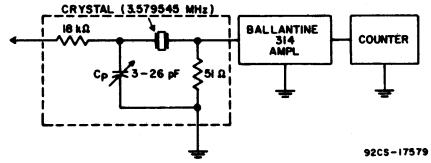


Fig. 5 – Crystal probe for frequency measurements.

CA3070, CA3071, CA3072

CA3071 Chroma Amplifier

The CA3071 is a combined two-stage chroma amplifier and functional control circuit. The input signal is received from the video amplifier and applied to terminal No. 2 of the input amplifier stage. The first amplifier stage is part of the ACC system and is controlled by differential adjustment from the ACC input terminal Nos. 1 and 14. The output of the 1st amplifier is directed to terminal No. 6 from where the signal may be applied to the ACC detection system of the CA3070 or an equivalent circuit. The output at terminal No. 6 is also applied to terminal No. 7 which is the input to the 2nd amplifier stage. Another output of the 1st amplifier at terminal No. 13 is directed to the killer adjustment circuit.

The dc voltage level at terminal No. 13 rises as the ACC differential voltage decreases with a reduction in the burst amplitude. At a pre-set condition determined by the killer adjustment resistor the killer circuit is activated and causes the 2nd chroma amplifier stage to be cut off. The 2nd chroma amplifier stage is also gain controlled by the adjustment of dc voltage at terminal No. 10. The output of the 2nd chroma amplifier stage is available at terminal No. 9. The typical output termination circuit that is shown, provides differential chroma drive signal to the demodulator circuit. Both amplifier outputs utilize emitter-followers with short-circuit protection.

MAXIMUM RATINGS, *Absolute Maximum-Values at $T_A = 25°C$*

DC Supply Voltage (Terminal 8 to Terminal 4)	30	VDC
Device Dissipation:		
Up to $T_A = +70°C$	530	mW
Above $T_A = +70°C$	Derate Linearly at 6.7	mW/°C
Ambient Temperature Range:		
Operating	−40 to +85	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/32 in (3.17 mm) from seating plane for 10 s max.	+265	°C

Maximum Voltage and Current Ratings @ $T_A = +25°C$

Current			Voltage*		
Terminal No.	I_I mA	I_O mA	Terminal No.	MIN VOLTS	MAX VOLTS
1	5	1.0	1	−5	+15
2	5	1.0	2	−5	+5
3	10	10	3	0	+2
6	1.0	20	6	0	+24
7	5	1.0	7	−5	+5
9	1.0	20	8	0	+30
12	1.0	5	9	0	+24
14	5	1.0	10	0	+24
			11	0	+24
			12	0	+20
			13	0	+20
			14	−5	+15

* With reference to terminal No. 4 and with +24 V on terminal No. 8 except for the rating given for terminal No. 8.

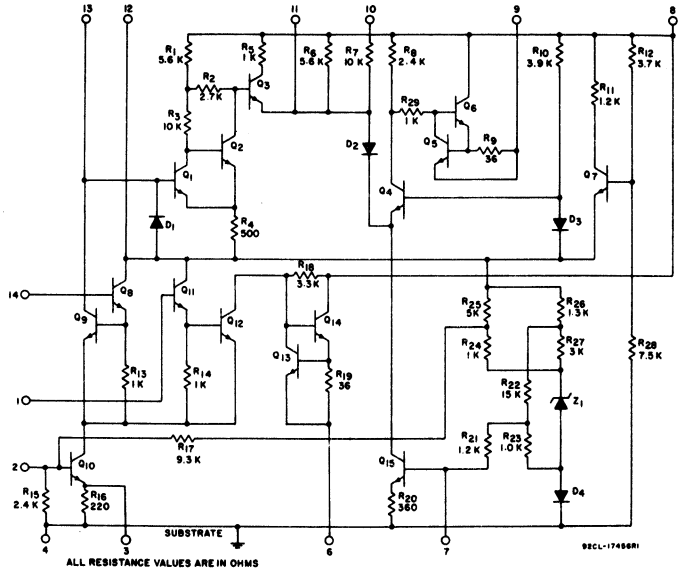


Fig. 6 -Schematic diagram for CA3071.

ELECTRICAL CHARACTERISTICS, at $T_A = 25°C$

CHARACTERISTICS	SYMBOLS (Measure)	SPECIAL TEST CONDITIONS	LIMITS CA3071 MIN.	LIMITS CA3071 TYP.	LIMITS CA3071 MAX.	UNITS	CURVES & TEST CIRCUITS FIG.
Static Characteristics							
Voltages							
Bias Reference Terminal	V_{12}	S_1 Open, S_2 Open	–	17.3	–	V	7
Ampl. No. 1 Chroma Input	V_2	S_1 Open, S_2 Open	–	1.75	–		
Ampl. No. 1 Chroma Output Balanced	V_6	S_1 Open, S_2 Open	–	20	–		
Unbalanced	V_6	S_1 Open, S_2 Closed	–	13.5	–		
Ampl. No. 2 Chroma Input	V_7	S_1 Open, S_2 Open	–	1.5	–		
Ampl. No. 2 Chroma Output	V_9	S_1 Closed, S_2 Open	–	20.6	–		
Supply Current	I_T	S_1 Open, S_2 Open	17	24.5	31	mA	
Dynamic Characteristics							
Amplifier No. 1 Voltage Gain	A_{V1}	E_g = 30 mV_{RMS} Measure v_6	14	–	–	dB	8
Amplifier No. 2 Voltage Gain	A_{V2}	V_g = 1.0 V (RMS) Measure v_7	–	14	–	dB	
Max. Chroma Output Voltage	v_9		–	2	–	V_{RMS}	11
10% Chroma Gain Control Reference Voltage	$V_8 - V_{10}$	E_g = 50 mV_{RMS}, adjust Chroma Gain Control to Change v_9 to 10% of Maximum Chroma Output	2.1	3.8	6.8	V	8
Output Voltage, Killer Off	v_9	S_1 in Position 2 E_g = 50 mV_{RMS}, adjust "Killer Adjust" for an abrupt decrease in V_9	..	–	12	mV RMS	
Output Voltage, Chroma Off	v_9	E_g = 50 mV_{RMS}, adjust Chroma control to min. Chroma Output	–	–	12	mV RMS	
Bandwidth: Amplifier No. 1	BW		–	12	–	MHz	9, 10
Amplifier No. 2			–	30	–		
Ampl. No. 1 Input Impedance	r_{i1}		–	2	–	kΩ	8
	c_{i1}		–	4	–	pF	
Ampl. No. 1 Output Impedance	r_{o1}		–	85	–	Ω	
Ampl. No. 2 Input Impedance	r_{i2}		–	2.1	–	kΩ	
	c_{i2}		–	3.5	–	pF	
Ampl. No. 2 Output Impedance	r_{o2}		–	85	–	Ω	

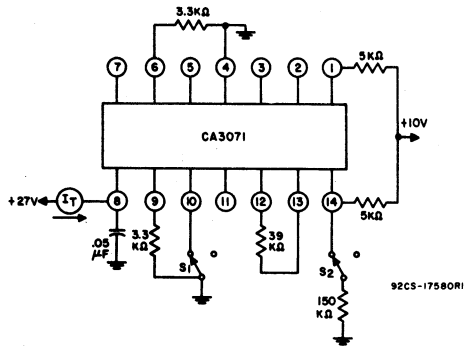
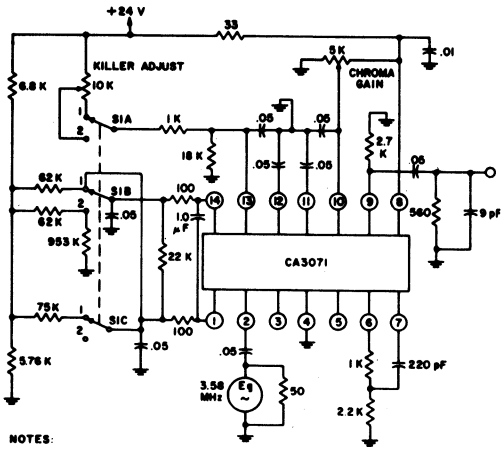


Fig. 7 - Static characteristics test circuit–CA3071.



NOTES:
1. SWITCH SI IN POSITION 1 UNLESS OTHERWISE NOTED IN TABLE OF DYNAMIC CHARACTERISTICS
2. CHROMA GAIN CONTROL SET TO GROUND UNLESS OTHERWISE NOTED IN TABLE OF DYNAMIC CHARACTERISTICS
3. ALL RESISTANCES IN OHMS
4. ALL CAPACITANCES ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED

92CM-17581

Fig. 8 – Dynamic characteristics circuit-CA3071.

CA3070, CA3071, CA3072

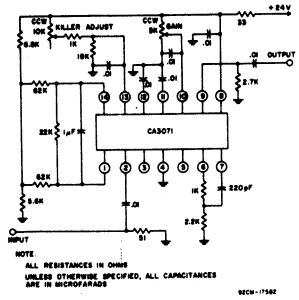


Fig. 9 – CA3071 Wideband amplifier circuit.

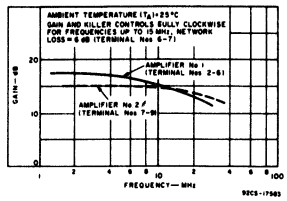


Fig. 10— Frequency response for wideband amplifier CA3071.

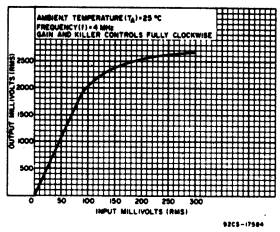


Fig. 11 – Typical CA3071 wideband amplifier linearity

CA3072 Chroma Demodulator

The CA3072 has two sets of synchronous detectors with matrix circuits to achieve the R-Y, G-Y, and B-Y color difference output signals. The chroma input signal is applied to terminal Nos. 3 and 4 while the oscillator injection signal is applied to terminal Nos. 6 and 7. The color difference signals, after matrix, have a fixed relationship of amplitude and phase nominally equal dc voltage levels. The outputs of the CA3072 are suitable for driving high level color difference or R, G, B output amplifiers. Emitter-follower output stages used to drive the high level color amplifiers have short-circuit protection.

MAXIMUM RATINGS, *Absolute Maximum-Values at T_A = 25° C*

DC Supply Voltage (Terminal 8 to Terminal 14)	27 V
Reference Input Voltage	5 V_{p-p}
Chroma Input Voltage	5 V_{p-p}
Device Dissipation:	
Up to T_A = +70°C	530 mW
Above T_A = +70°C	Derate Linearly at 6.7 mW/°C
Ambient Temperature Range:	
Operating	-40 to +85°C
Storage	-65 to +150°C
Lead Temperature (During Soldering):	
At distance 1/32 in (3.17 mm) from seating plane for 10 s max	+265°C

Maximum Voltage and Current Ratings at T_A = +25°C

Voltage*			Current		
Terminal No.	MIN VOLTS	MAX VOLTS	Terminal No.	I_I mA	I_O mA
3	0	+5	3	–	–
4	0	+5	4	–	–
6	0	+12	6	–	–
7	0	+12	7	–	–
8	0	+27	8	–	–
9	0	+20	9	1.0	20
11	0	+20	11	1.0	20
13	0	+20	13	1.0	20

*With reference to terminal No. 14 and with the voltage between terminal No. 8 and terminal No. 14 at +24 V except as given in rating for terminal No. 8.

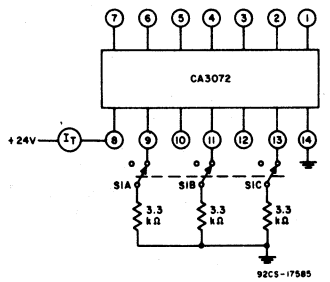


Fig. 13 — Static characteristics test circuit–CA3072.

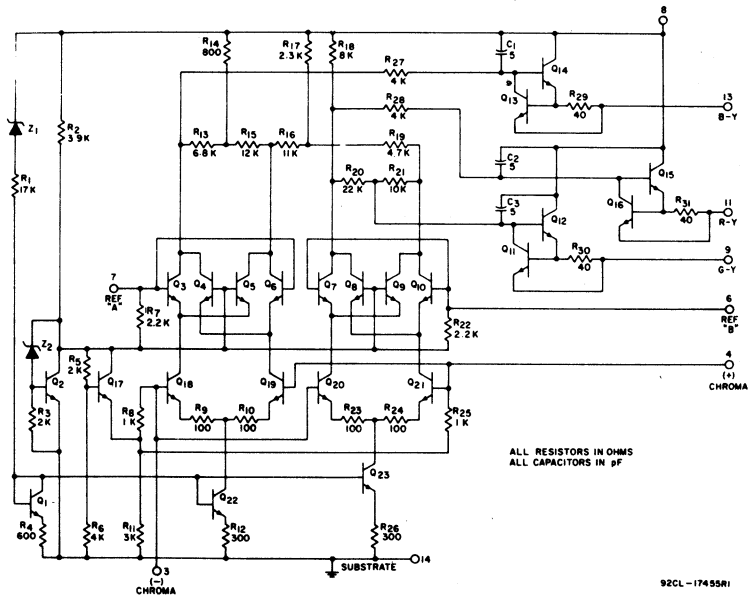


Fig. 12 — Schematic diagram for CA3072.

ELECTRICAL CHARACTERISTICS, at T_A = 25° C and V^+ = +24 V unless otherwise specified

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS CA3072 MIN.	TYP.	MAX.	UNITS	TEST CIRCUITS FIG.
Static Characteristics							
Supply Current With Output Loads	I_T	S_1 Closed	16.5	–	26.5	mA	13
With No Output Loads		S_1 Open	–	9			
G-Y, R-Y, B-Y Outputs	V_9, V_{11}, V_{13}	S_1 Closed	13.2	14.7	15.8	V	
Chroma Inputs	V_3, V_4	S_1 Open	–	3.3	–		
Reference Subcarrier	V_6, V_7	S_1 Open	–	6.2	–		
Dynamic Characteristics							
Demodulator Unbalance	V_9, V_{11}, V_{13}	$V_3 = V_4 = 0$	–	–	0.8	V_{p-p}	14
Maximum Color Difference Output Voltage	V_{13}	$V_3 = V_4 = 0.6$ V_{p-p}	8.0	–	–	V_{p-p}	
	V_{11}		5.5	–	–		
	V_9		1.2	–	–		
Chroma Input Sensitivity	V_3	Adjust e_c for 5.0 V_{p-p} @ term No. 13 (B-Y)	–	0.2	0.35		
Relative R-Y Output	V_{11}		3.5	–	4.2		
Relative G-Y Output	V_9		0.75	–	1.25		
V_{DC} Difference Between any two Output Terminals	$\lvert V_9\rvert - \lvert V_{11}\rvert$ $\lvert V_9\rvert - \lvert V_{13}\rvert$ $\lvert V_{11}\rvert - \lvert V_{13}\rvert$	e_c = 0	–	–	0.6	V	
Input Impedance Reference Subcarrier Inputs	r_i6, 7		–	1.7	–	kΩ	
	c_i6, 7		–	6	–	pF	
Input Impedance at Chroma Inputs	r_i3, 4		–	0.95	–	kΩ	
	c_i3, 4		–	6	–	pF	
Output Resistance	r_o9, r_o11, r_o13		–	180	–	Ω	

CA3070, CA3071, CA3072

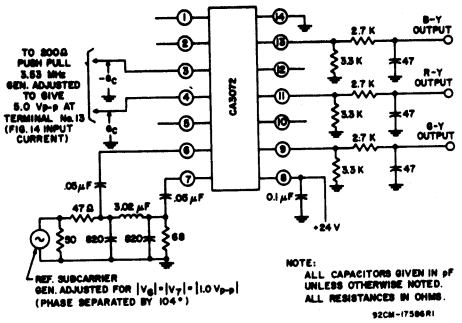


Fig. 14 - Dynamic characteristics test circuit for CA3072.

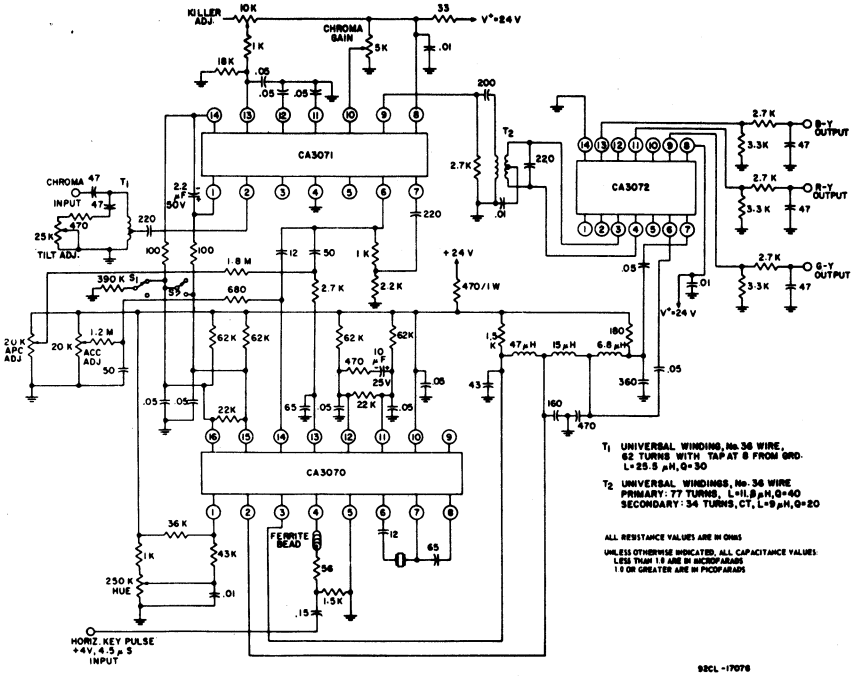


Fig. 15 – Typical chroma system for color-TV receivers utilizing RCA-CA3070, CA3071, and CA3072.

Application Information

TYPICAL APPLICATION CIRCUIT FOR THE CHROMA SYSTEM

The circuit of *Fig.15* is a complete signal processing system for color TV. The RCA types CA3070, CA3071 and CA3072 monolithic integrated circuits are respectively used as the subcarrier regenerator, chroma amplifier, and chroma demodulator.

The input to the system is the chroma signal which may be taken from the first or second video stage and is coupled into the CA3071 chroma amplifier through a bandpass filter. The outputs from the system are the color difference signals which are intended to drive high level amplifiers. Luminance mixing may be external to the picture tube or, the difference signals may be amplified and applied to the picture tube grid or cathode, where they are internally mixed with the luminance signal.

Other input requirements to the system are the power supply voltage of +24 volts and the horizontal keying pulse. The power supply voltage should be maintained within ±3 volts of the recommended value of +24 volts. The total current for the system is approximately 70 milliamperes. The horizontal keying pulse input to the subcarrier regenerator is approximately +4 volts peak and centered on the burst as seen at terminal Nos. 13 and 14 of the CA3070. The pulse width should be maintained as close as possible to the recommended value of 4.5 microseconds.

CA3070 Circuit Operation

The CA3070 circuit as shown in Fig. 2, consists of an oscillator, automatic phase control (APC) detector, automatic chroma control (ACC) detector, gated oscillator output amplifier and a shunt regulator. The shunt regulator provides the necessary bias stability for the 3.579545 MHz oscillator, as well as the bias to all functions of the CA3070 circuit. The regulation voltage is nominally +12 volts as measured at terminal No. 10.

The APC and ACC detectors are synchronous detectors which are keyed by the horizontal input pulse. This form of detection eliminates the need for a burst separator as an individual amplifier stage. When a positive pulse is present at terminal No. 4, the oscillator output is cutoff and the oscillator drive signal is diverted to the APC and ACC detectors. Referring to Fig. 2, the APC detector (Q_9 & Q_{10}) and the ACC detector (Q_5 & Q_6) are emitter driven from the oscillator transistor (Q_{17}), when the oscillator output amplifier transistors (Q_2 & Q_3) are cutoff. The chroma signal is applied to terminal Nos. 13 and 14. There is oscillator current drive to the APC and ACC detectors during the keying interval; burst separation is effectively accomplished by the gating action of the detectors. A further advantage of the keying action is the high gain made possible as a result of the low average current flow of the APC and ACC detectors. High resistor values of 62 kilohms at the detector output terminals provide proper detector bias consistent with the duty factor of the keying pulse. For a wider keying pulse, it is necessary that smaller values of detector load resistors be used.

In the absence of the keying pulse (line period), the resistor, R_{20}, biases the oscillator's output amplifier transistors (Q_2 & Q_3) on by keeping their emitters at a higher potential than the base bias voltages of Q_5, Q_6, Q_9, and Q_{10}. The 3.58 MHz signal is now present at terminal Nos. 2 & 3. Photographs of oscilloscope traces for one line period at the terminal Nos. 1, 2, and 3 are shown in Fig.16. The effect of the keying pulse is shown in Fig.16a, and the cutoff of the oscillator output amplifier is shown in Fig.16(b) and 16c.

The oscillator section of the CA3070 consists of the loop formed by Q_{18} and the emitter driven differential pair, Q_{13} & Q_{14}. The signal output from terminal Nos. 7 & 8 is coupled through the series tuned crystal circuit back through terminal No. 6 to Q_{16} & Q_{17}. The collector of Q_{17} drives the oscillator output amplifier and the APC & ACC detectors. Q_{17} is emitter coupled to transistor Q_{18}. The oscillator frequency and phase control is accomplished by the differential drive from the APC detector to transistors Q_{12} & Q_{15} which control the balance of Q_{13} & Q_{14}. The resulting phase of the feedback loop is determined by the relative amplitudes of the oscillator output signal at terminal Nos. 7 and 8. The 65 pF capacitor between terminal No. 7 and 8 provides the phase shifting component as the balance of Q_{13} and Q_{14} is varied. In this way the APC detector controls the crystal frequency at which the phase shift is cancelled in the feedback loop.

The controls for the CA3070 subcarrier regenerator circuit are the APC balance, the ACC balance, and the hue control. The hue control is a dc balance adjustment of the oscillator output amplifier transistors Q_2 & Q_3. A phase delay network between the output terminals Nos. 2 & 3 determines the range of the hue control, which for the value shown in Fig. 15, is approximately 90°.

The ACC adjustment sets the initial balance of the ACC drive to the input of the CA3071 in Fig. 15 (terminal Nos. 1 and 14 of the CA3071). The APC is a frequency adjustment of the oscillator through the balance control of the APC detector.

As a setup adjustment, for both the ACC and APC, switch S1 is opened and S2 is closed. The chroma input to the system is removed and the dc voltage at terminal No. 6 of the CA3071 is noted. The switch S2 is then opened and the ACC adjusted to set the voltage at terminal No. 6 to that previously noted. Alternatively, the differential dc voltage at terminal Nos. 15 & 16 of the CA3070 may be set to 0 mV (±2 mV) when S1 and S2 are open, and the CA3071 is removed from the circuit.

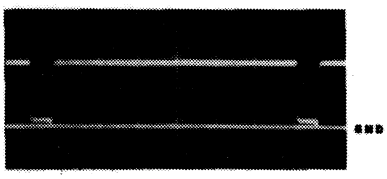


Fig. 16(a) - CA3070 terminal No. 1 7.5 V oscillator "gate off" pulse.

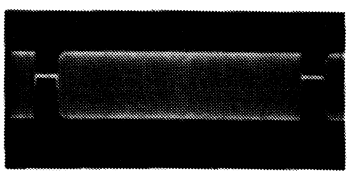


Fig. 16(b) - CA3070 terminal No. 2, 3.5 V_{p-p} oscillator output; one horizontal line, (gated off during burst).

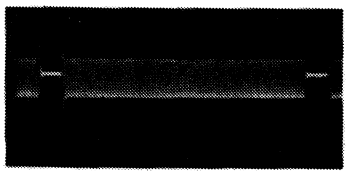


Fig. 16(c) - CA3070 terminal No. 3, 2.0 V_{p-p} oscillator output; one horizontal line, (gated off during burst).

CA3070, CA3071, CA3072

With the chroma signal still removed, the APC adjustment sets the frequency of the oscillator to 3.579545 MHz. Due to the gated off interval, a counter will not accurately record the frequency at the oscillator output amplifier terminals. Two simple and accurate methods are as follows: (1) a buffered crystal filter circuit, connected to the oscillator output amplifier terminals will continue to ring and fill the gated off window providing the proper interface to a counter; (2) the other method involves monitoring the demodulated output at the color difference output terminals of the CA3072. A zero beat signal, at the color difference outputs may be seen on an oscilloscope.

When these adjustments are made, similar oscilloscope traces should be seen as shown in Fig. 17.

CA3071 CIRCUIT OPERATION

The CA3071 is the basic amplifier and control circuit of the chroma system. It contains the gain control functions of the ACC loop, the color killer, and the dc chroma gain control. The CA3071 is a wide band amplifier having two stages of voltage gain. Curves of frequency-response and linearity are shown in Figs. 10 & 11 for the wideband circuits shown in Fig. 9. This is the same basic amplifier as the one in the system shown in Fig. 15 except for the omission of the tuned circuits and the ACC loop connection. The amplifiers have bandwidths of greater than 10 MHz, and are usable well beyond 30 MHz. The signal swing of the wide band amplifier is in excess of 5 V_{p-p}, even with the typical load coupling as shown in Fig. 15. Fig. 18 (a, b and c) show the oscilloscope traces for an NTSC signal at the chroma input. The overall frequency-response curves are shown in Fig. 19.

CA3071 operation is as follows (Refer to Figs. 6 &15). The input chroma signal is applied to terminal No. 2. This signal is amplified in a cascode differential circuit from Q_{10} to Q_{12} and the output is an emitter follower, Q_{14} (Terminal No. 6.) The signal is divided in the Q_9 & Q_{12} differential amplifier, depending on the applied ACC error signal amplitude at terminal Nos. 1 & 14. The ACC error signal is derived from terminal Nos. 15 & 16 of the CA3070 and after filtering, is applied to terminal Nos. 1 & 14 of the CA3071.

At low signal drive, the 390 kilohm resistor at switch S1 (normally closed) unbalances the differential amplifier for high signal gain through Q_{12}. As the burst level at the chroma input increases, the ACC drive changes differentially in a positive direction at terminal No. 14 and a negative direction at terminal No. 14 and a negative direction at terminal No. 1. At strong signal levels the gain is reduced by diverting the balance of ac current in the differential amplifier from Q_{12} to Q_9, which is shunted to ac ground at terminal Nos. 12 and 13. The ACC loop is completed through the chroma signal at terminal No. 6 of the CA3071 to terminal No. 14 (input) of the CA3070. A typical ACC characteristic is shown in Fig. 23.

The chroma signal is buffer connected from terminal No. 6 to terminal No. 7 of the CA3071 and is amplified in the 2nd stage of voltage gain. Both the color killer adjustment and the dc chroma gain control are applied to the 2nd stage to control the chroma output at terminal No. 9. The color killer section of the CA3071 is a Schmitt trigger & amplifier circuit consisting of transistors Q_1, Q_2 and Q_3. Under maximum chroma output conditions, the diode D_2 is reversed biased, and the signal path is through Q_{15}, Q_4 and Q_5 to terminal No. 9. When the color killer circuit is actuated, or the chroma gain control is adjusted to a higher positive voltage at terminal No. 10, the anode voltage of diode D_2 is increased to draw current from the signal path at the emitter of Q_4. This decreases the chroma gain as the potential at terminal No. 10 is increased. When the potential at terminal No. 10 is the same as terminal No. 8, the chroma output at terminal 9 is cutoff.

The color killer circuit provides an abrupt voltage swing at the anode of D_2 to cutoff the chroma output when the Schmitt trigger circuit is forward biased at terminal No. 13. In the circuit of Fig. 18, the color killer adjustment is a resistance divider circuit which establishes the threshold of burst level at which the killer operates the chroma amplifier.

CA3072 CIRCUIT OPERATION

The CA3072 is a chroma demodulator having full color difference signal demodulation capability. The chroma signal is applied to terminal Nos. 3 & 4 and the reference subcarrier signal is applied to terminals Nos. 6 & 7 of the CA3072. The output color difference signals are B-Y at terminal No. 13, R-Y at terminal No. 11, and G-Y at terminal No. 9. The typical level of differential chroma drive required at terminal Nos. 3 & 4 is 400 mV_{p-p}. The amplitude of chroma at terminal No. 6 & 7 is approximately 1.0 volt at 104° relative phase difference which results in a B-Y output amplitude of $5V_{p-p}$. The voltages of the R-Y & G-Y outputs are at 3.8 and 1.0 V_{p-p} respectively, when there is $5V_{p-p}$ output at B-Y. These comparative signals are based upon a complete phase rotation of the chroma relative to the subcarrier signal reference. The relative demodulation phase and amplitude ratios of the Fig. 15 circuit are shown in the oscilloscope trace photographs of Fig. 21. Using the hue control setting for B-Y phase at the B-Y output, the G-Y color-difference signal is approximately −104° and the R-Y color-difference signal is approximately +106°. Since the amplitude ratios are a function of the applied signal phase relationship, the NTSC color difference output signals are shown here primarily for phase reference conditions.

CHROMA SYSTEM CONSTRUCTION

Fig. 25 shows the complete CA3070, CA3071 and CA3072 chroma system in the Fig. 18 circuit. Table I lists the dc terminal voltages for the system. The chroma gain and hue controls, as well as the switches S1 and S2 are removed. The template circuit board layout is also shown for duplication purposes. It should be noted that a few component values are modified in Fig. 18 from the dynamic circuit values of the data sheet. These are necessary for system matching and overall filter requirements.

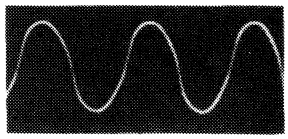


Fig. 17(a) - CA3070 terminal No. 6, oscillator waveform 1.1 V_{p-p} 3.58 MHz.

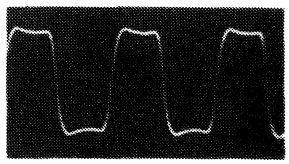


Fig. 17(b) - CA3070 terminal No. 7, oscillator waveform 1.4 V_{p-p} 3.58 MHz.

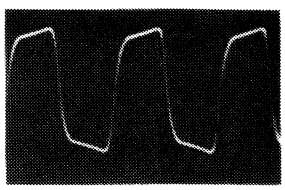


Fig. 17(c) - CA3070 terminal No. 8, oscillator waveform 1.6 V_{p-p} 3.58 MHz.

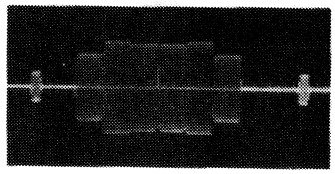


Fig. 18(a) - CA3071 chroma input 1.25 V_{p-p}; one horizontal line of NTSC input signal.

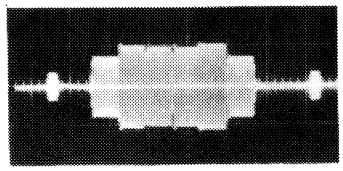


Fig. 18(b) - CA3071 terminal No. 6, amplifier No. 1 chroma output 2.3 V_{p-p}; one horizontal line for 1.25 V_{p-p} chroma input

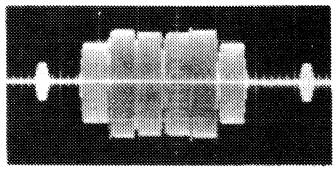


Fig. 18(c) - CA3071 terminal No. 9, amplifier No. 2 chroma output 5.5 V_{p-p}; one horizontal line for 1.25V_{p-p} chroma input

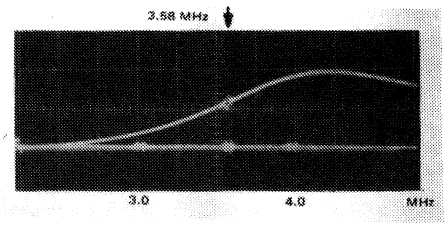


Fig. 19(a) - Frequency response sweep curve between terminal Nos. 2 & 6 for CA3071. f = 250 KHz/div.

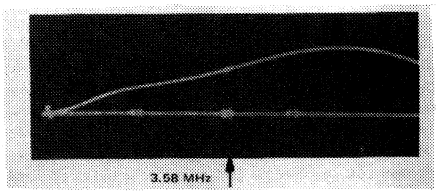


Fig. 19(b) - Frequency response sweep curve between terminal No. 2 of CA3071 and terminal No. 3 of CA3072. f = 250 KHz/div.

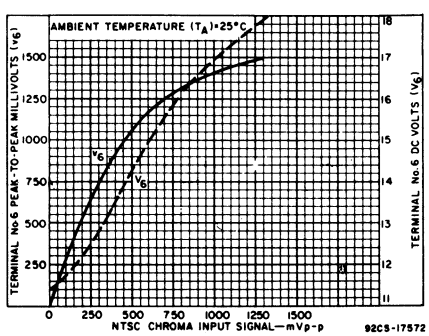


Fig. 20 - Typical ACC characteristics for chroma system of Fig. 18

CA3070, CA3071, CA3072

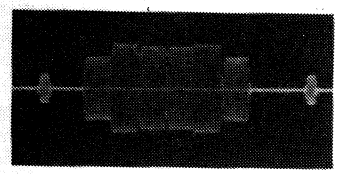


Fig. 21(a) - CA3072 - terminal No. 3 or 4, chroma input signal, 220 mV_{p-p}, one horizontal line

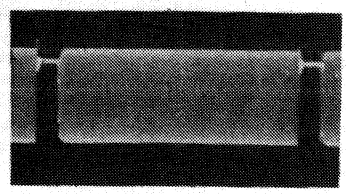


Fig. 21(b) - CA3072 - terminal No. 6 or 7, reference subcarrier 1.2 V_{p-p}, one horizontal line

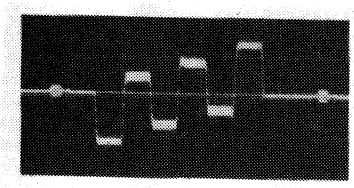


Fig. 21(c) - CA3072 terminal No. 13, 4.8 v_{p-p} B-Y output, one horizontal line

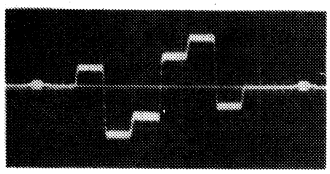


Fig. 21(d) - CA3072 - terminal No. 11, 5.2 v_{p-p} R-Y output, one horizontal line

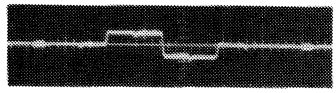


Fig. 21(e) - CA3072 - terminal No. 9, 1.2 v_{p-p} G-Y output, one horizontal line

CA3075

FM IF Amplifier - Limiter, Detector, and Audio Preamplifier

For FM IF Amplifier Applications Up To 20 MHz In Communications Receivers And High-Fidelity Receivers

Features:

- Good sensitivity: Input limiting voltage (knee) = 250 μV typ. at 10.7 MHz
- Excellent AM rejection: 55 dB typ. at 10.7 MHz
- Internal Zener diode regulation for the IF amplifier section
- Low harmonic distortion
- Differential peak detection: Permits simplified single-coil tuning
- Audio preamplifier voltage gain: 21 dB typ.
- Minimum number of external parts required

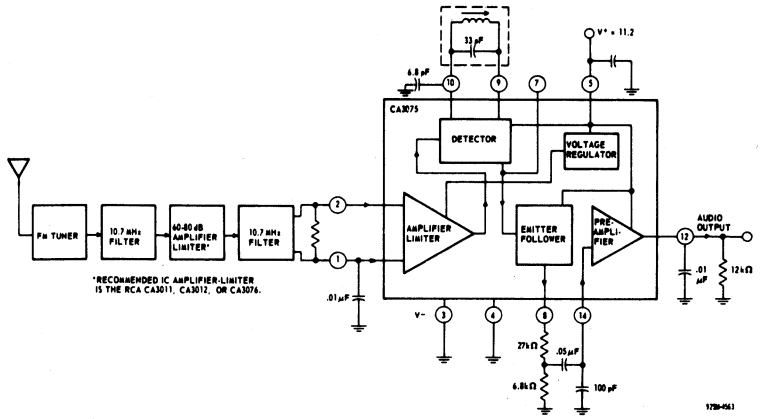


Fig. 1 - Block diagram of typical FM receiver utilizing the CA3075

RCA CA3075 is an integrated circuit which provides, in a single monolithic chip, an FM IF subsystem for Communications and High-Fidelity Receivers This device, shown in the schematic diagram (Fig. 2), consists of a multistage IF amplifier-limiter section with a Zener regulated power supply, an FM detector stage, and an AF preamplifier section. A typical application of the CA3075, in FM receiver circuits, is shown in the block diagram (Fig. 1).

The three-stage, emitter-follower-coupled IF amplifier section provides a 60-dB typ. voltage gain at an operating frequency of 10.7 MHz and features, because of its transistor constant-current sink, an output stage with exceptionally good limiting characteristics.

The FM detector section, which utilizes a differential-peak-detection circuit, requires only a single coil in the associated outboard detector circuit; hence, tuning the detector circuit is a simple procedure.

The audio preamplifier circuit provides a 21-dB voltage gain with low impedance output for driving subsequent audio amplifier stages.

The CA3075 utilizes a 14-lead dual-in-line plastic package with leads in a special quad-formed arrangement.

MAXIMUM RATINGS, *Absolute-Maximum Values at* T_A = 25°C

DC Supply Voltage [between Terminals 5 (V^+) and 3 (V^-)]	12.5	V
DC Current (into Terminal 5)	30	mA
Device Dissipation:		
Up to T_A = 50°C	760	mW
Above T_A = 50°C	derate linearly 7.6	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During soldering for 10 s max.)	+265	°C

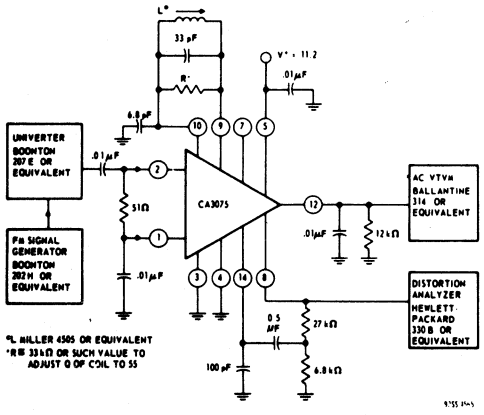


Fig. 2 - Test Circuit for input limiting voltage, recovered AF voltage, and total harmonic distortion

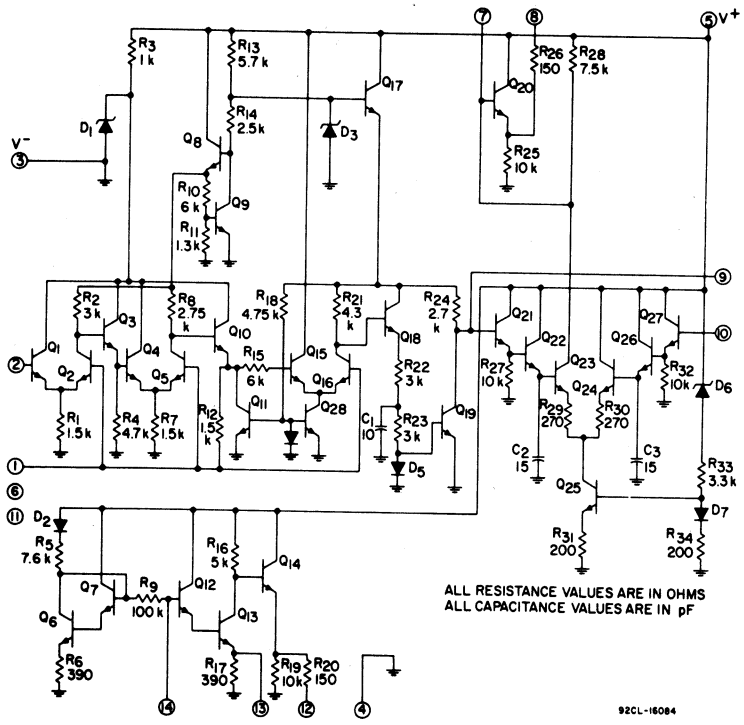


Fig.3 – Schematic diagram of CA3075

CA3075

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CIRCUIT FIG. NO.
Static Characteristics							
DC Voltage:							
At Terminal 7	V_7	V^+ = 11.2 V	–	6.1	–	V	6
At Terminal 8	V_8		–	5.4	–	V	
At Terminal 12	V_{12}		–	5.2	–	V	
DC Current (into Terminal 5):							
At V^+ = 8.5 V	I_5		8.5	15	–	mA	6
At V^+ = 11.2 V			–	17.5	–	mA	
At V^+ = 12.5 V			–	19	29	mA	
Dynamic Characteristics at V^+ = 11.2							
IF AMPLIFIER							
Input Limiting Voltage (knee, – 3dB point)	V_I(lim)	f_0 = 10.7 MHz, f(Modulation) = 400 Hz, Deviation = ±75 kHz	–	250	600	μV	3
AM Rejection	AMR	f_0 = 10.7 MHz, f(Modulation) = 400 Hz, FM: Deviation = ±75 kHz, AM: Modulation = 30%	–	55	–	dB	5
Input Impedance Components:							
Parallel Resistance	R_I	f_0 = 10.7 MHz	–	4.5	–	kΩ	–
Parallel Capacitance	C_I	V_{IN} = 10 mV RMS	–	4.5	–	pF	
DETECTOR							
Recovered AF Voltage (at Terminal 12)	V_O(AF)	f_0 = 10.7 MHz, f(Modulation) = 400 Hz, Deviation = ± 75 kHz	–	1.5	–	V	3
Total Harmonic Distortion	THD		–	1	2	%	
AUDIO PREAMPLIFIER							
Voltage Gain	A(AF)	V_{IN} = 100 mV, f_0 = 400 Hz	–	21	–	dB	4
Total Harmonic Distortion	THD	V_{OUT} = 2 V, f_0 = 400 Hz	–	1.5	5	%	4

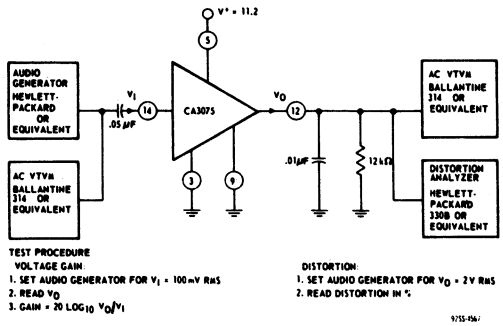


Fig.4 – Test circuit for audio preamplifier voltage gain and total harmonic distortion

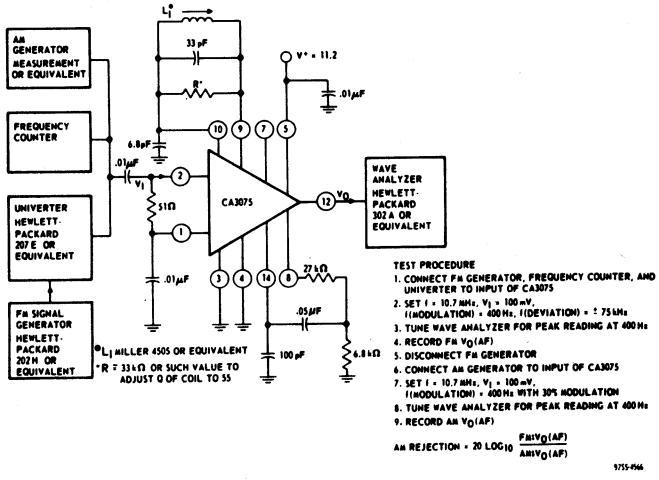


Fig.5 – Test circuit for AM rejection

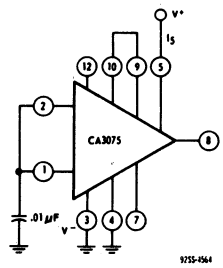


Fig. 6-Test circuit for static characteristics

CA3076
High-Gain Wide-Band IF Amplifier-Limiter

For FM IF Amplifier Applications in Communications Receivers

RCA CA3076, monolithic integrated circuit, is a high-gain wide-band amplifier-limiter for use in the IF sections of Communications and High-Fidelity FM Receivers. The CA3076, shown in the schematic diagram (Fig. 2), consists of a four stage IF amplifier-limiter section with a voltage regulator section. A typical application of the CA3076 in FM receiver circuits is shown in the block diagram (Fig. 1).

The four-stage emitter-follower-coupled IF amplifier section provides an 80-dB voltage gain with a 2-kilohm load at a frequency of 10.7 MHz. The output stage has exceptionally good limiting characteristics because of its transistor constant-current sink. The voltage regulator section provides zener-regulated, decoupled voltages for the IF amplifier.

The CA3076 utilizes an hermetically-sealed 8-lead TO-5 package.

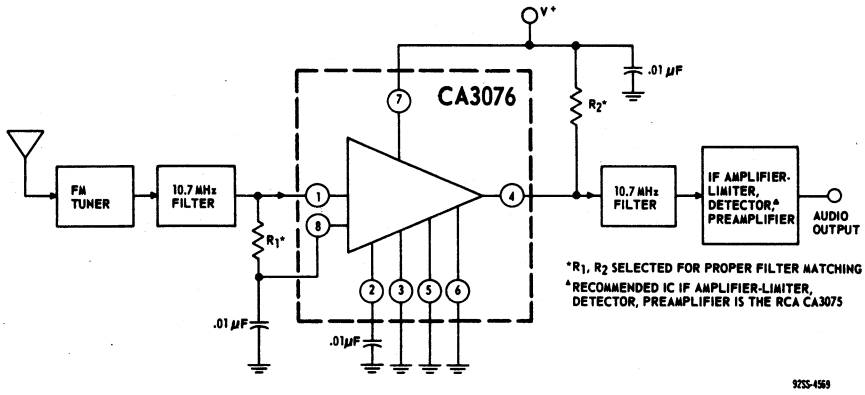


Fig. 1 - Block diagram of typical FM receiver utilizing the CA3076.

Features:

- exceptionally good sensitivity: input limiting voltage (knee) = 50 μV typ. at 10.7 MHz
- high gain: 80 dB with 2-kilohm load
- internal voltage supply regulator
- wide frequency capability: > 20 MHz

MAXIMUM RATINGS, *Absolute Maximum-Values at* T_A = 25°C

DC Supply Voltage [between Terminals 7 (V^+) and 3 (V^-)]	15	V
DC Current (into Terminal 7)	35	mA
Device Dissipation:		
Up to T_A = 50°C	500	mW
Above T_A = 50°C	derate linearly 5 mW/°C	
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/32 in (3.17 mm) from seating plane for 10 s max	+265	°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
***Static Characteristics* – V^+ = 8.5 V**						
DC Current (into Term. 7)	I_7	–	10	15	24	mA
Quiescent Operating Current (into Term. 4)	I_4	–	–	0.65	–	mA
***Dynamic Characteristics* – V^+ = 8.5 V, f_O = 10.7 MHz**						
Input Limiting Voltage (knee, −3 dB point)	V_I (lim.)	–	–	50	200	μV
Output Voltage	V_O	V_I = 20 μV	4	12	–	mV
Output Noise Voltage	V_N	V_I = 0	–	1	–	mV
Forward Transfer Admittance:						
Magnitude	$\lvert Y_{21} \rvert$	V_I =	–	6	–	mho
Phase	θ_{21}	10 μV	–	80	–	degrees
Reverse Transfer Admittance:						
Magnitude	$\lvert Y_{12} \rvert$	–	–	0.1	–	μmho
Phase	θ_{12}		–	−90	–	degrees
Input-Impedance Components:						
Parallel Resistance	R_I	–	–	7.5	–	kΩ
Parallel Capacitance	C_I		–	4	–	pF
Output-Impedance Components:						
Parallel Resistance	R_O	–	50	–	–	kΩ
Parallel Capacitance	C_O		–	1.7	–	pF

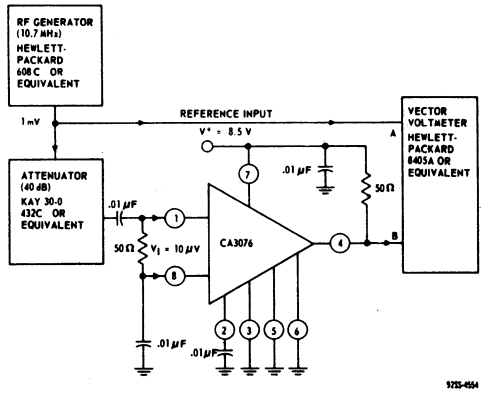


Fig. 2 - Forward transfer admittance (Y_{21}) test circuit

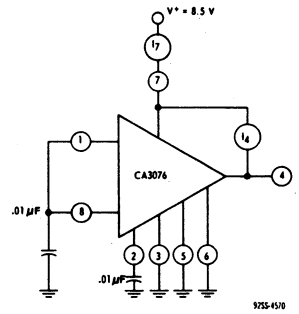
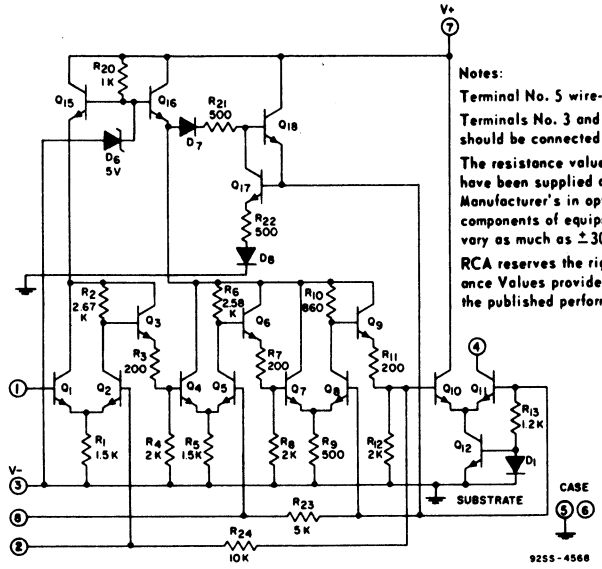


Fig. 3 - Test circuit for DC current (Terminal 7) and operating current (Terminal 4).

CA3076



Notes:

Terminal No. 5 wire-connected to the case.

Terminals No. 3 and 6 which are connected to the substrate should be connected to the most negative point in the circuit.

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturer's in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ±30%.

RCA reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

Fig. 4 - Schematic diagram of CA3076.

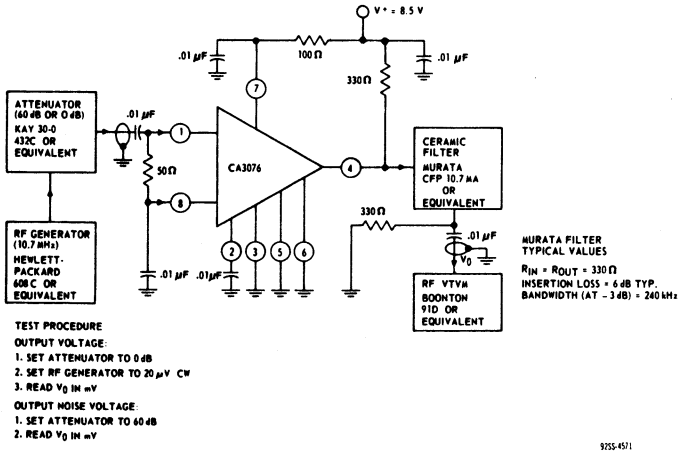


Fig. 5 - 10.7 MHz voltage gain and noise test circuit

CA3078, CA3078A Types

Amplifier

The RCA CA3078T and CA3078AT are high-gain monolithic operational amplifiers which can deliver milliamperes of current yet only consume microwatts of standby power. Their operating points are externally adjustable and frequency compensation may be accomplished with one external capacitor. The CA3078T and CA3078AT provide the designer with the opportunity to tailor the frequency response and improve the slew rate without sacrificing power. Operation with a single 1.5-volt battery is a practical reality with these devices.

The CA3078AT is a premium device having a supply voltage range of $V^{\pm}$ = 0.75V to $V^{\pm}$ = 15V and an operating temperature range of -55°C to +125°C. The CA3078T has the same lower supply voltage limit but the upper limit is V^+ = +6V and V^- = -6V. The operating temperature range is from 0°C to +70°C.

The CA3078 and CA3078A are supplied in either the standard 8-lead TO-5 package ("T" suffix), or in the 8-lead dual-in-line formed-lead "DIL-CAN" package ("S" suffix).

Features:

- Low standby power: as low as 700 nW
- Wide supply voltage range: ±0.75 to ±15 V
- High peak output current: 6.5 mA min.
- Adjustable quiescent current
- Output short-circuit protection

Applications:

- Portable electronics
- Medical electronics
- Instrumentation
- Telemetry

MAXIMUM RATINGS, *Absolute Maximum Values at T_A = 25°C*

	CA3078AT	CA3078T
DC Supply Voltage (between V^+ and V^- terminal	36V	14V
Differential Input Voltage	±8V	±6V
DC Input Voltage	V^+ to V^-	V^+ to V^-
Input Signal Current	0.1 mA	0.1 mA
Output Short-Circuit Duration*	No Limitation	No Limitation
Device Dissipation	50 mW (up to 125°C)	500 mW (up to 70°C)
Temperature Range:		
Operating	-55 to +125°C	0 to +70°C ▲
Storage	-65 to +150°C	-65 to +150°C
Lead Temperature (During Soldering):		
At distance 1/16 ±1/32 in. (1.59 ±0.79 mm) from case for 10s max.	+300°C	+300°C

*Short circuit may be applied to ground or to either supply.

▲ Types CA3078S and T can be operated over the temperature range of -55 to +125° C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to 70° C.

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS			CA3078T LIMITS R_{SET} = 1 MΩ, I_Q = 100 μA					CA3078AT LIMITS R_{SET} = 5.1 MΩ, I_Q = 20 μA					UNITS
		V^+ & V^-	R_S KΩ	R_L KΩ	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	T_A = 0 to 70°C MIN	T_A = 0 to 70°C MAX	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	T_A = -55 to 125°C MIN	T_A = -55 to 125°C MAX	
Input Offset Voltage	V_{IO}	6	≤10		–	1.3	4.5	–	5	–	0.70	3.5	–	4.5	mV
Input Offset Current	I_{IO}				–	6	32	–	40	–	0.50	2.5	–	5.0	nA
Input Bias Current	I_{IB}				–	60	170	–	200	–	7	12	–	50	nA
Open-Loop Diff. Voltage Gain	A_{OL}			≥10	88	92	–	86	–	92	100	–	90	–	dB
Total Quiescent Current	I_Q				–	100	130	–	150	–	20	25	–	45	μA
Device Dissipation	P_D				–	1200	1560	–	1800	–	240	300	–	540	μW
Maximum Output Voltage	V_{OM}			≥10	±5.1	±5.3	–	±5	–	±5.1	±5.3	–	±5	–	V
Common-Mode Input Voltage Range	V_{ICR}		≤10		–	-5.5 to +5.8		-5 to +5	–	–	-5,5 to +5.8	–	-5 to +5	–	V
Common-Mode Rejection Ratio	CMRR		≤10		80	110		–	–	80	115	–	–	–	dB
Maximum Output Current	I_{OM}^+ or I_{OM}^-				–	12	–	6.5	30	–	12	–	6.5	30	mA
Input Offset Voltage Sensitivity Positive	$\Delta V_{IO}/\Delta V^+$		≤10			22	150	–	–		6	150	–	–	μV/V
Negative	$\Delta V_{IO}/\Delta V^-$					22	150	–	–		6	150	–	–	
										R_{SET} = 13 MΩ, I_Q = 20 μA					
Input Offset Voltage	V_{IO}	15	≤10							–	1.4	3.5	–	4.5	mV
Open-Loop Diff. Voltage Gain	A_{OL}		–	≥10			–	–	–	92	100	–	88	–	dB
Total Quiescent Current	I_Q						–	–	–	–	20	30	–	50	μA
Device Dissipation	P_D						–	–	–	–	600	750	–	1350	μW
Maximum Output Voltage	V_{OM}			≥10			–	–	–	±13.7	±14.1		±13.5	–	V
Common-Mode Rejection Ratio	CMRR		≤10				–	–	–	80	106	–	–	–	dB
Input Bias Current	I_{IB}						–	–	–	–	7	14	–	55	nA
Input Offset Current	I_{IO}						–	–	–	–	0.50	2.7	–	5.5	nA

OPERATING CONSIDERATIONS

Compensation Techniques

The CA3078AT and CA3078T can be phase-compensated with one or two external components depending upon the closed-loop gain, power consumption, and speed desired. The recommended compensation is a resistor in series with a capacitor connected from terminal 1 to terminal 8. Values of the resistor and capacitor required for compensation as a function of closed loop gain are shown in Figs. 24 and 25. These curves represent the compensation necessary at quiescent currents of 20 μA and 100 μA, respectively, for a transient response with 10% overshoot. Figs. 21 and 22 show the slew rates that can be obtained with the two different compensation techniques. Higher speeds can be achieved with input compensation, but this increases noise output.

Compensation can also be accomplished with a single capacitor connected from terminal 1 to terminal 8, with speed being sacrificed for simplicity. Table 1 gives an indication of slew rates that can be obtained with various compensation techniques at quiescent currents of 20 μA and 100 μA.

Single Supply Operation

The CA3078AT and CA3078T can operate from a single supply with a minimum total supply voltage of 1.5 volts. Figs. 27 and 28 show the CA3078AT or CA3078T in inverting and non-inverting 20-dB amplifier configurations utilizing a 1.5-volt type "AA" cell for a supply. The total power consumption for either circuit is approximately 675 nanowatts. The output voltage swing in this configuration is 300 mV p-p with a 20 kΩ load.

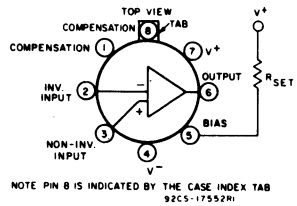


Fig.1 – Functional diagram of the CA3078T and CA3078AT.

CA3078, CA3078A Types

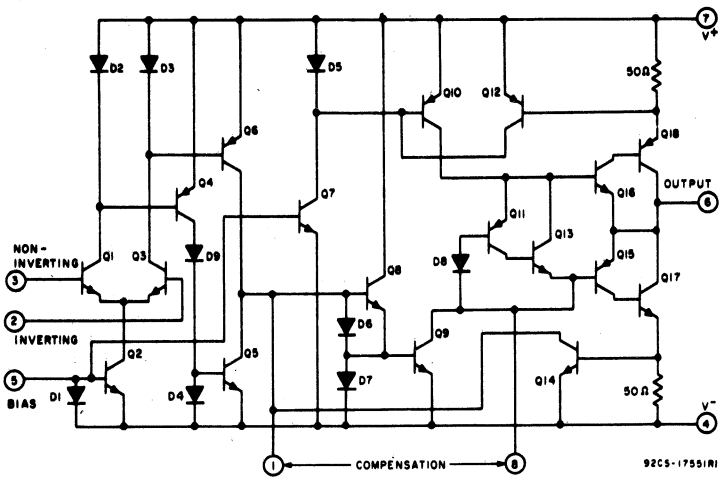


Fig.2-Schematic diagram of the CA3078T and CA3078AT.

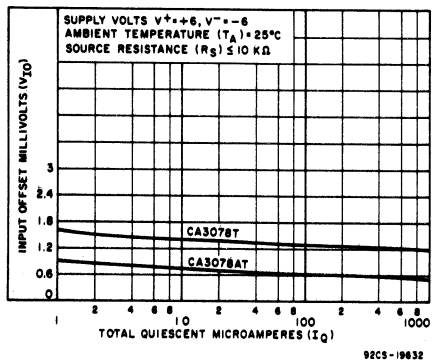


Fig.3 – Input offset voltage vs. total quiescent current.

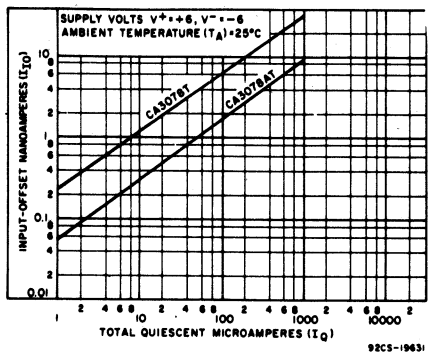


Fig.4 – Input offset current vs. total quiescent current.

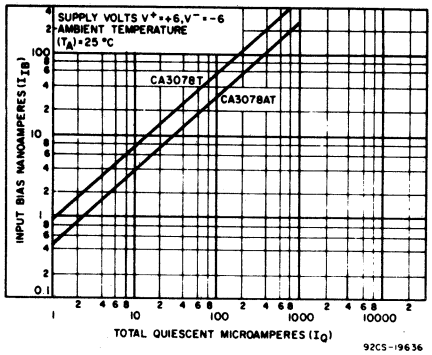


Fig.5 – Input bias current vs. total quiescent current.

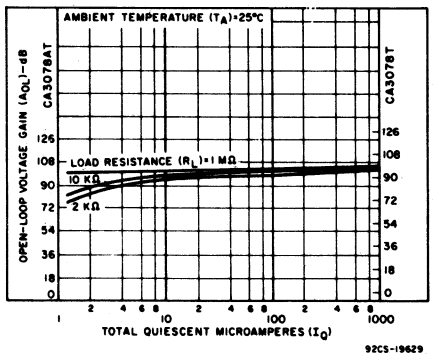


Fig.6 – Open-loop voltage gain vs. total quiescent current.

Typical Values Intended Only for Design Guidance at T_A = 25°C and V^+ = +6 V, V^- = 6 V

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	CA3078AT		CA3078T	UNITS
			R_{SET} = 5.1 MΩ, I_Q = 20 μA	R_{SET} = 1 MΩ, I_Q = 100 μA	R_{SET} = 1 MΩ, I_Q = 100 μA	
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T_A$	$R_S \leq 10$ KΩ	5	6	6	μV/°C
Input Offset Current Drift	$\Delta V_{IO}/\Delta T_A$	$R_S \leq 10$ KΩ	6.3	70	70	pA/°C
Open-Loop Bandwidth	BW_{OL}	3dB pt	0.3	2	2	kHz
Slew Rate:						
Unity Gain	SR	See Figs.	0.027	0.04	0.04	V/μs
Comparator		20, 21	0.5	1.5	1.5	
Transient Response		10% to 90% Rise Time	3	2.5	2.5	μs
Input Resistance	R_I		7.4	1.7	0.87	MΩ
Output Resistance	R_O		1	0.8	0.8	KΩ
Equiv. Input Noise Voltage	e_N(10Hz)	R_S = 0	40	–	25	nV/√Hz
Equiv. Input Noise Current	i_N(10Hz)	R_S = 1 MΩ	0.25	–	1	pA/√Hz

ELECTRICAL CHARACTERISTICS, at T_A = 25°C
Typical Values Intended Only for Design Guidance

CHARACTERISTICS SYMBOLS	TYPICAL VALUES				UNITS
	CA3078AT		CA3078T		
	V^+ = +1.3V, V^- = −1.3V, R_{SET} = 2 MΩ, I_Q = 10 μA	V^+ = +0.75V, V^- = −0.75V, R_{SET} = 10 MΩ, I_Q = 1 μA	V^+ = +1.3V, V^- = −1.3V, R_{SET} = 2 MΩ, I_Q = 10 μA	V^+ = 0.75V, V^- = −0.75V, R_{SET} = 10 MΩ, I_Q = 1 μA	
V_{IO}	0.7	0.9	1.3	1.5	mV
I_{IO}	0.3	0.054	1.7	0.5	nA
I_{IB}	3.7	0.45	9	1.3	nA
A_{OL}	84	65	80	60	dB
I_Q	10	1	10	1	μA
P_D	26	1.5	26	1.5	μW
V_{OPP}	1.4	0.3	1.4	0.3	V
V_{ICR}	−0.8 to +1.1	−0.2 to +0.5	−0.8 to +1.1	−0.2 to +0.5	V
CMRR	100	90	100	90	dB
$I_{OM}^{\pm}$	12	0.5	12	0.5	mA
$\Delta V_{IO}/\Delta V^{\pm}$	20	50	20	50	μV/V

CA3078, CA3078A Types

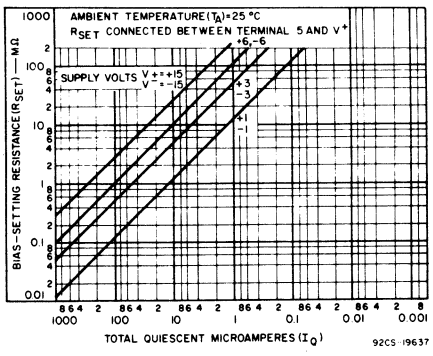


Fig.7 – Bias-setting resistance vs. total quiescent current.

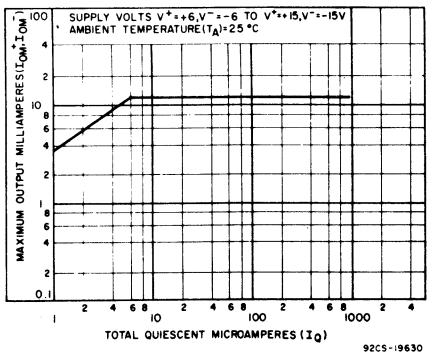


Fig.8 – Maximum output current vs. total quiescent current.

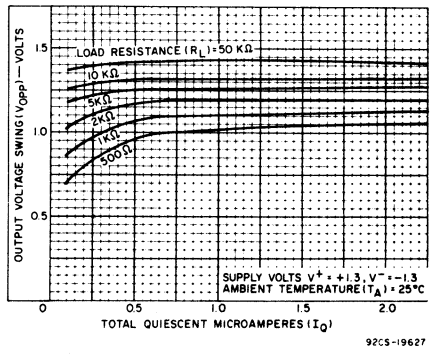


Fig.9 – Output voltage swing vs. total quiescent current.

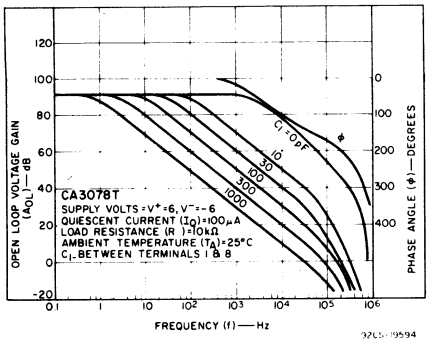


Fig.10 – Open-loop voltage gain vs. frequency for I_Q = 100 μA – CA3078T.

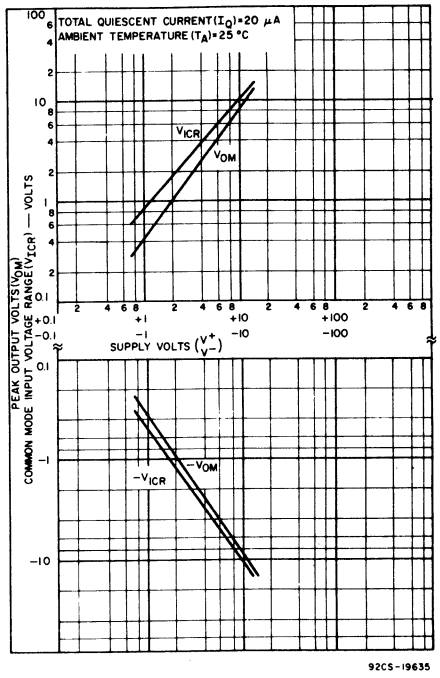


Fig.11 – Output and common-mode voltage vs. supply voltage.

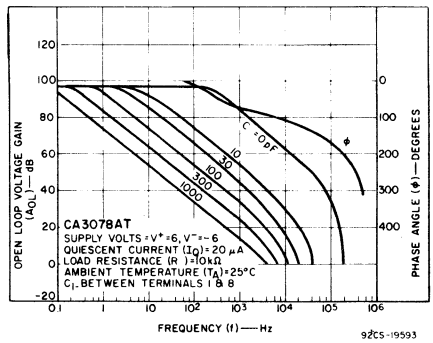


Fig.12 – Open-loop voltage gain vs. frequency for I_Q = 20 μA – CA3078AT.

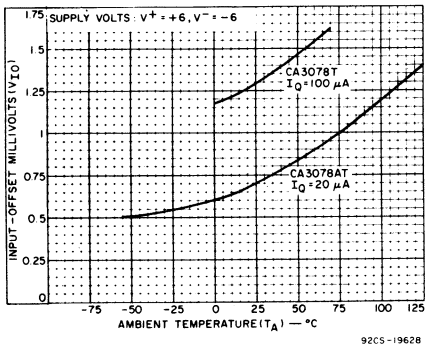


Fig.13 – Input offset voltage vs. temperature.

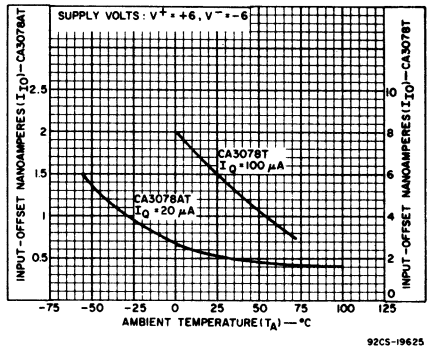


Fig.14 – Input offset current vs. temperature.

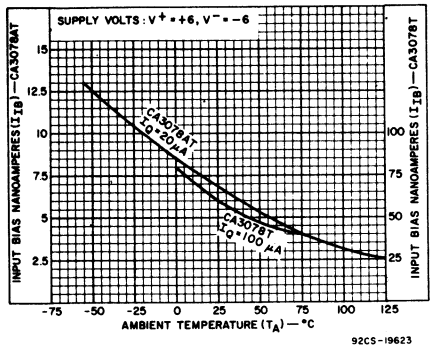


Fig.15 – Input bias current vs. temperature.

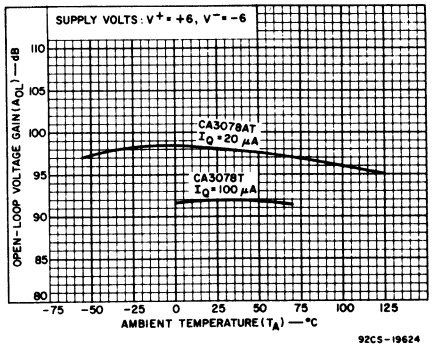


Fig.16 – Open-loop voltage gain vs. temperature.

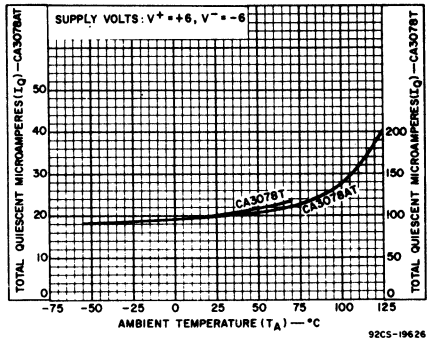


Fig.17 – Total quiescent current vs. temperature.

CA3078, CA3078A Types

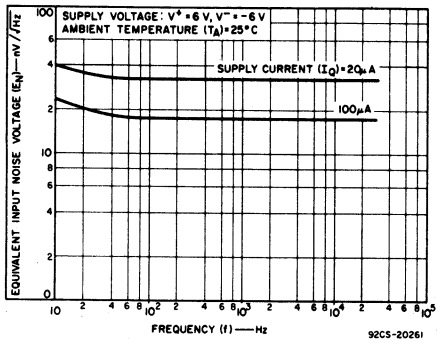


Fig.18 – Equivalent input noise voltage vs. frequency.

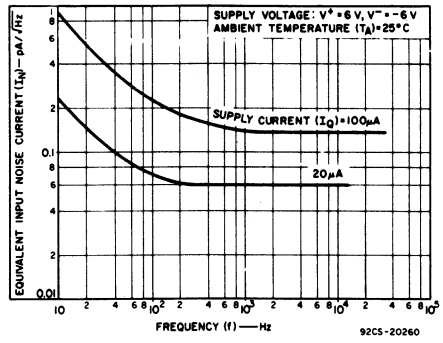


Fig.19 – Equivalent input noise current vs. frequency.

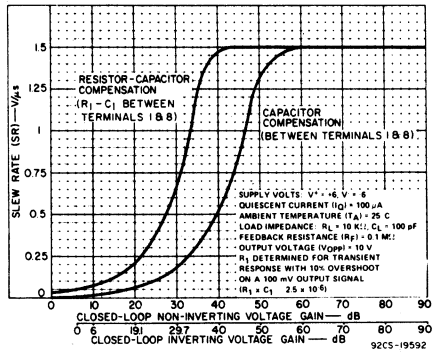


Fig.20 – Slew rate vs. closed-loop gain for I_Q = 100 μA – CA3078T.

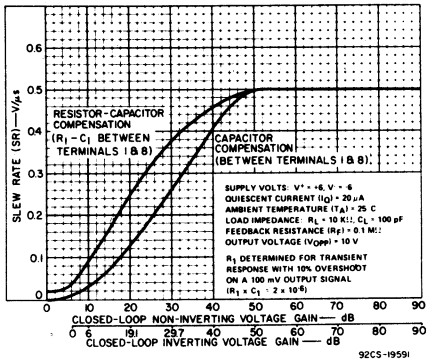


Fig.21 – Slew rate vs. closed-loop gain for I_Q = 20 μA – CA3078AT.

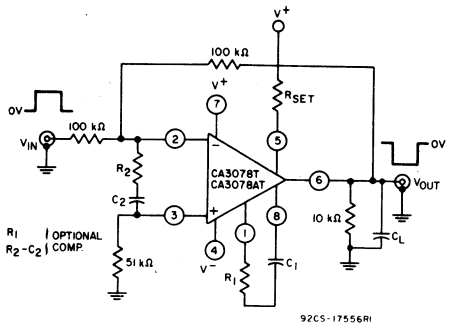


Fig.22 – Transient response and slew-rate, unity gain (inverting) test circuit.

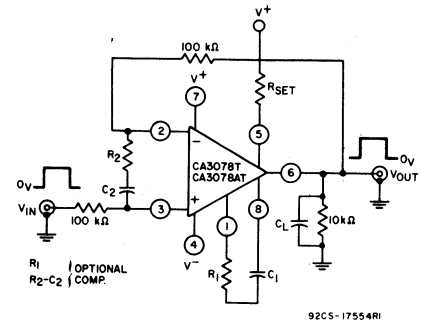


Fig.23 – Slew, rate, unity gain (non-inverting) test circuit.

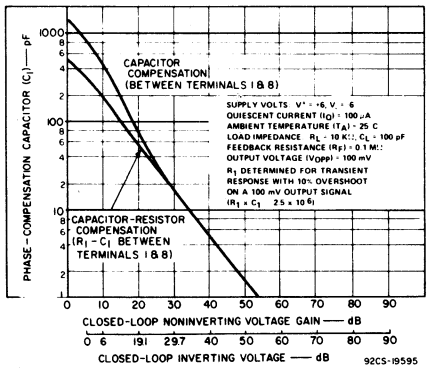


Fig.24 – Phase compensation capacitance vs. closed-loop gain – CA3078T.

Table I - Unity-gain slew rate vs. compensation – CA3078T and CA3078AT

SUPPLY VOLTS: V^+ = 6, V^- = -6 OUTPUT VOLTAGE (V_O) = ±5V LOAD RESISTANCE (R_L) = 10 kΩ						TRANSIENT RESPONSE: 10% OVERSHOOT FOR AN OUTPUT VOLTAGE of 100 mV AMBIENT TEMPERATURE (T_A) = 25°C				
COMPENSATION TECHNIQUE	UNITY GAIN (INVERTING) Fig. 22					UNITY GAIN (NON-INVERTING) Fig. 23				
	R1	C1	R2	C2	SLEW RATE	R1	C1	R2	C2	SLEW RATE
CA3078T – I_Q = 100 μA	kΩ	pF	kΩ	μF	V/μs	kΩ	pF	kΩ	μF	V/μs
Single Capacitor	0	750	∞	0	0.0085	0	1500	∞	0	0.0095
Resistor & Capacitor	3.5	350	∞	0	0.04	5.3	500	∞	0	0.024
Input	∞	0	0.25	0.306	0.67	∞	0	0.311	0.45	0.67
CA3078AT – I_Q = 20 μA										
Single Capacitor	0	300	∞	0	0.0095	0	800	∞	0	0.003
Resistor & Capacitor	14	100	∞	0	0.027	34	125	∞	0	0.02
Input	∞	0	0.644	0.156	0.29	∞	0	0.77	0.4	0.4

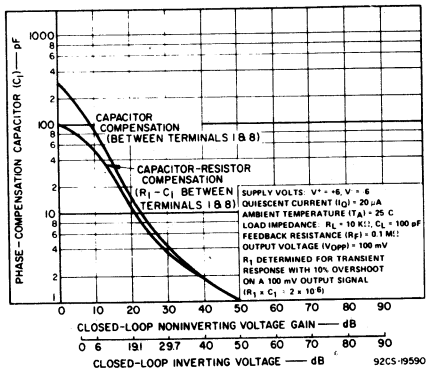


Fig.25 – Phase compensation capacitance vs. closed-loop gain – CA3078AT.

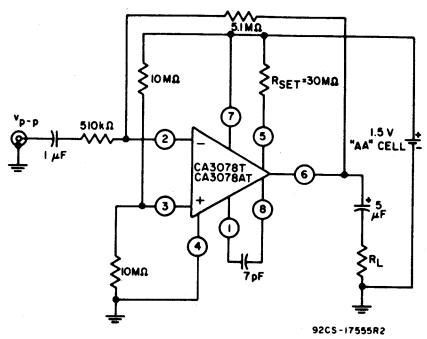


Fig.27 – Inverting 20-dB amplifier circuit.

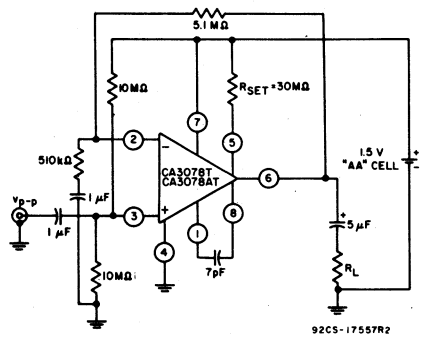


Fig.28 – Non-inverting 20-dB amplifier circuit.