CA3080, CA3080A Types

Operational Transconductance Amplifiers (OTA's)

Gateable-Gain Blocks

The RCA-CA3080 and CA3080A are Gateable-Gain Blocks which utilize the unique Operational Transconductance Amplifier (OTA) concept described in Application Note ICAN-6668, "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers".

The CA3080 and CA3080A have differential input and a single-ended, push-pull, class A output. In addition, these types have an amplifier bias input which may be used either for gating or for linear gain control. These types also have a high output impedance and their transconductance (g_m) is directly proportional to the amplifier bias current (I_{ABC}).

The CA3080 and CA3080A are notable for their excellent slew rate (50 V/μs), which makes them especially useful for multiplex and fast unity-gain voltage followers. These types are especially applicable for multiplex applications because power is consumed only when the devices are in the "ON" channel state.

The CA3080A is rated for operation over the full military-temperature range (−55 to +125°C) and its characteristics are specifically controlled for applications such as sample-hold, gain-control, multiplex, etc. Operational transconductance amplifiers are also useful in programmable power-switch applications, e.g., as described in Application Note ICAN-6048, "Some Applications of a Programmable Power Switch/Amplifier" (CA3094, CA3094A, CA3094B).

These types are supplied in the 8-lead TO-5 style package (CA3080, CA3080A), and in the 8-lead TO-5 style package with dual-in-line formed leads ("DIL-CAN", CA3080S, CA3080AS). The CA3080E is also supplied in the 8-lead dual-in-line plastic ("MINI-DIP") package (CA3080E), and in chip form (CA3080H).

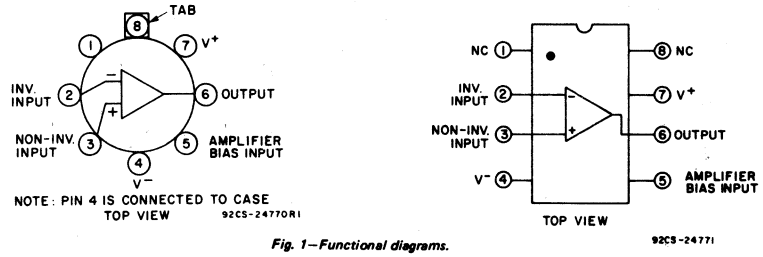


Fig. 1—Functional diagrams.

Plastic Package (CA3080E)

Features:

- Slew rate (unity gain, compensated): 50 V/μs
- Adjustable power consumption: 10μW to 30 mW
- Flexible supply voltage range: ± 2 V to ± 15 V
- Fully adjustable gain: 0 to $g_m R_L$ limit
- Tight g_m spread: CA3080 (2:1), CA3080A (1.6:1)
- Extended g_m linearity: 3 decades

Applications:

- Sample and hold
- Multiplex
- Voltage follower
- Multiplier
- Comparator

MAXIMUM RATINGS, *Absolute-Maximum Values at* $T_A = 25°C$

DC SUPPLY VOLTAGE (between V^+ and V^- terminals)	36 V
DIFFERENTIAL INPUT VOLTAGE	±5 V
DC INPUT VOLTAGE	V^+ to V^-
INPUT SIGNAL CURRENT	1 mA
AMPLIFIER BIAS CURRENT	2 mA
OUTPUT SHORT-CIRCUIT DURATION*	Indefinite
DEVICE DISSIPATION	125 mW
TEMPERATURE RANGE:	
Operating	
CA3080	0 to + 70 °C
CA3080A	−55 to + 125 °C
Storage	−65 to + 150 °C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265 °C

* Short circuit may be applied to ground or to either supply.

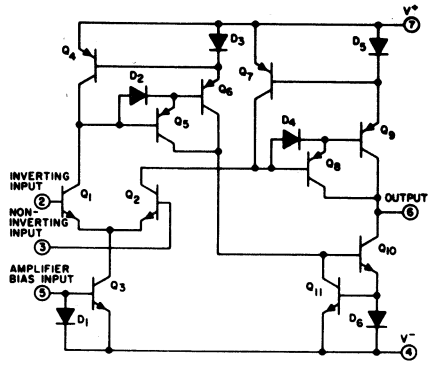


Fig.2 – Schematic diagram for CA3080 and CA3080A.

▲ Type CA3080 can be operated over the temperature of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to 70°C.

TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS FOR THE CA3080 AND CA3080A

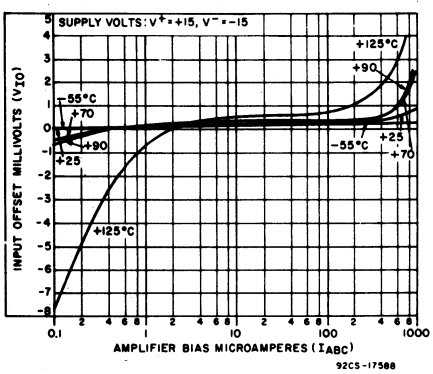


Fig.3 – Input offset voltage vs. amplifier bias current.

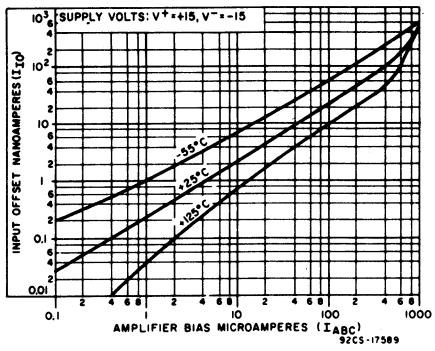


Fig.4 – Input offset current vs. amplifier bias current.

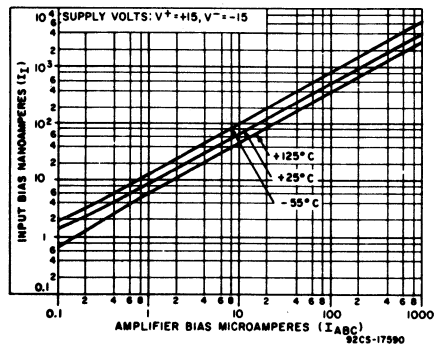


Fig.5 – Input bias current vs. amplifier bias current.

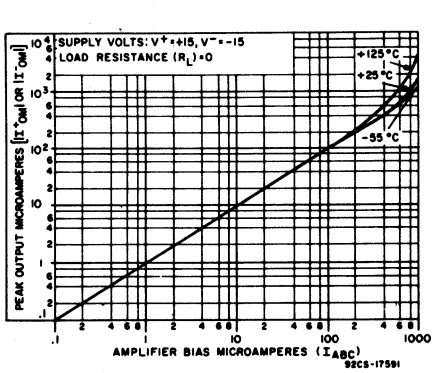


Fig.6 – Peak output current vs. amplifier bias current.

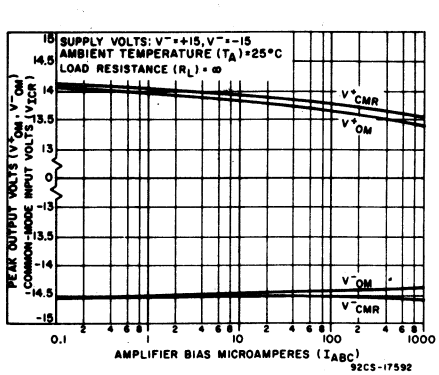


Fig.7 – Peak output voltage vs. amplifier bias current.

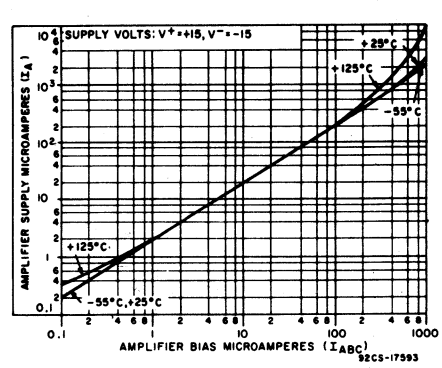


Fig.8 – Amplifier supply current vs. amplifier bias current.

CA3080, CA3080A Types

ELECTRICAL CHARACTERISTICS
For Equipment Design

CA3080

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS Circuit Fig.	TEST CONDITIONS $V^+ = 15$ V, $V^- = -15$ V, $I_{ABC} = 500\ \mu A$, $T_A = 25^oC$ (unless indicated otherwise)	Typical Characteristics Curves Fig.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Input Offset Voltage	V_{IO}	–		3	–	0.4	5	mV
			T_A = 0 to 70°C		–	–	6	
Input Offset Current	I_{IO}	–		4	–	0.12	0.6	μA
Input Bias Current	I_I	–		5	–	2	5	μA
			T_A = 0 to 70°C		–	–	7	
Forward Transconductance (large signal)	g_m	–		14	6700	9600	13000	μmho
			T_A = 0 to 70°C		5400	–	–	
Peak Output Current	$\|I_{OM}\|$	–	R_L = 0	6	350	500	650	μA
			R_L = 0, T_A = 0 to 70°C		300	–	–	
Peak Output Voltage: Positive	V^+_{OM}	–	$R_L = \infty$	7	12	13.5	–	V
Negative	V^-_{OM}				−12	−14.4	–	
Amplifier Supply Current	I_A	–		8	0.8	1	1.2	mA
Device Dissipation	P_D	–		9	24	30	36	mW
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V^+$	–		–	–	–	150	μV/V
Negative	$\Delta V_{IO}/\Delta V^-$	–		–	–	–	150	
Common-Mode Rejection Ratio	CMRR	–		–	80	110	–	dB
Common-Mode Input-Voltage Range	V_{ICR}	–		7	12 to −12	13.6 to −14.6	–	V
Input Resistance	R_I	–		15	10	26	–	kΩ

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

CA3080

Input Offset Voltage	V_{IO}	–	$I_{ABC} = 5\ \mu A$	3	0.3	mV
Input Offset Voltage Change	$\|\Delta V_{IO}\|$	–	Change in V_{IO} between $I_{ABC} = 500\ \mu A$ and $I_{ABC} = 5\ \mu A$	–	0.2	mV
Peak Output Current	I_{OM}	–	$I_{ABC} = 5\ \mu A$	6	5	μA
Peak Output Voltage: Positive	V^+_{OM}	–	$I_{ABC} = 5\ \mu A$	7	13.8	V
Negative	V^-_{OM}				−14.5	
Magnitude of Leakage Current		10	$I_{ABC} = 0$, $V_{TP} = 0$	11	0.08	nA
			$I_{ABC} = 0$, $V_{TP} = 36$ V		0.3	
Differential Input Current		12	$I_{ABC} = 0$, $V_{DIFF} = 4$ V	13	0.008	nA
Amplifier Bias Voltage	V_{ABC}	–		16	0.71	V
Slew Rate: Maximum (uncompensated)	SR			–	75	V/μs
Unity Gain (compensated)		23			50	
Open-Loop Bandwidth	BW_{OL}	–		–	2	MHz
Input Capacitance	C_I	–	f = 1 MHz	17	3.6	pF
Output Capacitance	C_O	–	f = 1 MHz	17	5.6	pF
Output Resistance	R_O	–		18	15	MΩ
Input-to-Output Capacitance	C_{I-O}	19	f = 1 MHz	20	0.024	pF

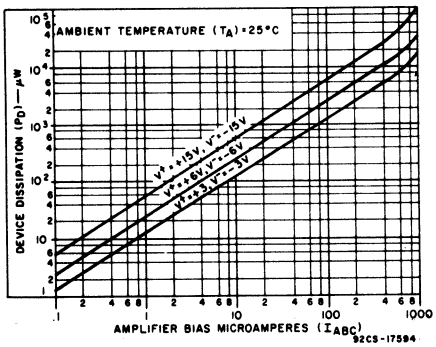


Fig.9 – Total power dissipation vs. amplifier bias current.

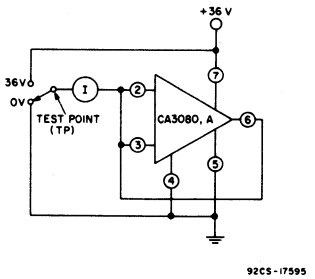


Fig.10 – Leakage current test circuit.

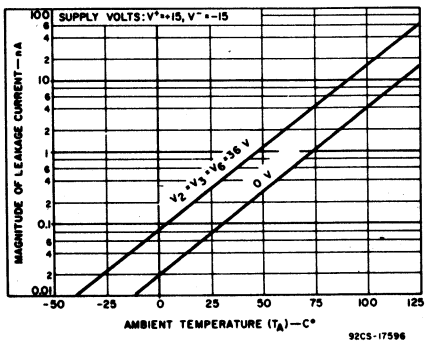


Fig.11 – Leakage current vs. temperature.

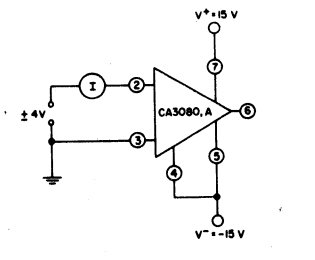


Fig.12 – Differential input current test circuit.

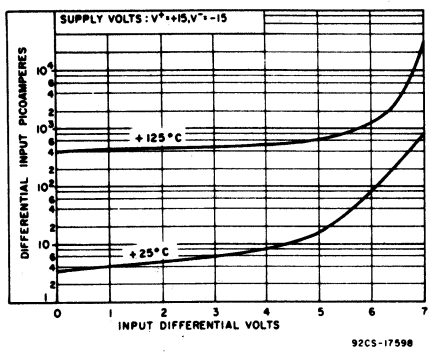


Fig.13 – Input current vs. input differential voltage.

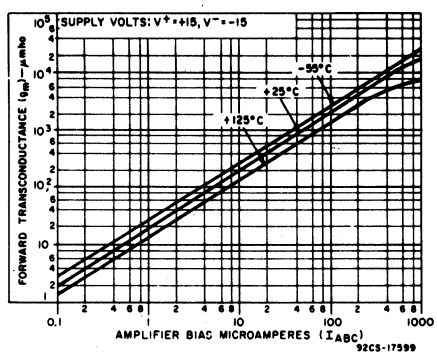


Fig.14 – Transconductance vs. amplifier bias current.

CA3080, CA3080A Types

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTICS	SYMBOLS	Circuit Fig.	TEST CONDITIONS (V^+ = 15 V, V^- = −15 V, I_{ABC} = 500 μA, T_A = 25°C (unless indicated otherwise)	Typical Characteristics Curves Fig.	CA3080A LIMITS Min.	Typ.	Max.	UNITS
Input Offset Voltage	V_{IO}	–	I_{ABC} = 5 μA	3	–	0.3	2	mV
					–	0.4	2	
			T_A = −55 to +125°C		–	–	5	
Input Offset Voltage Change	$\lvert\Delta V_{IO}\rvert$	–	Change in V_{IO} between I_{ABC} = 500 μA and I_{ABC} = 5 μA	3	–	0.1	3	mV
Input Offset Current	I_{IO}	–		4	–	0.12	0.6	μA
Input Bias Current	I_I	–		5	–	2	5	μA
			T_A = −55 to +125		–	–	8	
Forward Transconductance (large signal)	g_m	–		14	7700	9600	12000	μmho
			T_A = −55 to + 125°C		4000	–	–	
Peak Output Current	$\lvert I_{OM}\rvert$		I_{ABC} = 5 μA, R_L = 0	6	3	5	7	μA
			R_L = 0		350	500	650	
			R_L = 0, T_A = −55 to +125°C		300	–	–	
Peak Output Voltage: Positive	$+V_{OM}$	–	I_{ABC} = 5 μA, R_L = ∞	7	12	13.8	–	V
Negative	$-V_{OM}$				−12	−14.5	–	
Positive	$+V_{OM}$	–	R_L = ∞		12	13.5	–	
Negative	$-V_{OM}$				−12	−14.4	–	
Amplifier Supply Current	I_A	–		8	0.8	1	1.2	mA
Device Dissipation	P_D	–		9	24	30	36	mW
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V^+$	–		–	–	–	150	μV/V
Negative	$\Delta V_{IO}/\Delta V^-$				–	–	150	
Magnitude of Leakage Current		10	I_{ABC} = 0, V_{TP} = 0	11	–	0.08	5	nA
			I_{ABC} = 0, V_{TP} = 36 V		–	0.3	5	
Differential Input Current		12	I_{ABC} = 0, V_{DIFF} = 4 V	13	–	0.008	5	nA
Common-Mode Rejection Ratio	CMRR	–		–	80	110	–	dB
Common-Mode Input-Voltage Range	V_{ICR}	–		7	12 to −12	13.6 to −14.6	–	V
Input Resistance	R_I	–		15	10	26	–	kΩ

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only For Design Guidance

					CA3080A	
Amplifier Bias Voltage	V_{ABC}	–		16	0.71	V
Slew Rate: Maximum (uncompensated)	SR			–	75	V/μs
Unity Gain (compensated)		23			50	
Open-Loop Bandwidth	BW_{OL}	–	–	–	2	MHz
Input Capacitance	C_I	–	f = 1 MHz	17	3.6	pF
Output Capacitance	C_O	–	f = 1 MHz	17	5.6	pF
Output Resistance	R_O	–		18	15	MΩ
Input-to-Output Capacitance	$C_{I\text{-}O}$	19	f = 1 MHz	20	0.024	pF

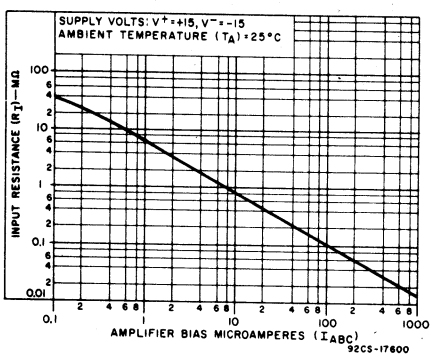


Fig. 15 – Input resistance vs. amplifier bias current.

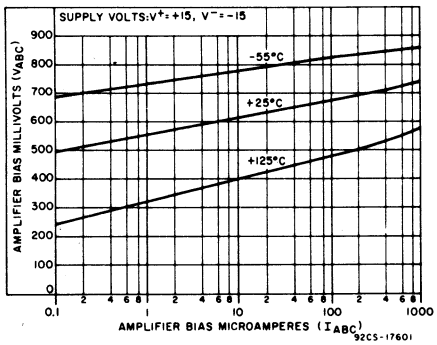


Fig. 16 – Amplifier bias voltage vs. amplifier bias current.

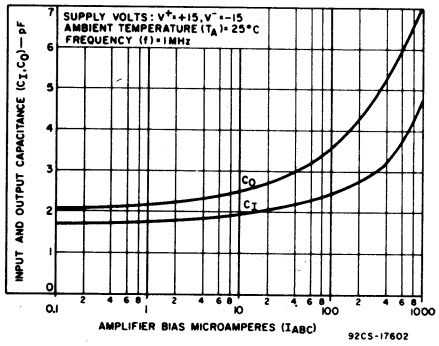


Fig. 17 – Input and output capacitance vs. amplifier bias current.

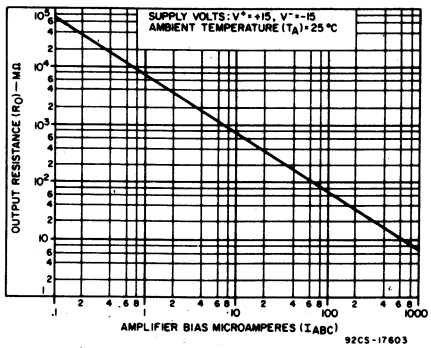


Fig. 18 – Output resistance vs. amplifier bias current.

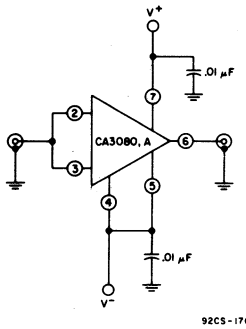


Fig. 19 – Input-to-output capacitance test circuit.

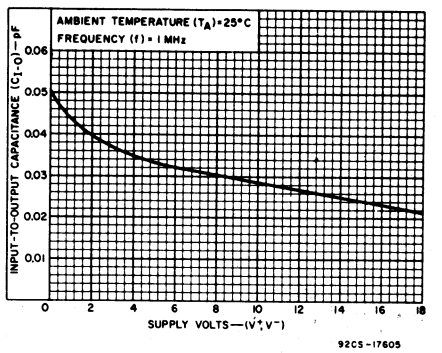


Fig. 20 – Input-to-output capacitance vs. supply voltage.

CA3081, CA3082 Types

General-Purpose High-Current N-P-N Transistor Arrays

CA3081–Common-Emitter Array CA3082–Common-Collector Array

Directly Drive 7-Segment Incandescent Displays and Light-Emitting-Diode (LED) Displays

Features

- **7 transistors permit a wide range of applications in either a common-emitter (CA3081) or common-collector (CA3082) configuration**
- **High I_C: 100 mA max.** **Low $V_{CE\ sat}$ (at 50 mA): 0.4 V typ.**

Applications

- **Drivers for:**
  - **Incandescent display devices (e.g. RCA NUMITRON DR2000 Series and lamps)**
  - **LED (e.g. RCA-SG1002 GaAs High-Efficiency Emitting Diode)**
  - **Relay control –Thyristor firing**

RCA-CA3081* and CA3082* consist of seven high-current (to 100 mA) silicon n-p-n transistors on a common monolithic substrate. The CA3081 is connected in a common-emitter configuration and the CA3082 is connected in a common-collector configuration.

The CA3081 and CA3082 are capable of directly driving seven-segment displays, such as the RCA NUMITRON devices (DR2000 and DR2010), and light-emitting diode (LED) displays. These types are also well-suited for a variety of other driver applications, including relay control and thyristor firing.

The CA3081 and CA3082 are supplied in a 16-lead dual-in-line plastic package, and the CA3081F and CA3082F in a 16-lead dual-in-line frit-seal ceramic package, which includes a separate substrate connection for maximum flexibility in circuit design.

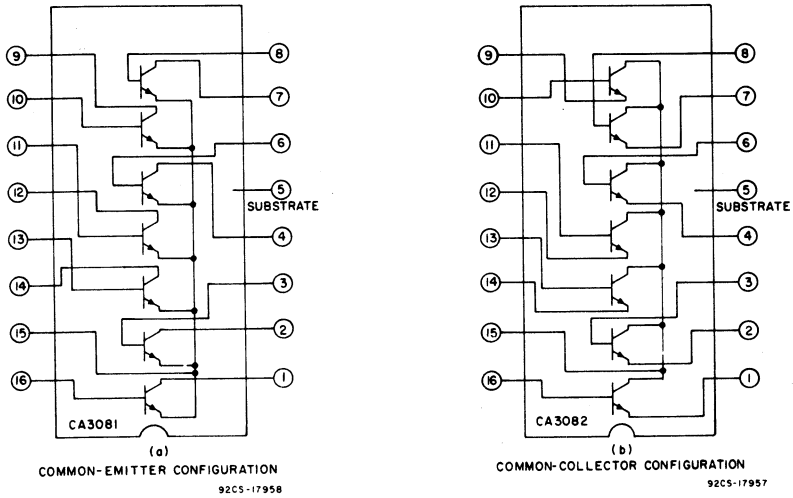


Fig.1–Functional diagrams of types CA3081 and CA3082.

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR OF TYPES CA3081 AND CA3082

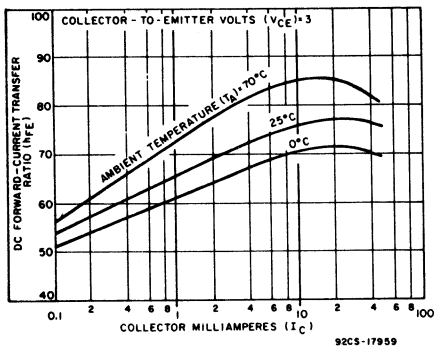


Fig.2–h_{FE} vs. I_C

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Power Dissipation:		
Any one transistor	500	mW
Total package	750	mW
Above 55°C	Derate linearly 6.67	mW/°C
Ambient Temperature Range:		
Operating	–55 to +125	°C
Storage	–65 to + 150	°C
Lead Temperature (During Soldering):		
At distance 1/16" ±1/32" (1.59 mm ±0.79 mm) from case for 10 seconds max.	265	°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage (V_{CEO})	16	V
Collector-to-Base Voltage (V_{CBO})	20	V
Collector-to-Substrate Voltage (V_{CIO})■	20	V
Emitter-to-Base Voltage (V_{EBO})	5	V
Collector Current (I_C)	100	mA
Base Current (I_B)	20	mA

■ The collector of each transistor of the CA3081 and CA3082 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

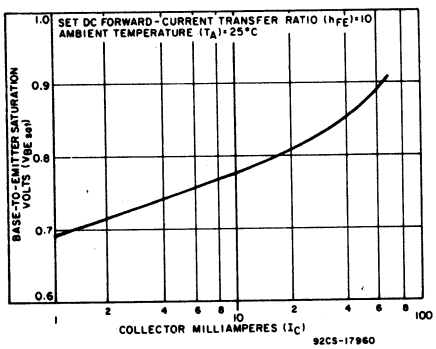


Fig.3–V_{BEsat} vs. I_C

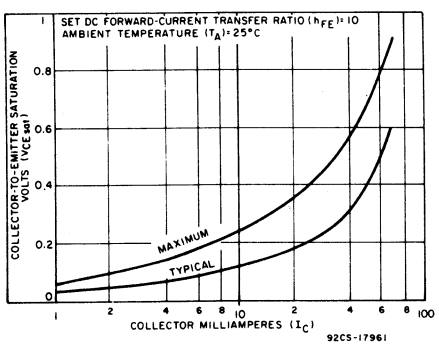


Fig.4–V_{CEsat} vs. I_C at T_A = 25°C.

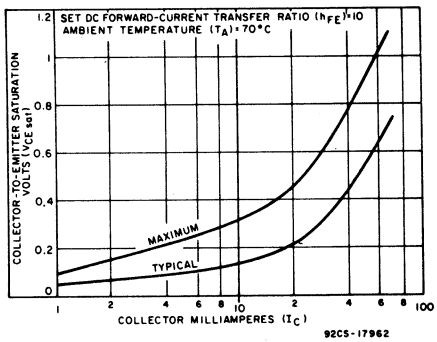


Fig.5–V_{CEsat} vs. I_C at T_A = 70°C.

CA3081, CA3082 Types

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$
For Equipment Design

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	Typ. Char. Curve Fig. No.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Collector-to-Base Breakdown Voltage	$V_{(BR)CES}$	I_C = 500 μA, I_E = 0	–	20	60	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 500 μA, I_E = 0, I_B = 0	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	–	16	24	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_C = 500 μA	–	5	6.9	–	V
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 0.5 V, I_C = 30 mA	–	30	68	–	
		V_{CE} = 0.8 V, I_C = 50 mA	–	40	70	–	
Base-to-Emitter Saturation Voltage	$V_{BE\ sat}$	I_C = 30 mA, I_B = 1 mA	3	–	0.87	1.0	V
Collector-to-Emitter Saturation Voltage: CA3081, CA3082	$V_{CE\ sat}$	I_C = 30 mA, I_B = 1 mA	–	–	0.27	0.5	V
CA3081		I_C = 50 mA, I_B = 5 mA	4	–	0.4	0.7	
CA3082		I_C = 50 mA, I_B = 5 mA	4	–	0.4	0.8	
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10 V, I_B = 0	–	–	–	10	μA
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	–	–	1	μA

TYPICAL READ-OUT DRIVER APPLICATIONS

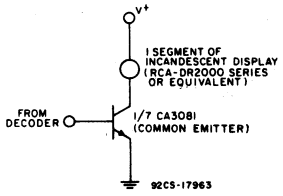


Fig.6—Schematic diagram showing one transistor of the CA3081 driving one segment of an incandescent display.

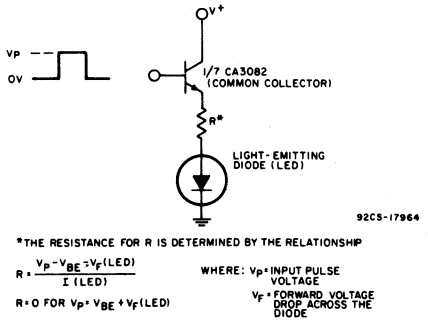


Fig.7—Schematic diagram showing one transistor of the CA3082 driving a light-emitting diode (LED).

CA3083

General-Purpose High-Current N-P-N Transistor Array

RCA-CA3083 is a versatile array of five high-current (to 100mA) n-p-n transistors on a common monolithic substrate. In addition, two of these transistors (Q1 and Q2) are matched at low currents (i.e. 1mA) for applications in which offset parameters are of special importance.

Independent connections for each transistor plus a separate terminal for the substrate permit maximum flexibility in circuit design. The CA3083 is supplied in a 16-lead dual-in-line plastic package, and the CA3083F in a 16-lead dual-in-line frit-seal ceramic package.

Features

- **High I_C: 100mA max.**
- **Low V_{CEsat} (at 50mA): 0.7V max.**
- **Matched pair (Q1 and Q2)–**
  V_{IO} (V_{BE} matched): ± 5 mV max.
  I_{IO} (at 1mA): 2.5 μA max.
- **5 independent transistors plus separate substrate connection**
- **The CA3083 is available in a sealed-junction Beam-Lead version (CA3083L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".**

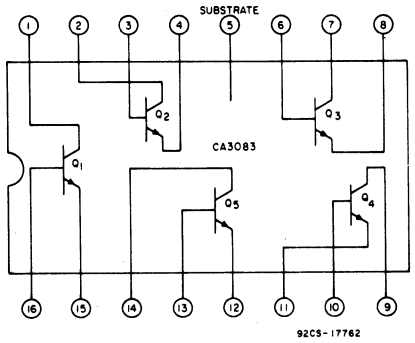


Fig.1–Functional diagram of the CA3083.

Applications

- **Signal processing and switching systems operating from DC to VHF**
- **Lamp and relay driver**
- **Differential amplifier**
- **Temperature-compensated amplifier**
- **Thyristor firing**
- **See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Circuit Transistor Array" for suggested applications**

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Power Dissipation:		
Any one transistor	500	mW
Total package	750	mW
Above 55°C	Derate linearly 6.67	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16" ±1/32" (1.59 mm ±0.79 mm) from case for 10 seconds max.	265	°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage (V_{CEO})	15	V
Collector-to-Base Voltage (V_{CBO})	20	V
Collector-to-Substrate Voltage (V_{CIO})■	20	V
Emitter-to-Base Voltage (V_{EBO})	5	V
Collector Current (I_C)	100	mA
Base Current (I_B)	20	mA

■ The collector of each transistor of the CA3083 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	Typ. Char. Curve Fig. No.	LIMITS Min.	Typ.	Max.	UNITS
For Each Transistor:							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 100μA, I_E = 0	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	–	15	24	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 100μA, I_B = 0, I_E = 0	–	20	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500μA, I_C = 0	–	5	6.9	–	V
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10V, I_B = 0	–	–	–	10	μA
Collector-Cutoff-Current	I_{CBO}	V_{CB} = 10V, I_E = 0	–	–	–	1	μA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3V, I_C = 10mA	2	40	76	–	
		V_{CE} = 3V, I_C = 50mA	2	40	75	–	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 10mA	3	0.65	0.74	0.85	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_C = 50mA, I_B = 5mA	4	–	0.40	0.70	V
For Transistors Q1 and Q2 (As a Differential Amplifier):							
Absolute Input Offset Voltage	$\lvert V_{IO}\rvert$	V_{CE} = 3V, I_C = 1mA	7	–	1.2	5	mV
Absolute Input Offset Current	$\lvert I_{IO}\rvert$		8	–	0.7	2.5	μA

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

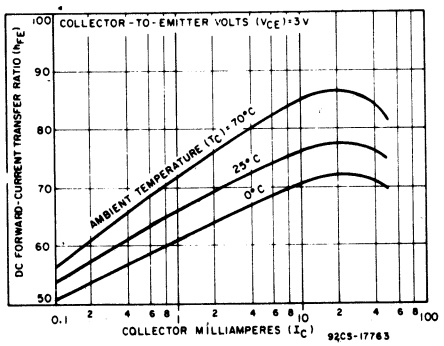


Fig.2 – h_{FE} vs I_C

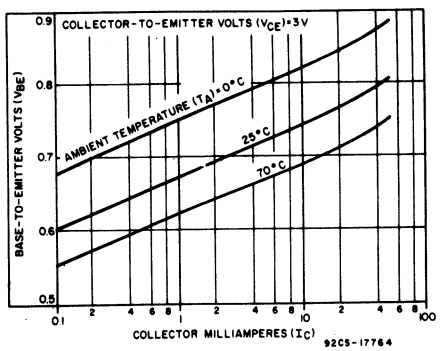


Fig.3 – V_{BE} vs I_C

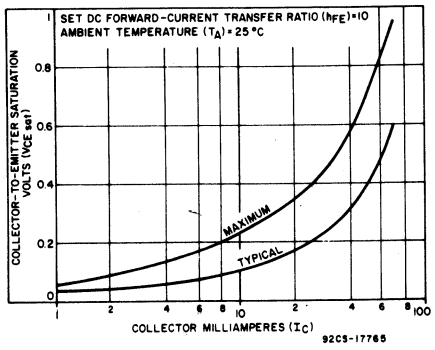


Fig.4 – V_{CEsat} vs I_C at 25°C

CA3083

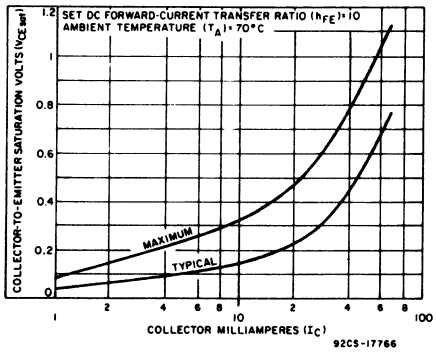


Fig.5 – V_{CEsat} vs I_C at 70°C

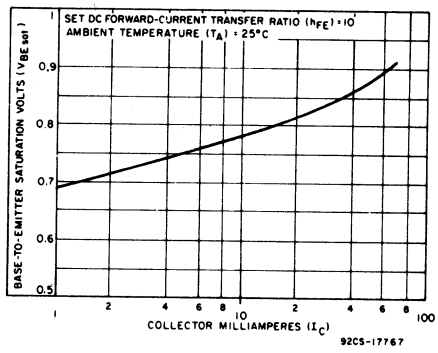


Fig.6 – V_{BEsat} vs I_C

TYPICAL STATIC CHARACTERISTICS FOR DIFFERENTIAL AMPLIFIER

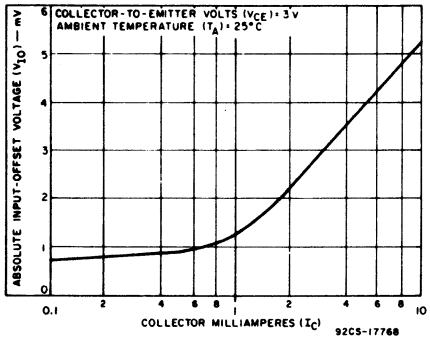


Fig.7 – V_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier).

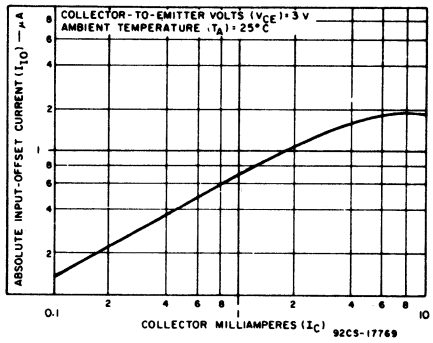


Fig.8 – I_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier).

CA3084

General-Purpose P-N-P Transistor Array

RCA-CA3084 is a general-purpose silicon p-n-p transistor array incorporating two independent transistors, a Darlington circuit, and a current-mirror pair with a shared diode.

The two independent transistors in the array may be used in a variety of circuit applications. The Darlington pair may be employed as the equivalent of a single high-beta transistor. The current-mirror pair is well suited for constant-current applications and can also be used as the active loads in a differential amplifier which uses n-p-n transistors.

The total array is especially useful for a wide range of applications in systems having low-power and low-frequency requirements. Although the transistors may be used as discrete units in conventional circuits, they offer the advantages inherent in integrated-circuit construction, that is, to provide close electrical and thermal matching.

The CA3084 utilizes the 14-lead dual-in-line plastic package.

FEATURES

- **Matched transistor pair (Q1 and Q2)**
  V_{IO} (V_{BE} matched): ± 6mV max.
  I_{IO} (at 100 μA): ± 0.6 μA
- **Wide operating current range**
- **Low noise figure - - 3.2 dB typ. at 1 kHz**
- **The CA3084 is available in a sealed-junction Beam-Lead version (CA3084L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".**

APPLICATIONS

- **General use in signal processing systems having low-power and low-frequency requirements**
- **Differential amplifiers**
- **Temperature compensated amplifiers**
- **Active loads for differential amplifiers using n-p-n transistors**
- **Complementary uses with RCA n-p-n transistor arrays**

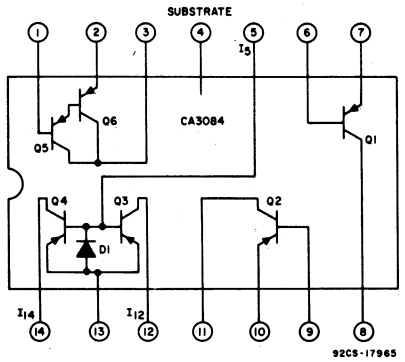


Fig.1 – Functional diagram of the CA3084.

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Dissipation:		
Any one transistor	200	mW
Total package	750	mW
Above T_A = 55°C	derate linearly6.67	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max.	+265	°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage (V_{CEO})	−40	V
Collector-to-Base Voltage (V_{CBO})	−40	V
Base-to-Substrate Voltage (V_{BIO})*	40	V
Emitter-to-Base Voltage (V_{EBO})	−40	V
Collector Current (I_C)	−10	mA

The base of each transistor of the CA3084 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any base voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (4) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

STATIC CHARACTERISTICS FOR EACH TRANSISTOR

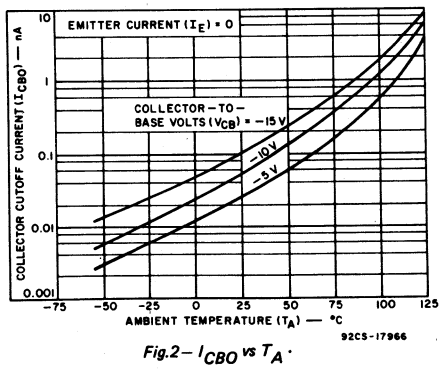


Fig.2 – I_{CBO} vs T_A.

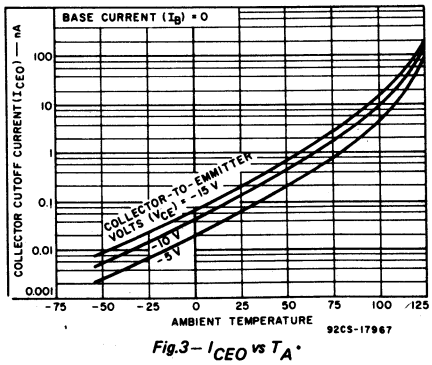


Fig.3 – I_{CEO} vs T_A.

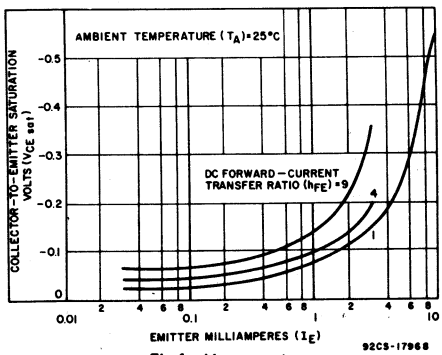


Fig.4 – V_{CEsat} vs I_E.

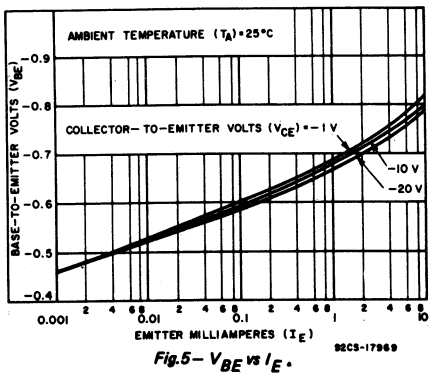


Fig.5 – V_{BE} vs I_E.

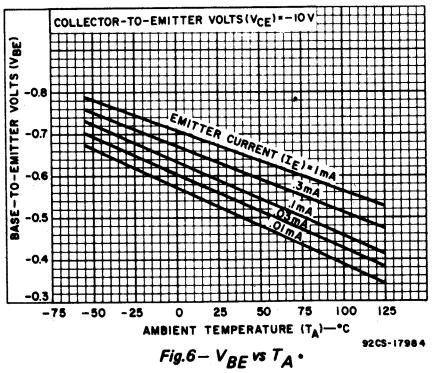


Fig.6 – V_{BE} vs T_A.

CA3084

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	Typ. Characteristics Curve Fig. No.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
For Each Transistor:							
Collector-Cutoff Current	I_{CBO}	V_{CB} = −10V, I_E = 0	2	–	−0.055	−100	nA
Collector-Cutoff Current	I_{CEO}	V_{CE} = −10V, I_B = 0	3	–	−0.12	−100	nA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_{CE} = −100μA, I_B = 0	–	−40	−70	–	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_{CB} = −100μA, I_E = 0	–	−40	−80	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_{EB} = −100μA, I_C = 0	–	−40	−100	–	V
Emitter-to-Substrate Breakdown Voltage	$V_{(BR)EIO}$	I_{EI} = 100μA	–	40	100	–	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_E = 1mA, I_B = 100μA	4	–	−0.125	−0.25	V
Base-to-Emitter Voltage	V_{BE}	I_E = 100μA, V_{CE} = −10V	5	−0.50	−0.59	−0.68	V
DC Forward-Current Transfer Ratio	h_{FE}	I_E = 100μA, V_{CE} = −10V	7	15	40	–	
For Transistors Q1 and Q2 (As a Differential Amplifier):							
Magnitude of Input Offset Voltage	$\lvert V_{IO} \rvert$	I_E = 100μA, V_{CE} = −10V	8	–	0.422	6	mV
Input Offset Current	I_{IO}	I_E = 100μA, V_{CE} = −10V	–	−0.6	0	0.6	μA
For Transistors Q3 and Q4 (Current-Mirror Configuration):							
Collector Current (Normalized)	I_C/I_5	V_{CE} = −5V, V_{CIO} = −5V, Term. 13 = Gnd. I_5 = −100μA,	10	0.85	1.00	1.15	
Magnitude of Collector Current Ratio	$\lvert I_{C(Q3)}/I_{C(Q4)} \rvert$	V_{CE} = −5V, V_{CIO} = −5V, Term. 13 = Gnd. I_5 = −100μA,	11	0.90	1.00	1.10	
For Transistors Q5 and Q6 (Darlington Configuration):							
Collector-Cutoff Current	I_{CEO}	V_{CE} = −10V, I_B = 0	–	–	–	−1.0	μA
Base-to-Emitter Voltage	V_{BE}	I_E = 100μA, V_{CE} = −10V	13	0.92	1.07	1.20	V
DC Forward-Current Transfer Ratio	h_{FE}	I_E = 100μA, V_{CE} = −10V	15	100	1230	–	

ELECTRICAL CHARACTERISTICS at T_A = 25°C
Typical Values Intended Only For Design Guidance

Magnitude of Temperature Coefficient:							
V_{BE} (for each transistor)	$\lvert \Delta V_{BE}/\Delta T \rvert$	I_E = 100μA,	6		−1.78		mV/°C
V_{IO} (as a differential amplifier)	$\lvert \Delta V_{IO}/\Delta T \rvert$	V_{CE} = −10V	9		0.54		μV/°C
V_{BE} (Darlington configuration)	$\lvert \Delta V_{BE}/\Delta T \rvert$		14		−3.7		mV/°C
For Each Transistor:							
Input Resistance	R_I	f = 1kHz, V_{CE} = −10V,	19		9		kΩ
Output Resistance	R_O	I_C = −100μA	20	–	600	–	kΩ
Forward Transconductance	g_m		22	–	3	–	mmho
Collector-to-Base Capacitance	C_{CBO}	I_{CB} = 0	23	–	3.3	–	pF
Collector-to-Emitter Capacitance	C_{CEO}	I_{CE} = 0	23	–	2.5	–	pF
Base-to-Substrate Capacitance	C_{BIO}	I_{CIO} = 0	23	–	4.5	–	pF

STATIC CHARACTERISTICS FOR EACH TRANSISTOR

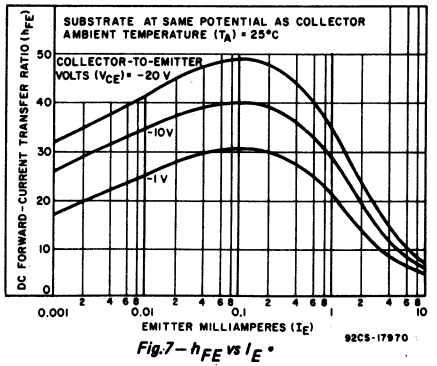


Fig.7 – h_{FE} vs I_E.

STATIC CHARACTERISTICS FOR DIFFERENTIAL AMPLIFIER

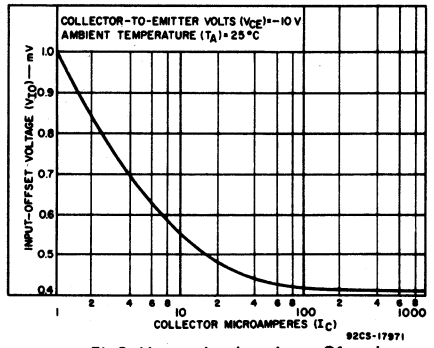


Fig.8–V_{IO} vs I_C, (transistors Q1 and Q2 as a differential amplifier).

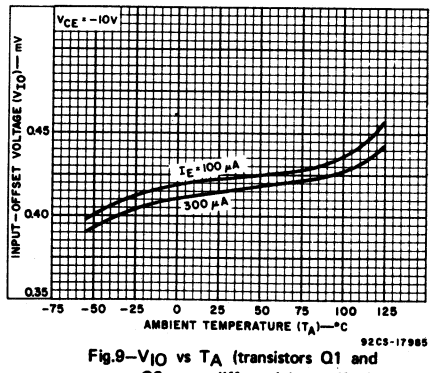


Fig.9–V_{IO} vs T_A (transistors Q1 and Q2 as a differential amplifier).

STATIC CHARACTERISTICS FOR CURRENT-MIRROR CONFIGURATION

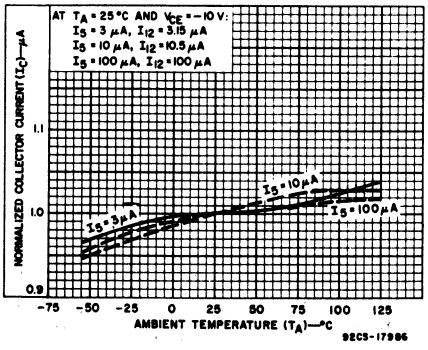


Fig.10–Normalized I_C vs T_A (transistors Q3 and Q4 in a current-mirror configuration.

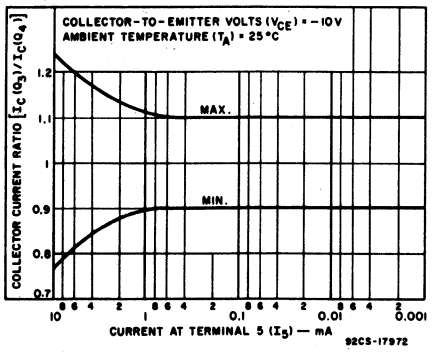


Fig.11–I_C ratio vs I_5 (transistors Q3 and Q4 in a current-mirror configuration.

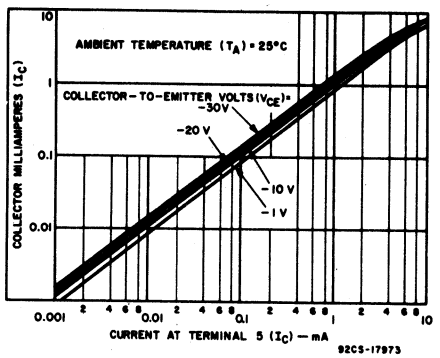


Fig.12 – I_C vs I_5 (transistors Q3 and Q4 in a current-mirror configuration).

CA3084

STATIC CHARACTERISTICS FOR DARLINGTON CONFIGURATION

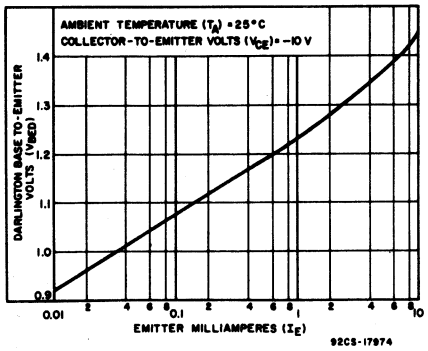


Fig.13 – V_{BE} vs I_E (transistors Q5 and Q6 in a darlingtron configuration).

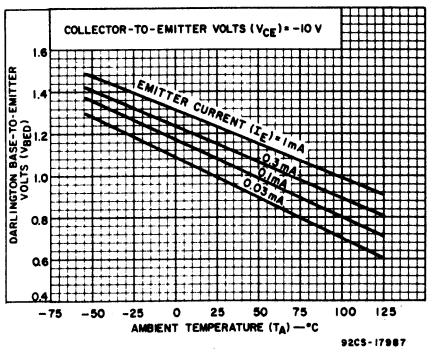


Fig.14 – V_{BE} vs T_A (transistors Q5 and Q6 in a darlington configuration).

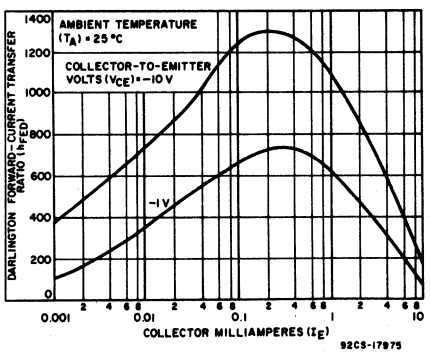


Fig.15 – h_{FE} vs. I_E (transistors Q5 and Q6 in a darlington configuration).

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

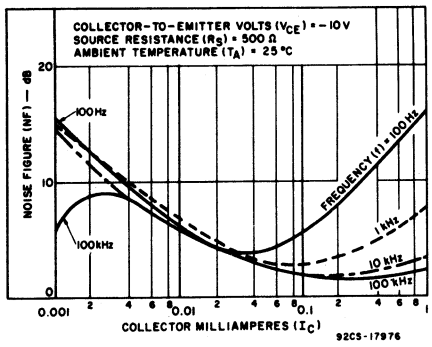


Fig.16 – NF vs I_C at R_S = 500 Ω

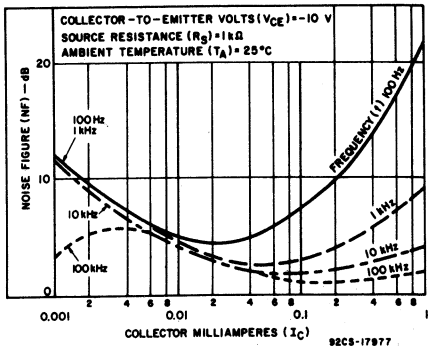


Fig.17 – NF bs I_C at R_S = 1 kΩ

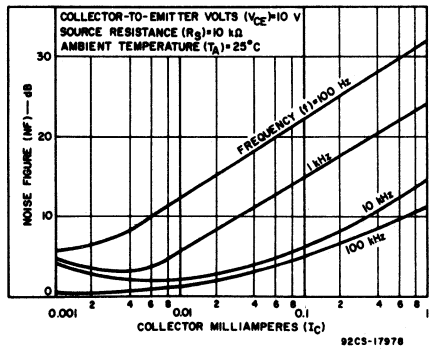


Fig.18 – NF vs I_C at R_S = 10kΩ

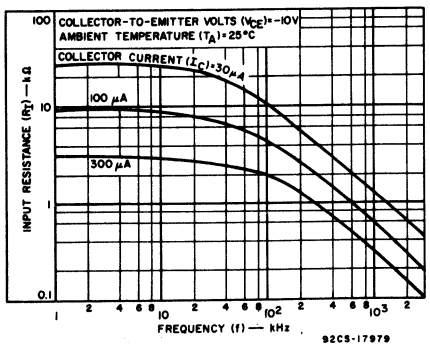


Fig.19 – R_I vs f

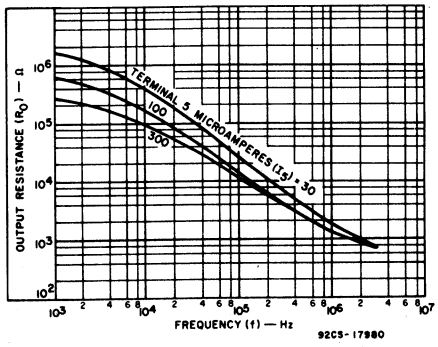


Fig.20 – R_O vs f

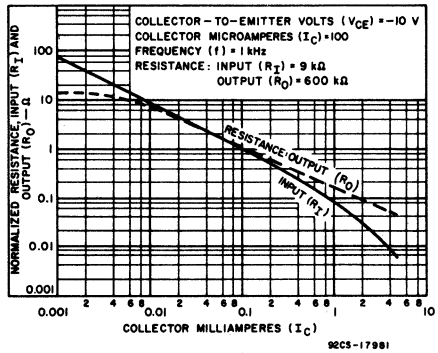


Fig.21 – Normalized R_I and R_O vs I_C

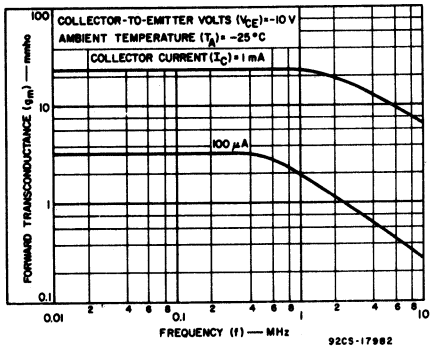


Fig.22 – g_m vs f

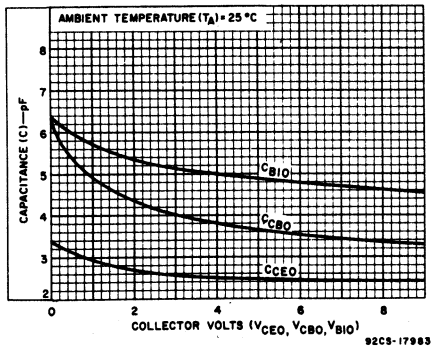


Fig.23 – Transistor capacitances vs collector voltages (V_{CEO}, V_{CBO}, V_{CIO})

CA3085, CA3085A, CA3085B Types

Positive Voltage Regulators

For Regulated Voltages from 1.7 V to 46 V at Currents up to 100 mA

RCA-CA3085, CA3085A, and CA3085B are silicon monolithic integrated circuits designed specifically for service as voltage regulators at output voltages ranging from 1.7 to 46 volts at currents up to 100 milliamperes.

A block diagram of the CA3085 Series is shown in Fig. 1. The diagram shows the connecting terminals that provide access to the regulator circuit components. The voltage regulators provide important features such as: frequency compensation, short-circuit protection, temperature-compensated reference voltage, current limiting, and booster input. These devices are useful in a wide range of applications for regulating high-current, switching, shunt, and positive and negative voltages. They are also applicable for current and dual-tracking regulation.

The CA3085A and CA3085B have output current capabilities up to 100 mA and the CA3085 up to 12 mA without the use of external pass transistors. However, all the devices can provide voltage regulation at load currents greater than 100 mA with the use of suitable external pass transistors. The CA3085 Series has an unregulated input voltage ranging from 7.5 to 30 V (CA3085), 7.5 to 40 V (CA3085A), and 7.5 to 50 V (CA3085B) and a minimum regulated output voltage of 26 V (CA3085), 36 V (CA3085A), and 46 V (CA3085B).

The CA3085A is unilaterally interchangeable with the CA3055.

The CA3085 is available in a sealed-junction Beam-Lead version (CA3085L). For further information see File No. 515, "Beam-Lead Devices for Hybrid Circuit Applications".

Type	V_{IN} Range V	V_{OUT} Range V	Max. I_{OUT} mA	Max. Load Regulation % V_{OUT}
CA3085	7.5 to 30	1.8 to 26	12*	0.1
CA3085A	7.5 to 40	1.7 to 36	100	0.15
CA3085B	7.5 to 50	1.7 to 46	100	0.15

* This value may be extended to 100 mA; however, regulation is not specified beyond 12 mA.

These types are supplied in the 8-lead TO-5 style package (CA3085, CA3085A, CA3085B, and the 8-lead TO-5 with dual-in-line formed leads ("DIL-CAN", CA3085S, CA3085AS, CA3085BS). The CA3085 is also supplied in the 8-lead dual-in-line plastic package ("MINI-DIP". CA3085E), and in chip form (CA3085H).

Features

- **Up to 100 mA output current**
- **Input and output short-circuit protection**
- **Load and line regulation: 0.025%**
- **Pin compatible with LM100 Series**
- **Adjustable output voltage**
- Low noise

Applications

- **Shunt voltage regulator**
- **Current regulator**
- **Switching voltage regulator**
- **High-current voltage regulator**
- **Combination positive and negative voltage regulator**
- **Dual tracking regulator**
- See Application Note ICAN-6157 "Applications of the CA3085-Series Monolithic IC Voltage Regulators".

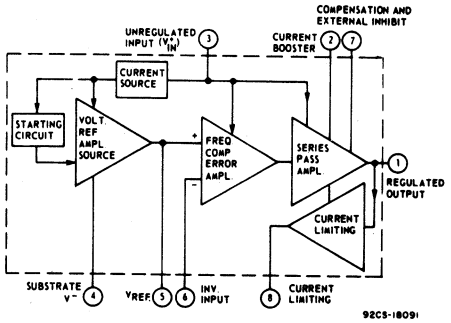


Fig. 1—Block diagram of CA3085 Series.

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES at T_A = 25°C

POWER DISSIPATION: WITHOUT HEAT SINK	WITH HEAT SINK (TO-5 ONLY)
up to T_A = 55°C ..... 630 mW	up to T_C = 55°C .... 1.6 W
above T_A = 55°C derate linearly @6.67 mW/°C	above T_C = 55°C .... derate linearly at 16.7 mW/°C

TEMPERATURE RANGE:
Operating ..... −55 to +125°C
Storage ..... −65 to +150°C

UNREGULATED INPUT VOLTAGE:
CA3085 ..... 30 V
CA3085A ..... 40 V
CA3085B ..... 50 V

LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. ..... +265°C

Maximum Voltage Ratings
The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical Terminal No. 7 and horizontal Terminal No. 1 is +3 to −10 volts.

MAXIMUM VOLTAGE RATINGS

TERMINAL No.	5	6	7	8	1	2	3	4
5	–	+5 −5	•	•	•	•	•	+10 0
6	–	–	•	•	•	•	•	•
7	–	–	–	+3 −10	+3 −10	•	•	+‡ 0
8	–	–	–	–	+5 −1	•	•	•
1	–	–	–	–	–	+10 −‡	0 −‡	+‡ 0
2	–	–	–	–	–	–	0 –	+‡ 0
3	–	–	–	–	–	–	–	+‡ 0
4	–	–	–	–	–	–	–	Substrate & Case

*Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.

‡30 V for CA3085
40 V for CA3085A
50 V for CA3085B

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
5	10	1.0
6	1.0	−0.1
7	1.0	−1.0
8	0.1	10
1	20	150
2	150	60
3	150	60
4	–	–

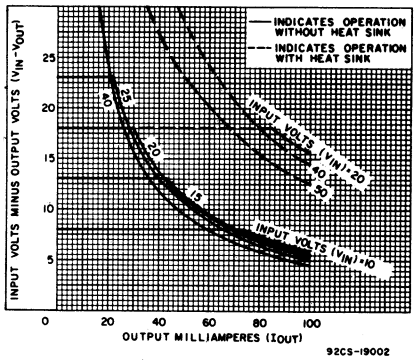


Fig. 3—Dissipation limitation (V_{IN}−V_{OUT} vs. I_{OUT}).

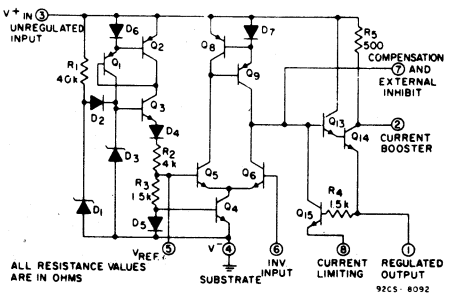


Fig. 2—Schematic diagram of CA3085 Series.

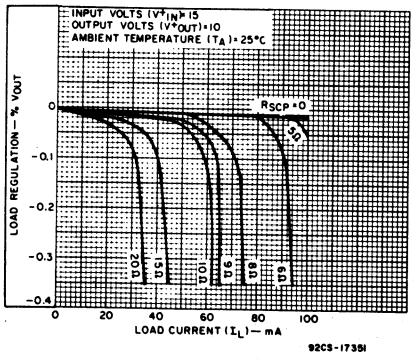


Fig. 4—Load regulation characteristics.

CA3085, CA3085A, CA3085B Types

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	TEST CONDITIONS: Test Circuit Fig. No.	TEST CONDITIONS: T_A = 25°C [Unless indicated otherwise]	LIMITS: CA3085 MIN.	CA3085 TYP.	CA3085 MAX.	CA3085A MIN.	CA3085A TYP.	CA3085A MAX.	CA3085B MIN.	CA3085B TYP.	CA3085B MAX.	UNITS
Reference Voltage	V_{REF}	15	V^+_{IN} = 15V	1.4	1.6	1.8	1.5	1.6	1.7	1.5	1.6	1.7	V
Quiescent Regulator Current	$I_{quiescent}$	15	V^+_{IN} = 30V	–	3.3	4.5	—	–	–	–	–	–	mA
			V^+_{IN} = 40V	–	–	–	–	3.65	5	–	–	–	
			V^+_{IN} = 50V	–	–	–	–	–	–	–	4.05	7	
Input Voltage Range	$V_{IN(range)}$	–	–	7.5	–	30	7.5	–	40	7.5	–	50	V
Maximum Output Voltage	$V_{O(max.)}$	15	V^+_{IN} = 30, 40, 50V#; R_L = 365 Ω; Term. No. 6 to Gnd.	26	27	–	36	37	–	46	47	–	V
Minimum Output Voltage	$V_{O(min.)}$	15	V^+_{IN} = 30V	–	1.6	1.8	–	1.6	1.7	–	1.6	1.7	V
Input-Output Voltage Differential	V_{IN}-V_{OUT}	–	–	4	–	28	4	–	38	3.5	–	48	V
Limiting Current	I_{LIM}	16	V^+_{IN} = 16V, V^+_{OUT} = 10V R_{SCP}* = 6Ω	–	96	120	–	96	120	–	96	120	mA
Load Regulation●	–	–	I_L = 1 to 100mA, R_{SCP} = 0	–	–	–	–	0.025	0.15	–	0.025	0.15	%V_{OUT}
		–	I_L = 1 to 100mA, R_{SCP} = 0, T_A = 0°C to +70°C	–	–	–	–	0.035	0.6	–	0.035	0.6	
		–	I_L = 1 to 12mA, R_{SCP} = 0	–	0.003	0.1	–	–	–	–	–	–	
Line Regulation▲	–	–	I_L = 1 mA, R_{SCP} = 0	–	0.025	0.1	–	0.025	0.075	–	0.025	0.04	%/V
		–	I_L = 1mA, R_{SCP} = 0, T_A = 0°C to +70°C	–	0.04	0.15	–	0.04	0.1	–	0.04	0.08	
Equivalent Noise Output Voltage■	V_{NOISE}	12	V^+_{IN} = 25V, C_{REF} = 0	–	0.5	–	–	0.5	–	–	0.5	–	mV p-p
			C_{REF} = 0.22μF	–	0.3	–	–	0.3	–	–	0.3	–	
Ripple Rejection	–	13	V^+_{IN} = 25V, f = 1kHz, C_{REF} = 0	–	50	–	–	50	–	45	50	–	dB
			C_{REF} = 2μF	–	56	–	–	56	–	50	56	–	
Output Resistance	r_o	13	V^+_{IN} = 25V, f = 1kHz	–	0.075	1.1	–	0.075	0.3	–	0.075	0.3	Ω
Temperature Coefficient of Reference and Output Voltages	ΔV_{REF}, ΔV_o	–	I_L = 0, V_{REF} = 1.6V	–	0.0035	–	–	0.0035	–	–	0.0035	–	%/°C
Load Transient Recovery Time: Turn On	t_{ON}	14	V^+_{IN} = 25V, +50mA Step	–	1	–	–	1	–	–	1	–	μs
Turn Off	t_{OFF}		V^+_{IN} = 25V, −50mA Step	–	3	–	–	3	–	–	3	–	μs
Line Transient Recovery Time: Turn On	t_{ON}	–	V^+_{IN} = 25V, f = 1kHz, 2V Step	–	0.8	–	–	0.8	–	–	0.8	–	μs
Turn Off	t_{OFF}	–		–	0.4	–	–	0.4	–	–	0.4	–	μs

30V (CA3085), 40V(CA3085A), 50V(CA3085B)

* R_{SCP}: Short-circuit protection resistance

■ Bandwidth DC to 10 MHz.

● Load Regulation = $\frac{\Delta V_{OUT}}{V_{OUT(initial)}} \times 100\%$

▲ Line Regulation = $\frac{(\Delta V_{OUT})}{[V_{OUT(initial)}]\ (\Delta V_{IN})} \times 100\%$

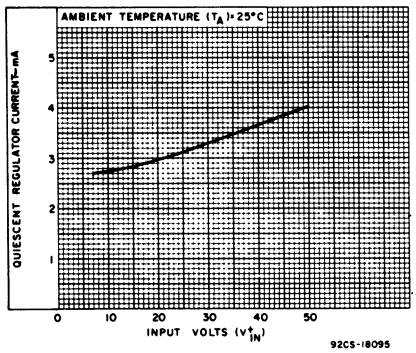


Fig.5–$I_{quiescent}$ vs. V^+_{IN}.

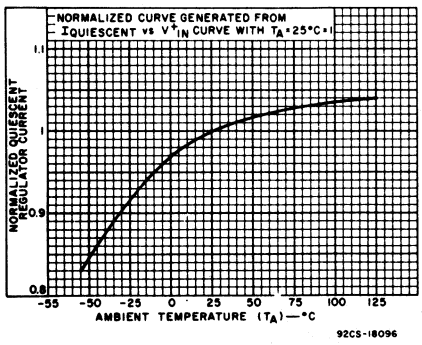


Fig.6–Normalized $I_{quiescent}$ vs. T_A.

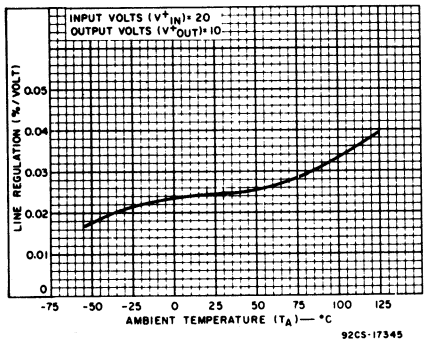


Fig.7–Line regulation temperature characteristics.

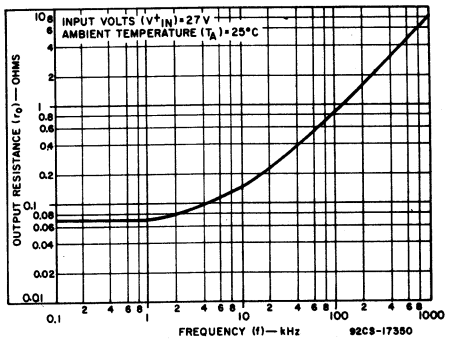


Fig.8–r_o vs. f.

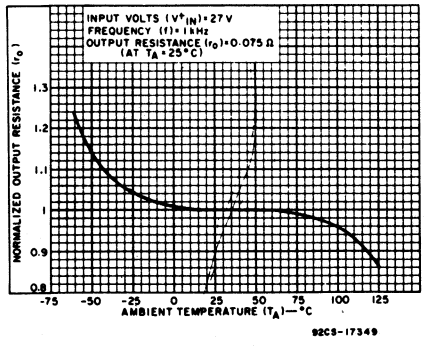


Fig.9–Normalized r_o vs. T_A.

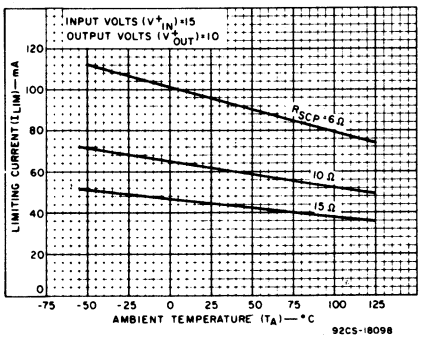


Fig.10–I_{LIM} vs. T_A.

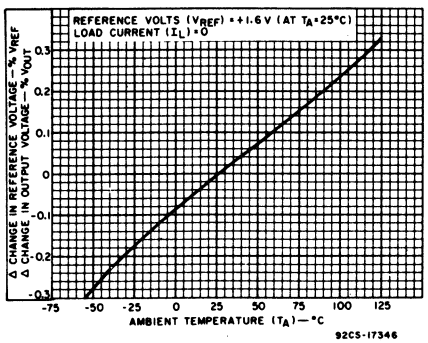


Fig.11–Temperature coefficient of V_{REF} and V_{OUT}.

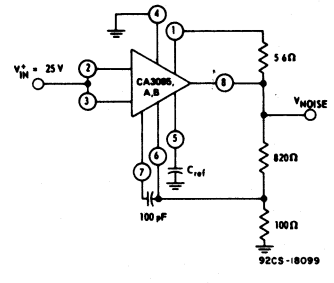


Fig.12–Test circuit for noise voltage.

CA3085, CA3085A, CA3085B Types

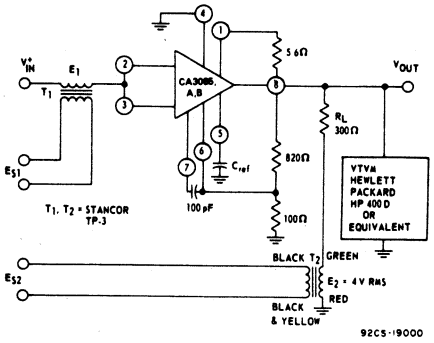


Fig.13—Test circuit for ripple rejection and output resistance.

TEST PROCEDURES FOR TEST CIRCUIT FOR RIPPLE REJECTION AND OUTPUT RESISTANCE

Output Resistance

Conditions:

1. V_{IN} = +25 V, C_{REF} = 0, Short E_1
2. Set E_{S2} at 1 kHz so that E_2 = 4 V rms
3. Read V_{OUT} on a VTVM, such as a Hewlett-Packard, HP400D or equivalent
4. Calculate R_{OUT} from $R_{OUT} = V_{OUT}(R_L/E_2)$

Ripple Rejection — I

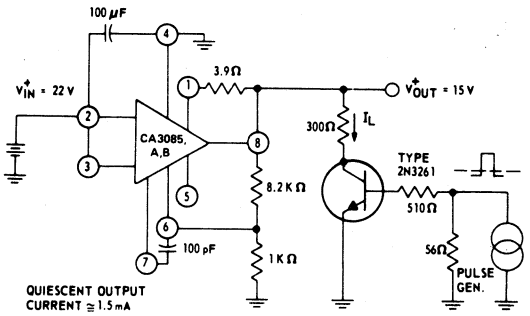
Conditions:

1. V_{IN} = +25 V, C_{REF} = 0, Short E_2
2. Set E_{S1} at 1 kHz so that E_1 = 3 V rms
3. Read V_{OUT} on a VTVM, such as a Hewlett-Packard, HP400D or equivalent
4. Calculate Ripple Rejection from 20 log (E_1/V_{OUT})

Ripple Rejection — II

Conditions:

1. Repeat Ripple Rejection I with C_{REF} = 2 μF



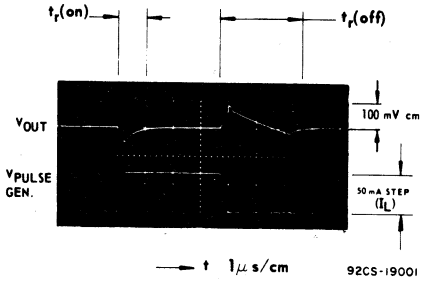
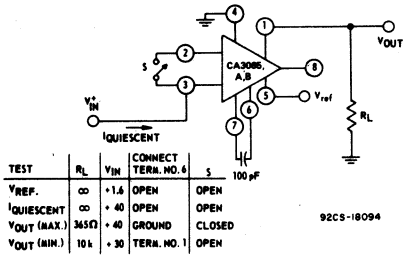


Fig.14—Turn-on and turn-off recovery time test circuit with associated waveforms.



TEST	R_L	V_{IN}	CONNECT TERM. NO. 6	S
V_{REF}	∞	+1.6	OPEN	OPEN
$I_{QUIESCENT}$	∞	+40	OPEN	OPEN
V_{OUT} (MAX.)	365Ω	+40	GROUND	CLOSED
V_{OUT} (MIN.)	10 k	+30	TERM. NO. 1	OPEN

Fig.15—Test circuit for V_{REF}, $I_{quiescent}$, $V_{OUT(max.)}$, $V_{OUT(min.)}$.

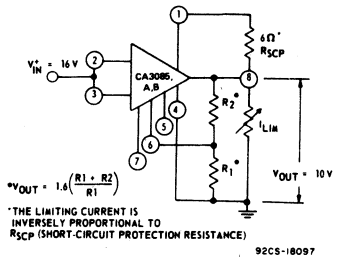


Fig.16—Test circuit for limiting current

TYPICAL REGULATOR CIRCUITS USING THE CA3085 SERIES

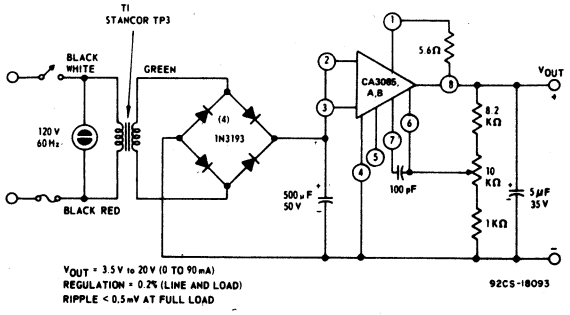
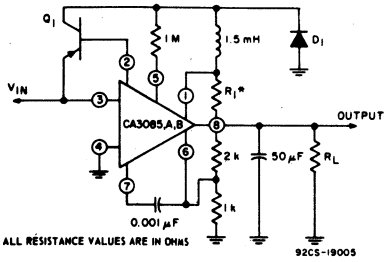
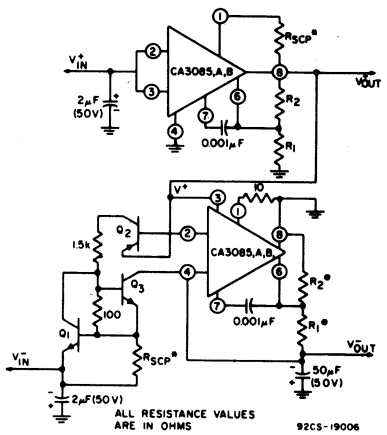


Fig.17—Application of the CA3085 Series in a typical power supply.



D1: RCA-1N1763A OR EQUIVALENT
Q1: RCA-2N5322 OR EQUIVALENT
*R1 = 0.7 I_L (MAX.)

Fig.18—Typical switching regulator circuit.



ALL RESISTANCE VALUES ARE IN OHMS

Q1 RCA-2N2102 OR EQUIVALENT
Q2 ANY P-N-P SILICON TRANSISTOR (RCA-2N5322 OR EQUIVALENT)
Q3 ANY N-P-N SILICON TRANSISTOR THAT CAN HANDLE THE DESIRED LOAD CURRENT (RCA-2N3772 OR EQUIVALENT)

*$V_{OUT} = \left(\frac{R_1 + R_2}{R_1}\right)$

*R_{SCP} SHORT-CIRCUIT PROTECTION RESISTANCE

Fig.21— Combination positive and negative voltage regulator circuit.

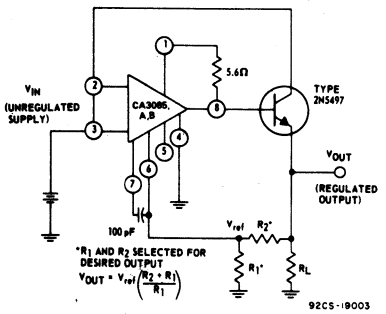
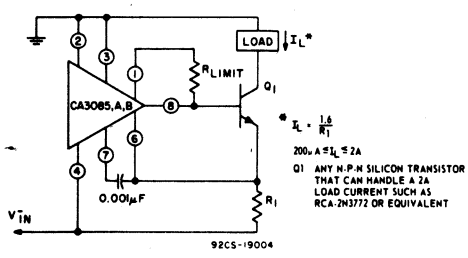


Fig.19— Typical high-current voltage regulator circuit.



Q1 ANY N-P-N SILICON TRANSISTOR THAT CAN HANDLE A 2A LOAD CURRENT SUCH AS RCA-2N3772 OR EQUIVALENT

Fig.20— Typical current regulator circuit.

CA3086
General-Purpose N-P-N Transistor Array

Three Isolated Transistors and One Differentially– Connected Transistor Pair

For Low–Power Applications from DC to 120MHz

RCA-CA3086 consists of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair.

The transistors of the CA3086 are well suited to a wide variety of applications in low-power systems at frequencies from DC to 120 MHz. They may be used as discrete transistors in conventional circuits. However, they also provide the very significant inherent advantages unique to integrated circuits, such as compactness, ease of physical handling and thermal matching.

The CA3086 is supplied in a 14-lead dual-in line plastic package. The CA3086F is supplied in a 14-lead dual-in-line hermetic (frit-seal) ceramic package.

Applications

- **General-purpose use in signal processing systems operating in the DC to 120-MHz range**
- **Temperature compensated amplifiers**
- **See RCA Application Note, ICAN-5296 "Application of the RCA-CA3018 Integrated-Circuit Transistor Array" for suggested applications.**

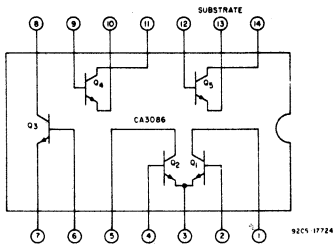


Fig.1 – Functional diagram of the CA3086.

MAXIMUM RATINGS, Absolute–Maximum Values at T_A = 25°C

DISSIPATION:		
Any one transistor	300	mW
Total package up to T_A = 55°C	750	mW
Above T_A = 55°C	derate linearly 6.67	mW/°C
AMBIENT TEMPERATURE RANGE:		
Operating	–55 to + 125	°C
Storage	–65 to + 150	°C
LEAD TEMPERATURE (During soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) From case for 10 seconds max.	+ 265	°C
The following ratings apply for each transistor in the device:		
COLLECTOR-TO-EMITTER VOLTAGE, V_{CEO}	15	V
COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	20	V
COLLECTOR-TO-SUBSTRATE VOLTAGE, V_{CIO}*	20	V
EMITTER-TO-BASE VOLTAGE, V_{EBO}	5	V
COLLECTOR CURRENT, I_C	50	mA

* The collector of each transistor in the CA3086 is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action. To avoid undesirable coupling between transistors, the substrate (terminal 13) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	Typ. Characteristic Curves Fig. No.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	–	15	24	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	–	20	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	–	5	7	–	V
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0	2	–	0.002	100	nA
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10V, I_B = 0	3	—	See Curve	5	μA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3V, I_C = 1mA	4	40	100	–	

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

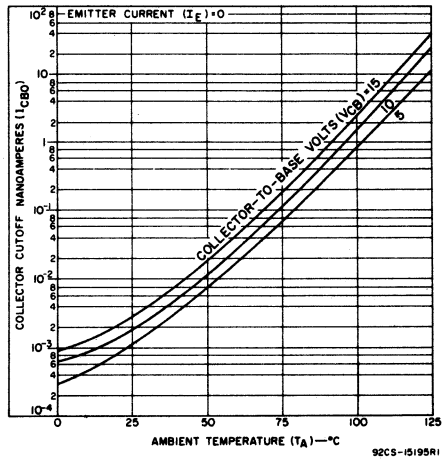


Fig.2– I_{CBO} vs T_A.

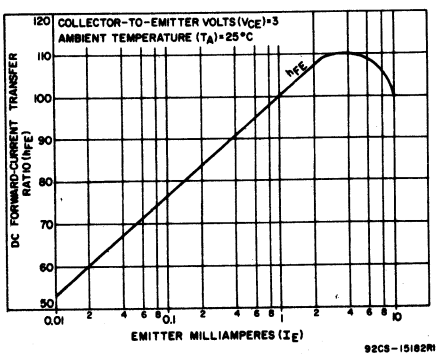


Fig.3– h_{FE} vs I_E.

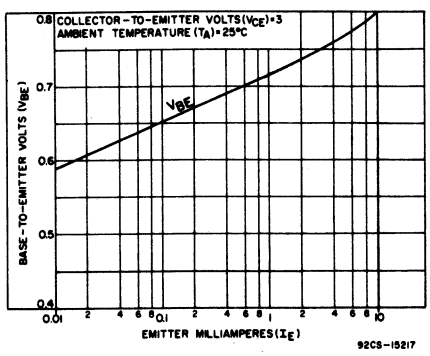


Fig.4 V_{BE} vs I_E.

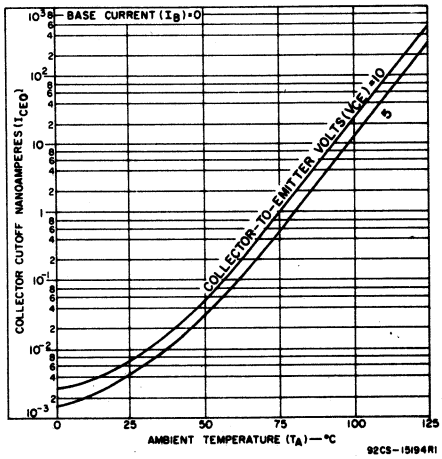


Fig.5– I_{CEO} vs T_A.

CA3086

ELECTRICAL CHARACTERISTICS at T_A = 25°C Typical Values Intended Only for Design Guidance

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		Typ. Characteristics Curves Fig. No.	TYPICAL VALUES	UNITS
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3 V	I_C = 10 mA	4	100	
			I_C = 10 μA	4	54	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V	I_E = 1 mA	5	0.715	V
			I_E = 10 mA	5	0.800	V
V_{BE} Temperature Coefficient	$\Delta V_{BE}/\Delta T$	V_{CE} = 3V, I_C = 1mA		6	−1.9	mV/°C
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_B = 1mA, I_C = 10mA		–	0.23	V
Noise Figure (low frequency)	NF	f = 1kHz, V_{CE} = 3V, I_C = 100μA, R_S = 1k Ω		–	3.25	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:						
Forward Current-Transfer Ratio	h_{fe}	f = 1kHz, V_{CE} = 3V, I_C = 1mA		7	100	–
Short-Circuit Input Impedance	h_{ie}			7	3.5	kΩ
Open-Circuit Output Impedance	h_{oe}			7	15.6	μmho
Open-Circuit Reverse-Voltage Transfer Ratio	h_{re}			7	1.8×10^{-4}	–
Admittance Characteristics:						
Forward Transfer Admittance	Y_{fe}	f = 1MHz, V_{CE} = 3V, I_C = 1mA		8	31 − j1.5	mmho
Input Admittance	Y_{ie}			9	0.3 + j0.04	mmho
Output Admittance	Y_{oe}			10	0.001 + j0.03	mmho
Reverse Transfer Admittance	Y_{re}			11	See Curve	–
Gain-Bandwidth Product	f_T	V_{CE} = 3V, I_C = 3mA		12	550	MHz
Emitter-to-Base Capacitance	C_{EBO}	V_{EB} = 3V, I_E = 0		–	0.6	pF
Collector-to-Base Capacitance	C_{CBO}	V_{CB} = 3V, I_C = 0		–	0.58	pF
Collector-to-Substrate Capacitance	C_{CIO}	V_{CI} = 3V, I_C = 0		—	2.8	pF

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

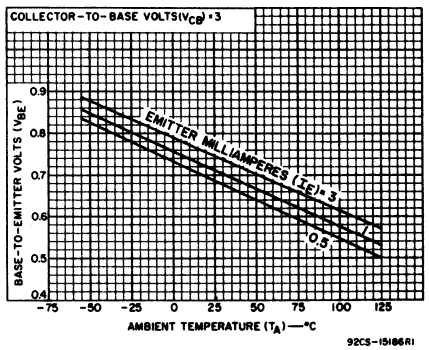


Fig.6– V_{BE} vs T_A.

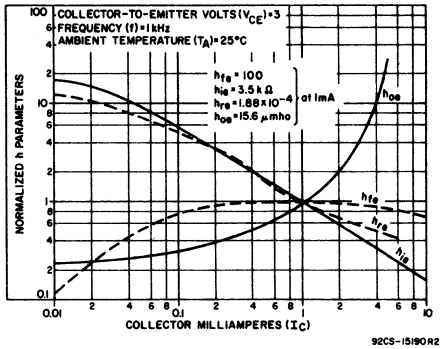


Fig.7– Normalized h_{fe}, h_{ie}, h_{oe}, h_{re} vs I_C.

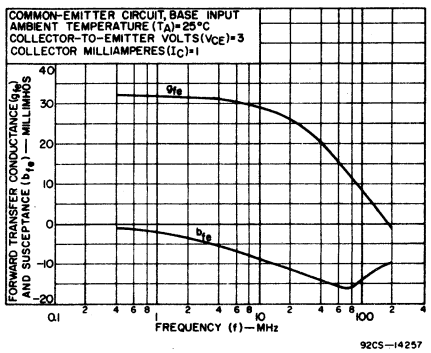


Fig.8– y_{fe} vs f.

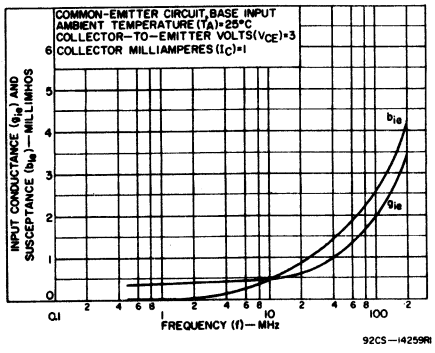


Fig.9– y_{ie} vs f.

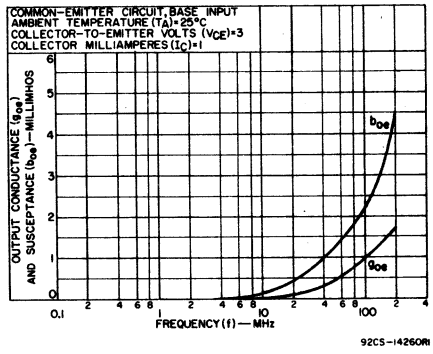


Fig.10– y_{oe} vs f.

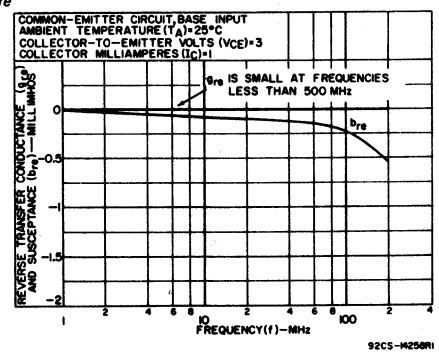


Fig.11– y_{re} vs f.

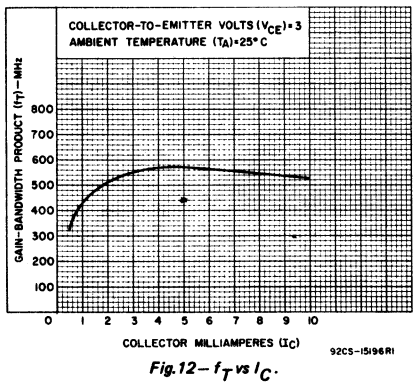


Fig.12– f_T vs I_C.