CA3094, CA3094A, CA3094B Types

Programmable Power Switch/ Amplifier

For Control & General-Purpose Applications

CA3094: For Operation Up to 24 Volts
CA3094A: For Operation Up to 36 Volts
CA3094B: For Operation Up to 44 Volts

APPLICATIONS:

- **Error-signal detector: temperature control with thermistor sensor; speed control for shunt wound dc motor**
- **Over-current, over-voltage, over-temperature protectors**
- **Dual-tracking power supply with RCA-CA3085**
- **Wide-frequency-range oscillator ■ Analog timer**
- **Level detector ■ Alarm systems ■ Voltage follower**
- **Ramp-voltage generator ■ High-power comparator**
- **Ground-fault interrupter (GFI) circuits**

The CA3094 is a differential-input power-control switch/amplifier with auxiliary circuit features for ease of programmability. For example, an error or unbalance signal can be amplified by the CA3094 to provide an on-off signal or proportional-control output signal up to 100 mA. This signal is sufficient to directly drive high-current thyristors, relays, dc loads, or power transistors. The CA3094 has the generic characteristics of the RCA-CA3080 operational amplifier directly coupled to an integral Darlington power transistor capable of sinking or driving currents up to 100 mA.

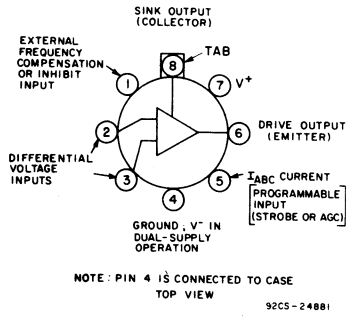
The gain of the differential input stage is proportional to the amplifier bias current (I_{ABC}), permitting programmable variation of the integrated circuit sensitivity with either digital and/or analog programming signals. For example, at an I_{ABC} of 100 μA, a one-millivolt change at the input will change the output from 0 to 100 mA (typical).

The CA3094 is intended for operation up to 24 volts and is especially useful for timing circuits, in automotive equipment, and in other applications where operation up to 24 volts is a primary design requirement (see Figs.27,28 and 29 in Applications Section). The CA3094A and CA3094B are like the CA3094 but are intended for operation up to 36 and 44 volts, respectively (single or dual supply).

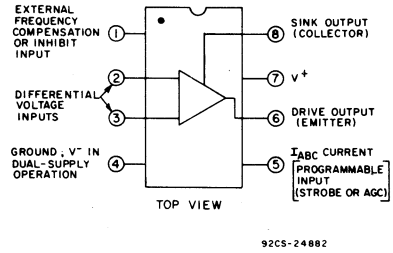
Application Note ICAN-6668 describes the rudiments of Operational Transconductance Amplifiers (OTA's).

These types are available in 8-lead TO-5 style packages with standard leads ("T" suffix) and with dual-in-line formed leads "DIL-CAN" ("S" suffix). Type CA3094 is also available in an 8-lead dual-in-line plastic package "MINI-DIP" ("E" suffix), and in chip form ("H" suffix).

APPLICATION NOTE ICAN-6048 GIVES DETAILED APPLICATION INFORMATION FOR THE CA3094, CA3094A, AND CA3094B.



TO-5 Style Package



Plastic Package

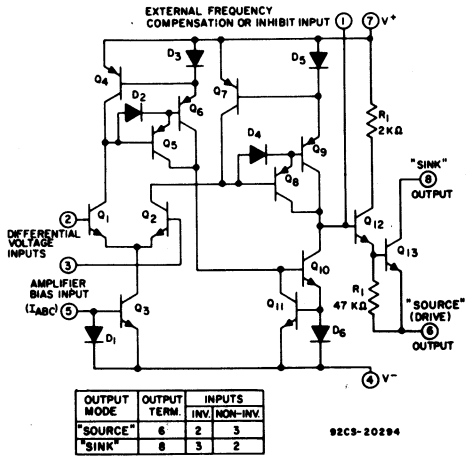
Features:

- **Designed for *single* or dual power supply**
- **Programmable: strobing, gating, squelching, AGC capabilities**
- **Can deliver 3 watts (avg.) or 10 W (peak) to external load (in switching mode)**
- **High-power, single-ended class A amplifier will deliver power output of 0.6 watt (1.6 W device dissipation)**
- **Total harmonic distortion (THD) @ 0.6 W in class A operation – 1.4% typ.**
- **High current-handling capability – 100 mA (avg.), 300 mA (peak)**
- **Sensitivity controlled by varying bias current**
- **Output: "sink" or "drive" capability**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	CA3094	CA3094A	CA3094B	
DC SUPPLY VOLTAGE:				
Dual Supply	± 12 V	± 18 V	± 22 V	V
Single Supply	24 V	36 V	44 V	V
DC DIFFERENTIAL INPUT VOLTAGE (Terminals 2 and 3)	± 5*			V
DC COMMON-MODE INPUT VOLTAGE	Term. 4 ≤ Term. 2 & 3 ≤ Term. 7			
PEAK INPUT SIGNAL CURRENT (Terminals 2 and 3)	± 1			mA
PEAK AMPLIFIER BIAS CURRENT (Terminal 5)	2			mA
OUTPUT CURRENT:				
Peak	300			mA
Average	100			mA
DEVICE DISSIPATION:				
Up to T_A = 55°C:				
Without heat sink	630			mW
With heat sink	1.6			W
Above T_A = 55°C:				
Without heat sink derate linearly	6.67			mW/°C
With heat sink derate linearly	16.7			mW/°C
THERMAL RESISTANCE (Junction to Air)	140			°C/W
AMBIENT TEMPERATURE RANGE:				
Operating	–55 to +125			°C
Storage	–65 to +150			°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+ 300			°C

*Exceeding this voltage rating will not damage the device unless the peak input signal current (1 mA) is also exceeded.



OUTPUT MODE	OUTPUT TERM.	INPUTS INV.	INPUTS NON-INV.
"SOURCE"	6	2	3
"SINK"	8	3	2

Fig. 1–Schematic diagram of CA3094.

Typical Characteristics Curves

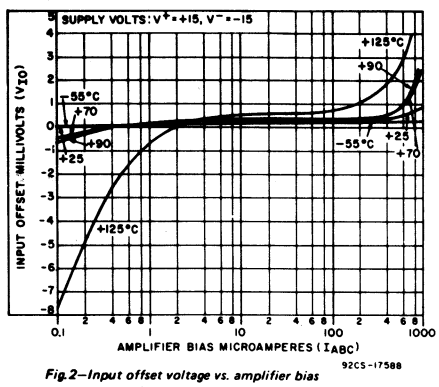


Fig.2–Input offset voltage vs. amplifier bias current (I_{ABC}, terminal No. 5).

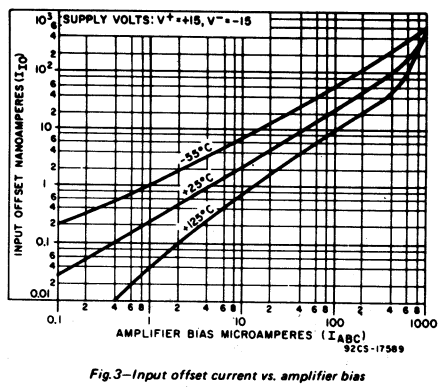


Fig.3–Input offset current vs. amplifier bias current (I_{ABC}, terminal No. 5).

CA3094, CA3094A, CA3094B Types

ELECTRICAL CHARACTERISTICS at T_A = 25°C For Equipment Design

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS			UNITS
		Test Circuit Fig. No.	Single Supply V^+ = 30 V Dual Supply V^+ = 15 V, V^- = 15 V I_{ABC} = 100 μA Unless Otherwise Specified	Char. Curves Fig. No.	Min.	Typ.	Max.	
INPUT PARAMETERS								
Input Offset Voltage	V_{IO}	17	T_A = 25°C	2	–	0.4	5	mV
			T_A = 0 to 70°C		–	–	7	mV
Input-Offset-Voltage Change	$\lvert\Delta V_{IO}\rvert$		Change in V_{IO} Between I_{ABC} = 100 μA and I_{ABC} = 5 μA		–	1	8	mV
Input Offset Current	I_{IO}	18	T_A = 25°C	3	–	0.02	0.2	μA
			T_A = 0 to 70°C		–	–	0.3	μA
Input Bias Current	I_I	19	T_A = 25°C	4	–	0.2	0.50	μA
			T_A = 0 to 70°C		–	–	0.70	μA
Device Dissipation	P_D	18	I_{out} = 0	5, 6	8	10	12	mW
Common-Mode Rejection Ratio	C_{MRR}	20			70	110	–	dB
Common-Mode Input–Voltage Range	V_{ICR}	20	V^+ = 30 V High	7	27	28.8	–	V
			Low		1.0	0.5	–	V
			V^+ = 15 V	7	+12	+13.8	–	V
			V^- = 15 V		−14	−14.5	–	V
Unity Gain-Bandwidth			I_C = 7.5 mA V_{CE} = 15 V I_{ABC} = 500 μA		–	30	–	MHz
Open-Loop Bandwidth At −3 dB Point	BW_{OL}		I_C = 7.5 mA V_{CE} = 15 V I_{ABC} = 500 μA	12	–	4	–	kHz
Total Harmonic Distortion (Class A Operation)	THD		P_D = 220 mW		–	0.4	–	%
			P_D = 600 mW		–	1.4	–	
Amplifier Bias Voltage (Terminal No.5 to Terminal No.4)	V_{ABC}				–	0.68	–	V
Input Offset Voltage Temperature Coefficient	$\Delta V_{IO}/\Delta T$				–	4	–	μV/°C
Power-Supply Rejection	$\Delta V_{IO}/\Delta V$	17			–	15	150	μV/V
1/F Noise Voltage	E_N	21	f = 10 Hz I_{ABC} = 50 μA	8	–	18	–	$\eta V/\sqrt{Hz}$
1/F Noise Current	I_N	21	f = 10 Hz I_{ABC} = 50 μA	9	–	1.8	–	$pA/\sqrt{Hz}$
Differential Input Resistance	R_I		I_{ABC} = 20 μA		0.50	1	–	MΩ
Differential Input Capacitance	C_I		f = 1 MHz V^+ = 30 V		–	2.6	–	pF

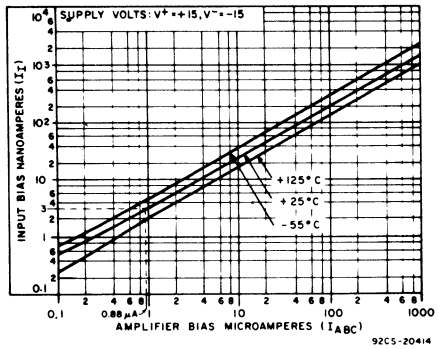


Fig.4—Input bias current vs. amplifier bias current (I_{ABC}, terminal No. 5).

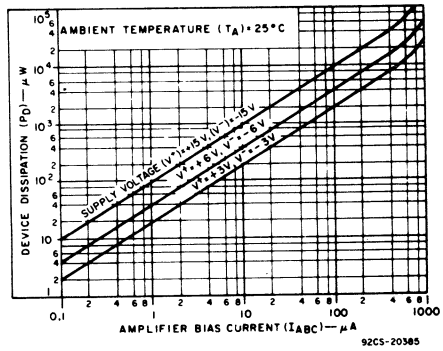


Fig.5—Device dissipation vs. amplifier bias current (I_{ABC}, terminal No. 5).

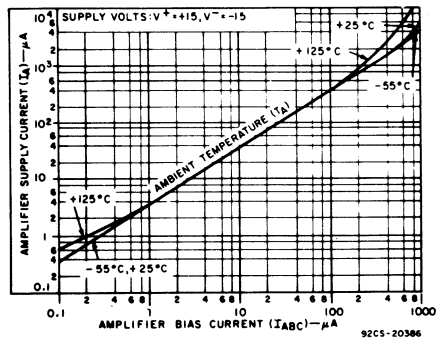


Fig.6—Amplifier supply current vs. amplifier bias current (I_{ABC}, terminal No. 5).

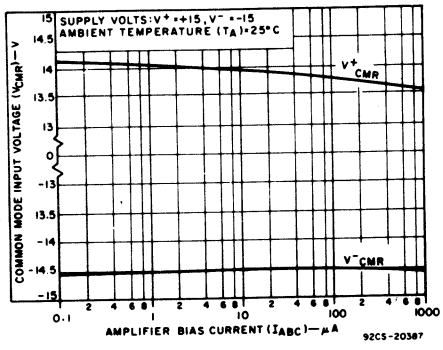


Fig.7—Common mode input voltage vs. amplifier bias current (I_{ABC}, terminal No. 5).

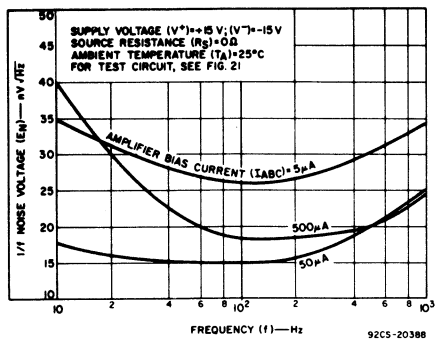


Fig.8—1/F Noise voltage vs. frequency.

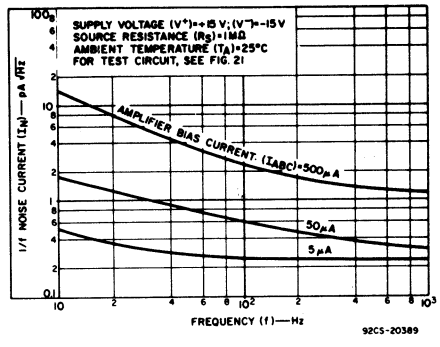


Fig.9—1/F Noise current vs. frequency.

CA3094, CA3094A, CA3094B Types

ELECTRICAL CHARACTERISTICS at T_A = 25°C For Equipment Design

CHARACTERISTIC	SYMBOL	TEST CONDITIONS			LIMITS			UNITS
		Test Circuit Fig. No.	Single Supply V^+ = 30 V Dual Supply V^+ = 15 V, V^- = 15 V I_{ABC} = 100 μA Unless Otherwise Specified	Char. Curves Fig. No.	Min.	Typ.	Max.	
OUTPUT PARAMETERS (Differential Input Voltage = 1V)								
Peak Output Voltage: (Terminal No. 6)			V^+ = 30 V					
With Q13 "ON"	V^+_{OM}		R_L = 2 kΩ to ground		26	27	–	V
With Q13 "OFF"	V^-_{OM}				–	0.01	0.05	V
Peak Output Voltage: (Terminal No. 6)			V^+ = +15 V, V^- = -15 V				0.5	
Positive	V^+_{OM}		R_L = 2 kΩ to −15 V		+11	+12	–	V
Negative	V^-_{OM}				–	−14.99	−14.95	V
Peak Output Voltage: (Terminal No. 8)			V^+ = 30 V					
With Q13 "ON"	V^+_{OM}		R_L = 2 kΩ to 30 V		29.95	29.99	–	V
With Q13 "OFF"	V^-_{OM}				–	0.040	–	V
Peak Output Voltage: (Terminal No. 8)			V^+ = 15 V, V^- = − 15 V					
Positive	V^+_{OM}		R_L = 2 kΩ to + 15 V		+14.95	+14.99	–	V
Negative	V^-_{OM}				–	14.96	–	V
Collector-to-Emitter Saturation Voltage (Terminal No. 8)	$V_{CE(sat)}$		V^+ = 30 V, I_C = 50 mA, Terminal No.6 grounded	10	–	0.17	0.80	V
Output Leakage Current (Terminal No. 6 to Terminal No. 4)			V^+ = 30 V		–	2	10	μA
Composite Small-Signal Current Transfer Ratio (Beta) (Q_{12} and Q_{13})	h_{fe}		V^+ = 30 V, V_{CE} = 5 V, I_C = 50 mA	11	16,000	100,000	–	
Output Capacitance:			f = 1 MHz,					
Terminal No. 6	C_O		All Remaining Terminals Tied to Terminal No. 4		–	5.5	–	pF
Terminal No. 8					–	17	–	pF
TRANSFER PARAMETERS								
Voltage Gain	A		V^+ = 30 V, I_{ABC} = 100 μA		20,000	100,000	–	V/V
		22	ΔV_{out} = 20 V, R_L = 2 kΩ	12	86	100	–	dB
Forward Transconductance To Terminal No. 1	g_m			13	1650	2200	2750	μmhos
Slew Rate:								
Open Loop:								
Positive Slope		23	I_{ABC} = 500 μA, R_L = 2 kΩ	14	–	500	–	V/μs
Negative Slope					–	50	–	V/μs
Unity Gain (Non-Inverting, Compensated)		24	I_{ABC} = 500 μA, R_L = 2 kΩ	15	–	0.7	–	V/μs

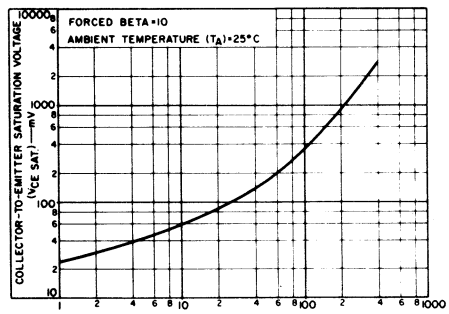
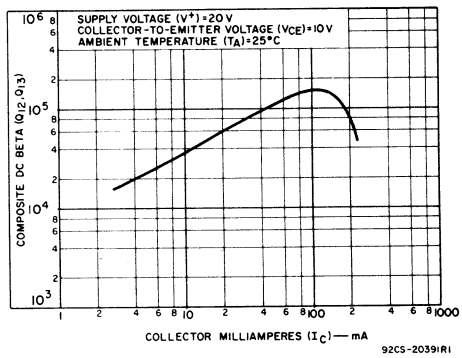


Fig.10—Collector-emitter saturation voltage vs. collector current of output transistor Q_{13}.



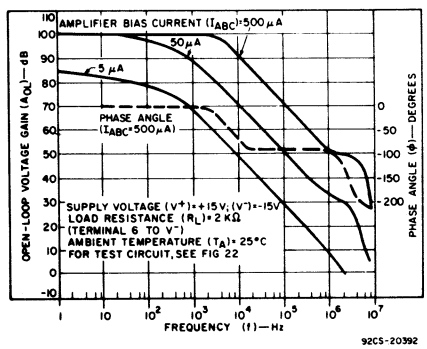


Fig.12—Open-loop voltage gain vs. frequency.

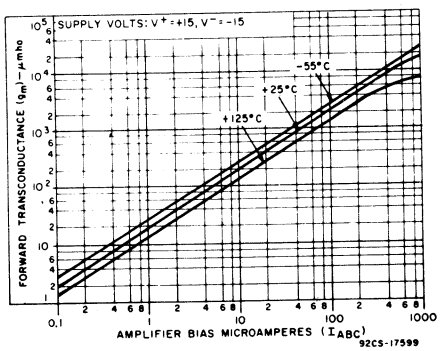


Fig.13—Forward transconductance vs. amplifier bias current.

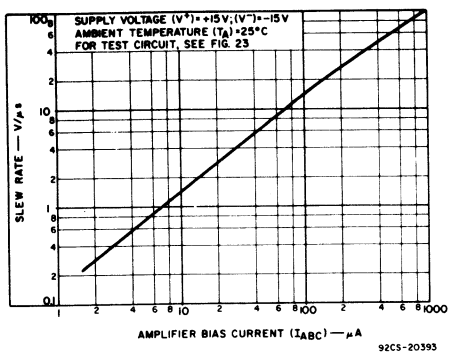


Fig.14—Slew rate vs. amplifier bias current.

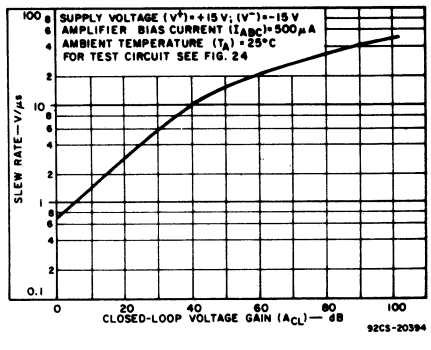


Fig.15—Slew rate vs. closed-loop voltage gain.

CA3094, CA3094A, CA3094B Types

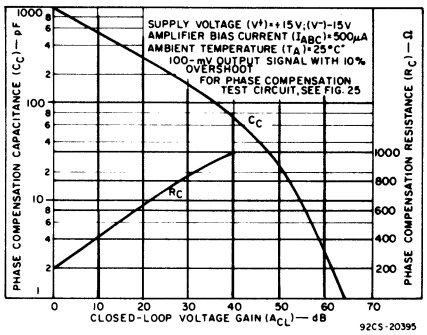


Fig. 16—Phase compensation capacitance and resistance vs. closed-loop voltage gain.

OPERATING CONSIDERATIONS

The "Sink" Output (terminal No. 8) and the "Drive" Output (terminal No. 6) of the CA3094 are not inherently current (or power) limited. Therefore, if a load is connected between terminal No. 6 and terminal No. 4 (V− or ground), it is important to connect a current-limiting resistor between terminal 8 and terminal No. 7 (V^+) to protect transistor Q_{13} under shorted load conditions. Similarly, if a load is connected between terminal No. 8 and terminal No. 7, the current-limiting resistor should be connected between terminal 6 and terminal No. 4 or ground. In circuit applications where the emitter of the output transistor is not connected to the most negative potential in the system, it is recommended that a 100-ohm current-limiting resistor be inserted between terminal No. 7 and the V^+ supply.

TEST CIRCUITS

1/F Noise Measurement Circuit

When using the CA3094, A, or B audio amplifier circuits, it is frequently necessary to consider the noise performance of the device. Noise measurements are made in the circuit shown in Fig. 21. This circuit is a 30-dB, non-inverting amplifier with emitter-follower output and phase compensation from terminal No. 2 to ground. Source resistors (Rs) are set to 0.Ω or 1 MΩ for ^{E} noise and ^{I} noise measurements, respectively. These measurements are made at frequencies of 10 Hz, 100 Hz, and 1 kHz with a 1-Hz measurement bandwidth. Typical values for 1/f noise at 10 Hz and 50 μA I_{ABC} are E_n = 18 nV/$\sqrt{Hz}$ and I_N = 1.8 pA/$\sqrt{Hz}$.

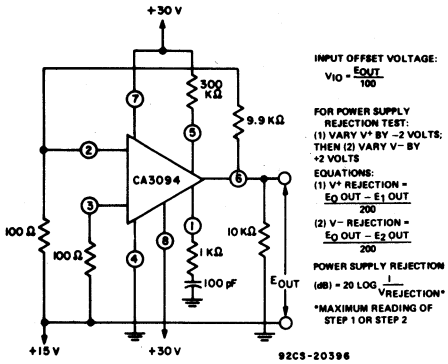


Fig. 17—Input offset voltage and power-supply rejection test circuit.

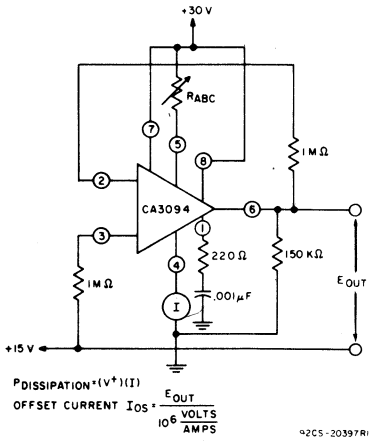


Fig. 18—Input offset current test circuit.

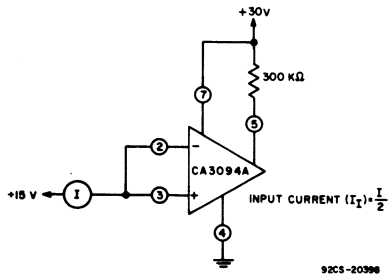


Fig. 19—Input bias current test circuit.

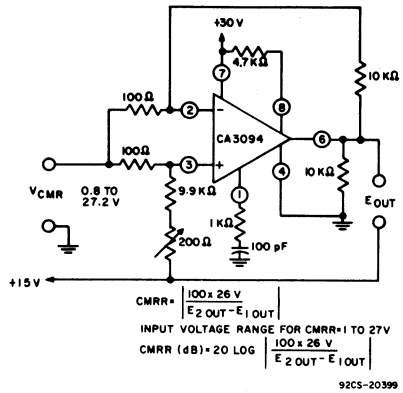
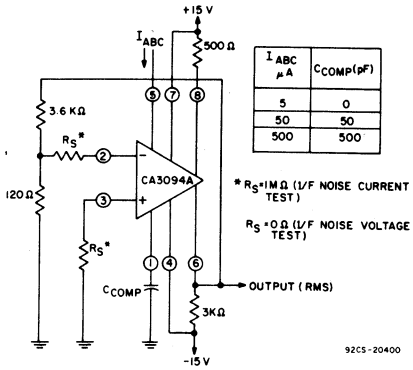
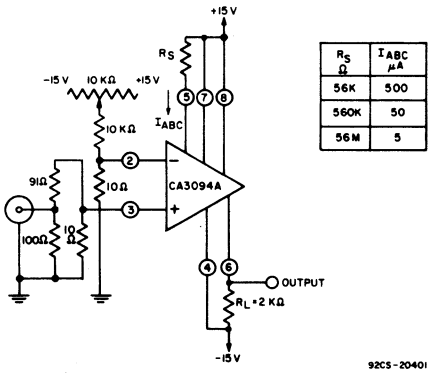


Fig. 20—Common-mode range and rejection ratio test circuit.



IABC μA	CCOMP(pF)
5	0
50	50
500	500

Fig. 21—1/F noise test circuit.



RS Ω	IABC μA
56K	500
560K	50
56M	5

Fig. 22—Open-loop gain vs. frequency test circuit.

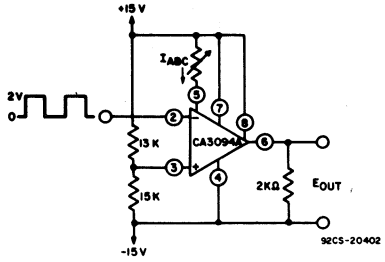


Fig. 23—Open-loop slew rate vs. I_{ABC} test circuit.

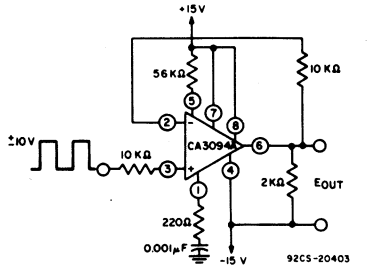
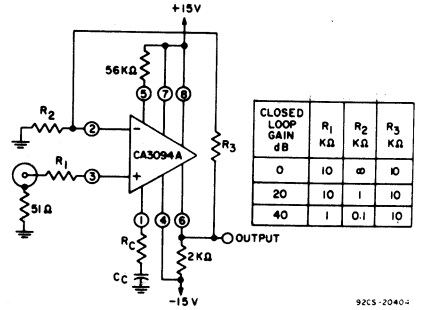


Fig. 24—Slew rate vs. non-inverting unity gain test circuit.



CLOSED LOOP GAIN dB	R1 KΩ	R2 KΩ	R3 KΩ
0	10	∞	10
20	10	1	10
40	1	0.1	10

Fig. 25—Phase compensation test circuit.

CA3095E

Super-Beta Transistor Array

Differential Cascode Amplifier Plus 3 Independent Transistors

RCA-CA3095E is a monolithic array of transistors connected as a super-beta differential cascode amplifier with three independent n-p-n transistors. (Refer to Fig. 1 for following description.)

The differential cascode amplifier incorporates two cascode amplifiers consisting of transistors Q1, Q3 and Q2, Q4, respectively, plus a voltage-limiting circuit, consisting of diodes D1, D2 and p-n-p transistor Q5. Two of these transistors, Q1 and Q2, are super-beta types that have an $h_{FE} > 1000$ and are capable of operating over a wide current range of 1 μA to 2 mA. Each of these types comprises the input section of its respective cascode amplifier. The output section of each cascode amplifier employs a conventional n-p-n transistor, Q3, Q4, respectively. The output signal is obtained at the collectors of these transistors. See Operating Considerations for bias considerations of the differential cascode amplifier.

The exceptionally high-beta characteristics of Q1 and Q2, plus the large signal-voltage swing capability of Q3 and Q4, make the composite differential cascode amplifier an excellent choice for a broad range of small-signal, high-input-impedance amplifier applications including low-noise video amplifiers. This amplifier is also recommended for use in long-interval timers, oscillators, and long-duration one-shot applications.

The independent transistors, Q6, Q7 and Q8, are high-voltage silicon n-p-n conventional types for general use in signal processing systems in the frequency range from dc through vhf. Separate terminals for each of these transistors permit maximum flexibility in circuit design.

The CA3095E is supplied in a 16-lead dual-in-line plastic package and operates over the ambient temperature range of −55°C to +125°C

Features

- Two super-beta n-p-n transistors – $h_{FE} > 1000$
- Voltage-limiting circuitry (D1, D2, Q5)
- Operation possible at I_{IB} down to < 1 nA
- Matched pair (Q1 and Q2) –
  V_{IO} = 5 mV max. at I_C = 100 μA dc
  I_{IO} = 20 nA max. at I_C = 100 μA dc
- Wide current range – < 1 μA to 2 mA

Independent Transistors:

- h_{FE} = 300 typ. for each transistor
- Wide current range – < 1 μA to 10 mA
- Matched general-purpose transistors
- High voltage – V_{CBO} = 45 V max.

Applications

Differential Cascode Amplifier:

- Super-beta pre-amplifier for op-amp
- High-impedance dc meter amplifier
- Low-noise video amplifier
- Piezoelectric transducer amplifier
- Long-interval timer
- Long-duration one-shot multivibrator
- Comparator with high-input impedance
- Long-time-constant integrator
- Photocell amplifier
- Low-noise amplifier–for operation from high-source impedances

Independent Transistors:

- General use in signal processing systems in dc through vhf range

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25 °C*

Power Dissipation:		
Any One Transistor	300	mW
Total Package–		
Up to 25 °C	750	mW
Above 25 °C ..... derate linearly	6.67	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−55 to +150	°C
Lead Temperature (During Soldering):		
At distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265	°C
Voltage and Current Ratings Apply for Each Specified Transistor:		
Super-Beta Transistors (Q1, Q2)–		
Collector-to-Base Voltage (V_{CBO})	6	V
Emitter-to-Base Voltage (V_{EBO})	6	V
Collector-to-Substrate Voltage (V_{CIO})*	45	V
Collector Current (I_C)	50	mA
Base Current (I_B)	20	mA
Conventional N-P-N Transistors (Q3, Q4, Q6, Q7, Q8)–		
Collector-to-Base Voltage (V_{CBO})	45	V
Collector-to-Emitter Voltage (V_{CEO})	35	V
Emitter-to-Base Voltage (V_{EBO})	6	V
Collector-to-Substrate Voltage (V_{CIO})*	45	V
Collector Current (I_C)	50	mA
Base Current (I_B)	20	mA
Conventional P-N-P Transistor (Q5)–		
Collector-to-Base Voltage (V_{CBO})	−45	V
Collector-to-Emitter Voltage (V_{CEO})	−35	V
Limiting Circuit Current ($I_{Pin\ 11}$)	20	mA

* The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either dc or signal (ac) ground. A suitable bypass capacitor can be used to establish a signal ground.

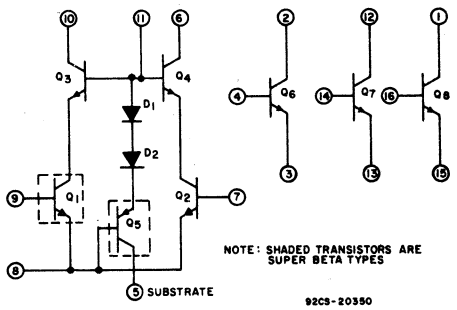


Fig. 1–Functional diagram.

STATIC CHARACTERISTICS

Characteristics	Symbol	Test Conditions (T_A = 25 °C)	Limits Min.	Limits Typ.	Limits Max.	Units
Characteristics Apply for Each Super-Beta Cascode Amplifier Transistor Pair (Q1, Q3) and (Q2, Q4), Unless Indicated Otherwise						
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0 See Note 1	6	–	–	V
Emitter-to-Base Breakdown Voltage (Applies only to Q1 & Q2)	$V_{(BR)EBO}$	I_E = 100 μA, I_C = 0 Term. 9 to 8 or Term. 7 to 8	6	8	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 100 μA, I_B = I_E = 0	45	–	–	V
Collector Cutoff Current	I_{CER}	V_{6-8} or V_{10-8} = 10 V, I_{11} = 100 μA, R_{BE} = 100 MΩ	–	–	100	nA
DC Forward-Current Transfer Ratio	h_{FE}	V_{10-8} = 5 V or V_{6-8} = 5 V; I_C = 1 mA	–	1500	–	
		I_C = 100 μA	1000	2000	5000	
		I_C = 10 μA	–	1500	–	
Base-to-Emitter Voltage (Applies only to Q1 & Q2)	V_{BE}	I_C = 100 μA, V_{6-8} or V_{10-8} = 5 V	0.50	0.59	0.68	V
Saturation Voltage	V_{sat}	I_6 or I_{10} = 1 mA, I_{11} = 100 μA, I_7 or I_9 = 100 μA	–	0.22	0.7	V
For Cascode Amplifiers as a Differential Matched Pair						
Magnitude of Input-Offset Voltage	$\lvert I_{IO}\rvert$	I_C = 100 μA, V_{6-8} = V_{10-8} = 5 V	–	1	5	mV
Magnitude of Input-Offset Current	$\lvert I_{IO}\rvert$		–	4	20	nA
Magnitude of Input-Offset Voltage Drift (Temp. Coeff.)	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$		–	3.3	–	μV/°C
Magnitude of Input-Offset Current Drift (Temp. Coeff.)	$\frac{\lvert\Delta I_{IO}\rvert}{\Delta T}$		–	0.05	–	nA/°C

Note 1: Terminal No. 9 to terminals 10 and 11 connected or terminal No. 7 to terminals 6 and 11 connected.

Test Circuits for Measurement of Super-Beta Cascode Amplifier Characteristics

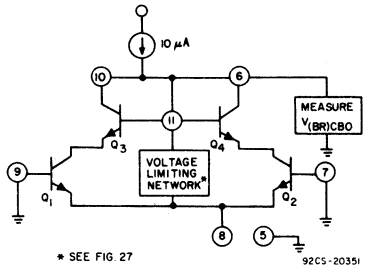


Fig. 2–$V_{(BR)CBO}$ test circuit.

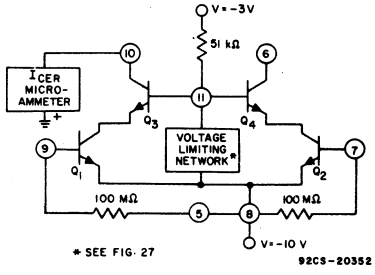


Fig. 3–I_{CER} test circuit

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STATIC CHARACTERISTICS (Cont'd)

Characteristics	Symbol	Test Conditions T_A = 25 °C		Limits Min.	Typ.	Max.	Units
For Each Conventional n-p-n Transistor (Q3, Q4, Q6, Q7, Q8)							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0		45	95	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0		35	50	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 100 μA, I_C = 0		6	8	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 100 μA, I_B = I_E = 0		45	95	–	V
Collector Cutoff Current	I_{CEO}	V_{CE} = 10 V, I_B = 0		–	–	100	nA
Collector Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0		–	–	10	nA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 5 V	I_C = 10 mA	–	210	–	
			I_C = 1 mA	150	300	500	
			I_C = 10 μA	–	180	–	
Base-to-Emitter Voltage	V_{BE}	I_C = 1 mA, V_{CE} = 5 V		0.60	0.69	0.78	V
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 10 mA, I_B = 1 mA		–	0.22	0.7	V

Dynamic Characteristics

Characteristics	Symbol	Test Conditions T_A = 25 °C	Limits Min.	Typ.	Max.	Units
Characteristics Apply for Each Super-Beta Cascode Amplifier Transistor Pair (Q1, Q3), Unless Indicated Otherwise						
Gain-Bandwidth Product	f_T	I_C = 100 μA, V_{6-8} = V_{10-8} = 5 V, *	–	78	–	MHz
Noise Voltage (Referred to Input) For Differential Amplifier Operation	E_N	I_C = 50 μA, f = 10 Hz	–	13	–	nV/$\sqrt{Hz}$
Noise Current (Referred to Input) For Differential Amplifier Operation	I_N	I_C = 5 μA, f = 10 Hz	–	0.12	–	pA/$\sqrt{Hz}$
Collector-to-Base Capacitance	C_{CB}	V_{6-7} = V_{10-9} = 5 V, I_E = 0	–	0.3		pF
Collector-to-Substrate Capacitance	C_{CIO}	V_{6-5} = V_{10-5} = 5 V, I_B = 0	–	3.0	–	pF
For Each Conventional Transistor (Q3 through Q8)						
Gain-Bandwidth Product	f_T	I_C = 100 μA, V_{CE} = 5 V	–	100	–	MHz
		I_C = 3 mA, V_{CE} = 5 V	–	320	–	
Noise Voltage (Referred to Input)	E_N	I_C = 100 μA, V_{CE} = 5 V, f = 10 Hz	–	5	–	nV/$\sqrt{Hz}$
Noise Current (Referred to Input)	I_N	I_C = 10 μA, V_{CE} = 5 V, f = 10 Hz	–	0.8	–	pA/$\sqrt{Hz}$
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 5 V, I_E = 0	–	0.4	–	pF
Collector-to-Substrate Capacitance	C_{CIO}	V_{CI} = 5 V, I_B = 0	–	2	–	pF

* Curve plotted for I_{CEO} characteristic.

Test Circuits for Measurement of Super-Beta Cascode Amplifier Characteristics

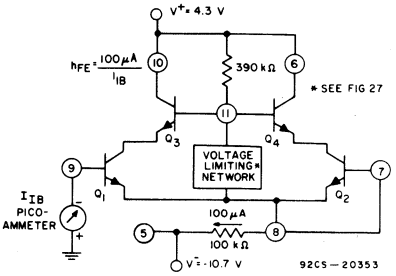

Fig.4—DC Beta (h_{FE}) test circuit.

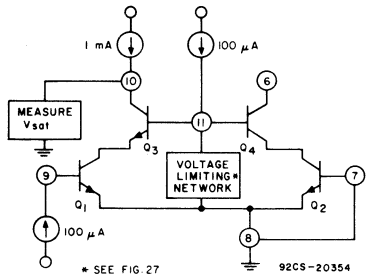

Fig.5—V_{sat} test circuit for super-beta cascode pairs.

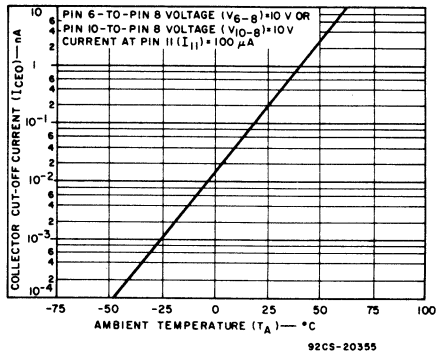

Fig.6—Collector cut-off current vs ambient temperature for super-beta cascode pairs.

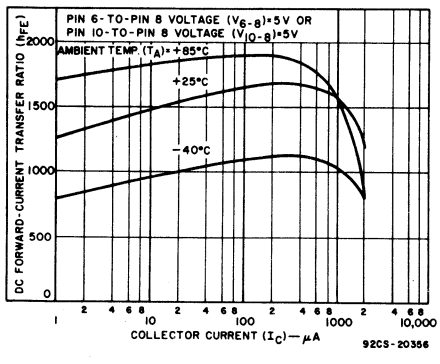

Fig.7—h_{FE} vs. I_C for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

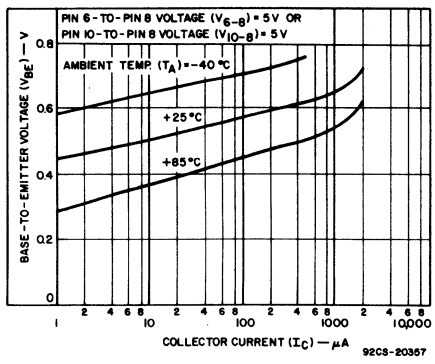

Fig.8—V_{BE} vs. I_C for each super-beta transistor (Q1 and Q2).

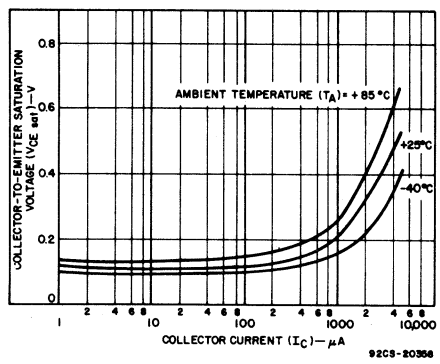

Fig.9—$V_{CE(sat)}$ vs. I_C for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

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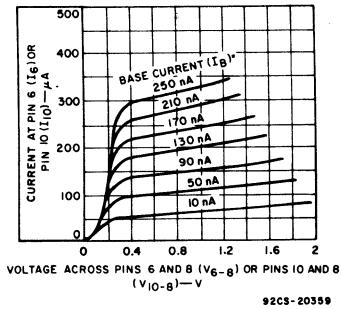

Fig.10—I-V characteristics for the super-beta cascode pairs.

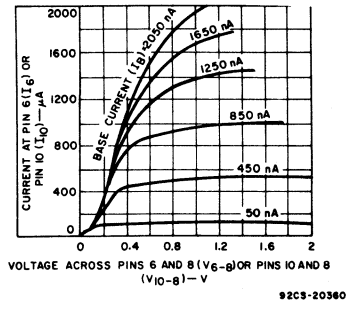

Fig.11—I-V characteristics for the super-beta cascode pairs.

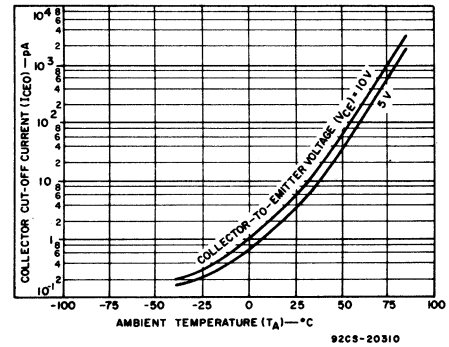

Fig.12—Collector cutoff current vs ambient temperature for the conventional transistors (V_{CE} = 5 V, 10 V).

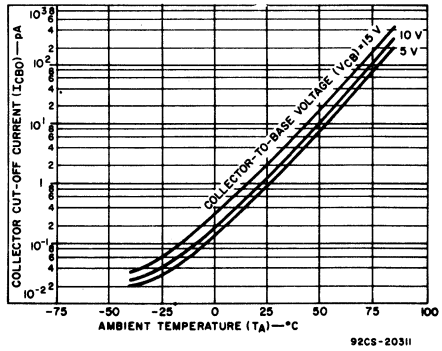

Fig.13—Collector cutoff current vs ambient temperature for the conventional transistors (V_{CB} = 5 V, 10 V, 15 V).

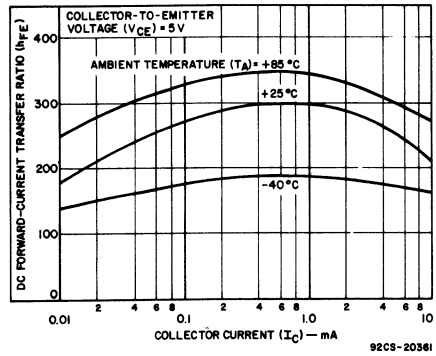

Fig.14—h_{FE} vs. I_C for each conventional transistor (Q6, Q7, Q8).

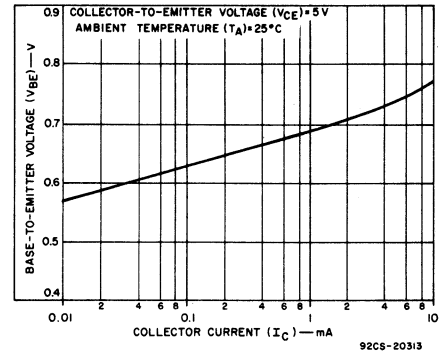

Fig.15—V_{BE} as a function of collector current for the conventional transistors.

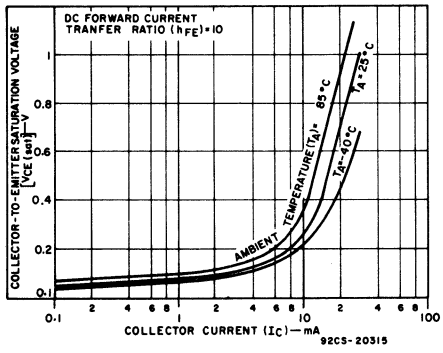

Fig.16—$V_{CE(sat)}$ as a function of collector current for the conventional transistors.

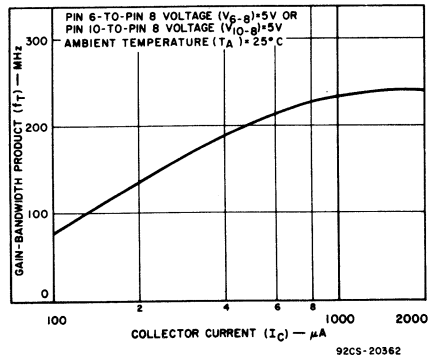

Fig.17—Gain bandwidth product vs collector current for the super-beta cascode pairs.

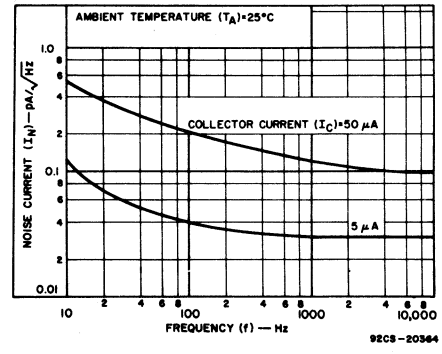

Fig.18—I_N vs. f for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

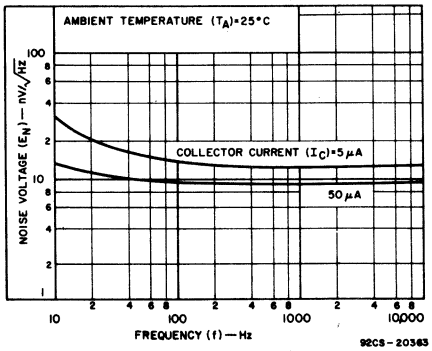

Fig.19—E_N vs. f for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

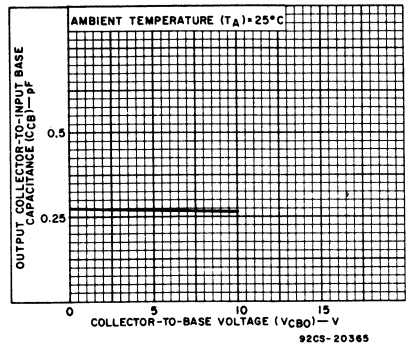

Fig.20—C_{CB} vs. V_{CBO} for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

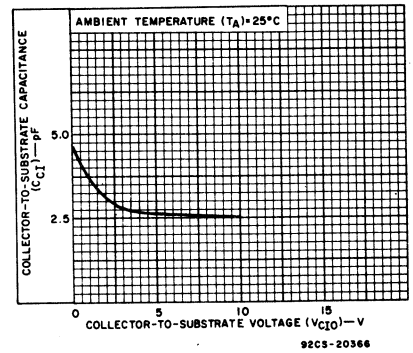

Fig.21—C_{CI} vs. V_{CIO} for each super-beta cascode amplifier transistor pair (Q1, Q3) and (Q2, Q4).

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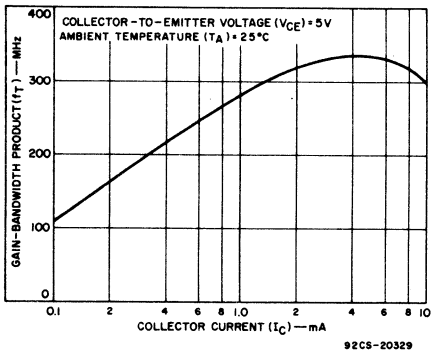

Fig.22—Gain bandwidth product vs collector current for the conventional transistors.

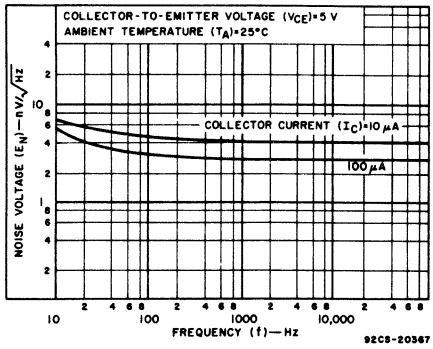

Fig.23—Noise voltage vs frequency for the conventional transistors.

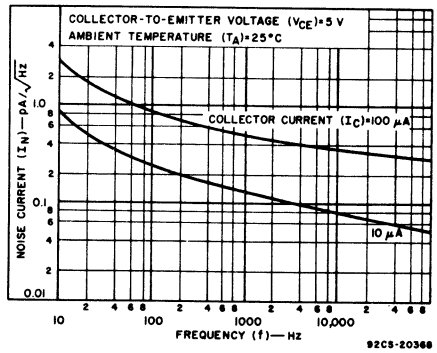

Fig.24—I_N vs. f for each conventional transistor (Q6, Q7, Q8).

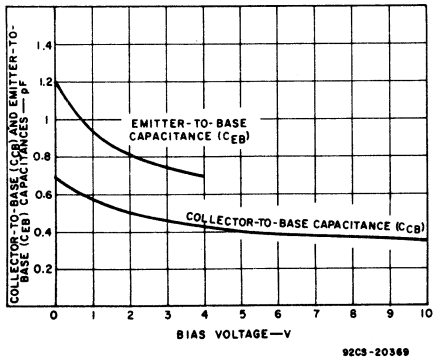

Fig.25—Collector-to-base and emitter-to-base capacitances vs bias voltage for the conventional transistors.

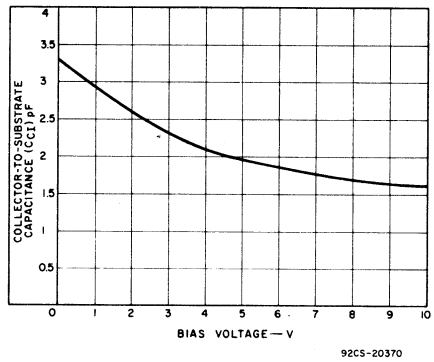

Fig.26—Collector-to-substrate capacitance vs bias voltage for the conventional transistors.

TYPICAL APPLICATIONS

Operating Considerations

Operation Considerations for the Super-Beta Differential Cascode Amplifier

An internal voltage-limiting network (diodes D1, D2 and p-n-p transistor Q5) incorporated in the differential cascode amplifier, assures that the applied collector-to-emitter voltage of each super-beta unit is maintained below two volts. Fig. 27 shows a typical bias arrangement of the super-beta differential cascode amplifier.

Bias current for this network must be supplied by an external source. This bias current can be obtained by simply connecting a resistor from Pin 11 to the positive supply of the differential amplifier. The return path for most of the bias current is through the substrate, Pin 5, rather than through the common emitter, Pin 8. This arrangement provides superior common-mode and power-supply rejection. As a general rule-of-thumb, the current supplied into Pin 11 should be approximately 0.04 to 0.1 times the value of the quiescent current of Pin 8.

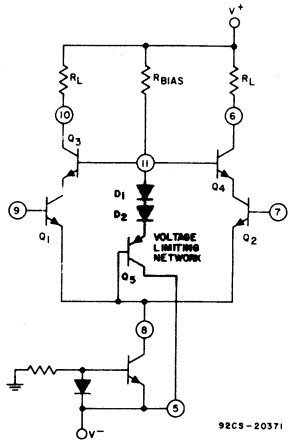

Fig.27—Bias arrangement for operation of the super-beta differential cascode amplifier.

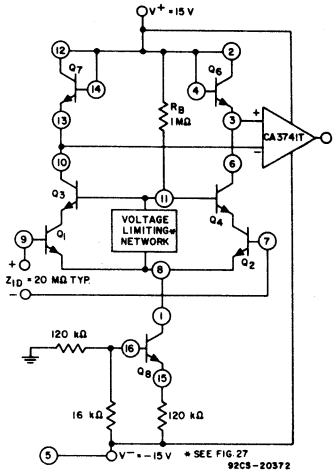

Fig.28—Super-beta Op-Amp with diode drive network.

CA3095E

TYPICAL APPLICATIONS (Cont'd)

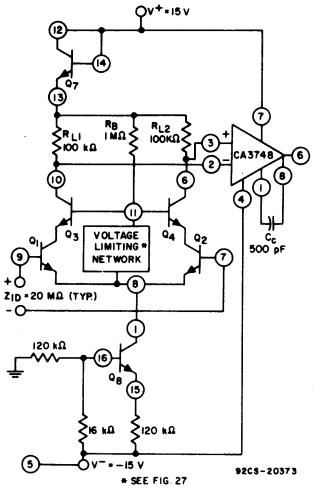

Fig.29—Super-beta Op-Amp with resistor drive network.

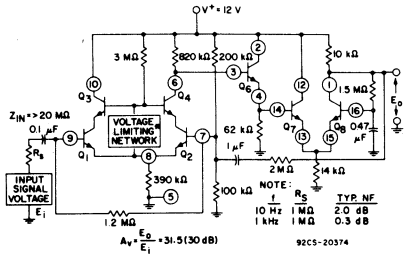

Fig.30—High-input-impedance, low-noise amplifier circuit.

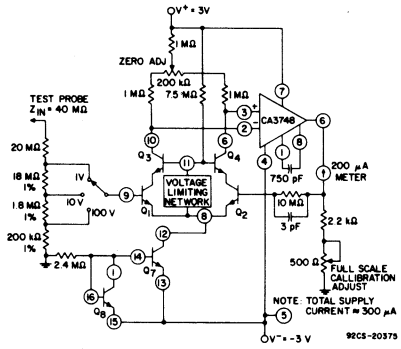

Fig.31—Typical high-input-impedance dc voltmeter circuit.

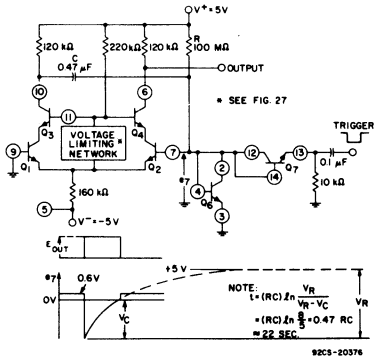

Fig.32—Long-delay monostable multivibrator circuit.

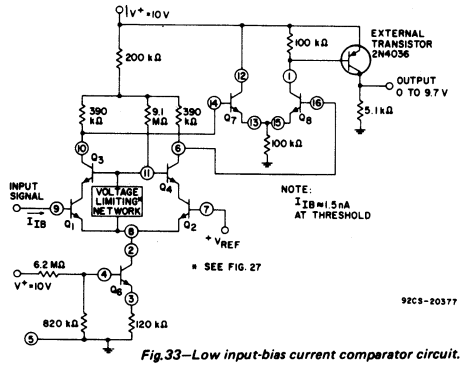

Fig.33—Low input-bias current comparator circuit.

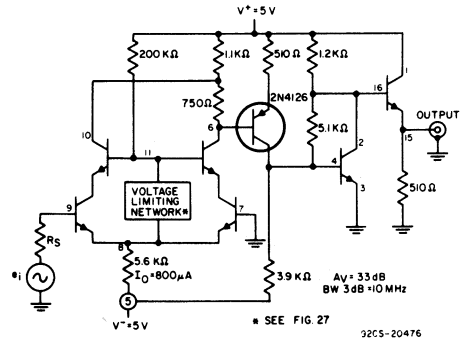

Fig.34—CA3095E wideband amplifier.

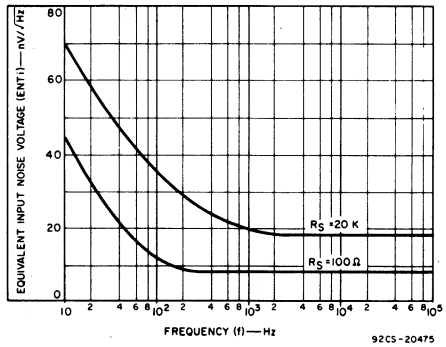

Fig.35—Equivalent input noise voltage vs. frequency for circuit of figure 34.