CA3098 Types

Programmable Schmitt Trigger

– With Memory

—Dual-Input Precision Level Detectors

Applications:

- Control of relays, heaters, LED's lamps, photo-sensitive devices, thyristors, solenoids, etc.
- Signal reconditioning
- Phase and frequency modulators
- On/off motor switching
- Schmitt triggers, level detectors
- Time delays
- Overvoltage, overcurrent, overtemperature protection
- Battery-operated equipment
- Square and triangular-wave generators

Features:

- Programmable operating current
- Micropower standby dissipation
- Direct control of currents up to 150 mA
- Low input on/off current of less than 1 nA for programmable bias current of 1 μA
- Built-in hysteresis: 20 mV max.
- Programmable hysteresis: 20 mV to V+
- Dual reference input
- High sensor range: 100 Ω to 100 MΩ
- Stable predictable switching levels
- Temperature-compensated reference voltage
- Power can be strobed off via term. 2

The RCA-CA3098 Programmable Schmitt Trigger is a monolithic silicon integrated circuit designed to control high-operating-current loads such as thyristors, lamps, relays, etc. The CA3098 can be operated with either a single power supply with maximum operating voltage of 16 volts, or a dual power supply with maximum operating voltage of ±8 volts. It can directly control currents up to 150 mA and operates with microwatt standby power dissipation when the current to be controlled is less than 30 mA. The CA3098 contains the following major circuit-function features (see Fig. 1):

1. Differential amplifiers and summer: the circuit uses two differential amplifiers, one to compare the input voltage with the "high" reference, and the other to compare the input with the "low" reference. The resultant output of the differential amplifiers actuates a summer circuit which delivers a trigger that initiates a change in state of a flip-flop.
2. Flip-flop: the flip-flop functions as a bistable "memory" element that changes state in response to each trigger command.
3. Driver and otuput stages: these stages permit the circuit to "sink" maximum peak load currents up to 150 mA at terminal 3.
4. Programmable operating current: the circuit incorporates access at terminal 2 to permit programming the desired quiescent operating current and performance parameters.

The CA3098 is supplied in the 8-lead dual-in-line plastic package ("Mini-Dip", E suffix), 8-lead TO-5 style package (T suffix), 8-lead TO-5-style package with formed leads "DIL-CAN" (S suffix), and in chip form (H suffix).

For information on another RCA Dual-Input Precision Level Detector, see the data bulletin for the RCA-CA3099E, File No. 620.

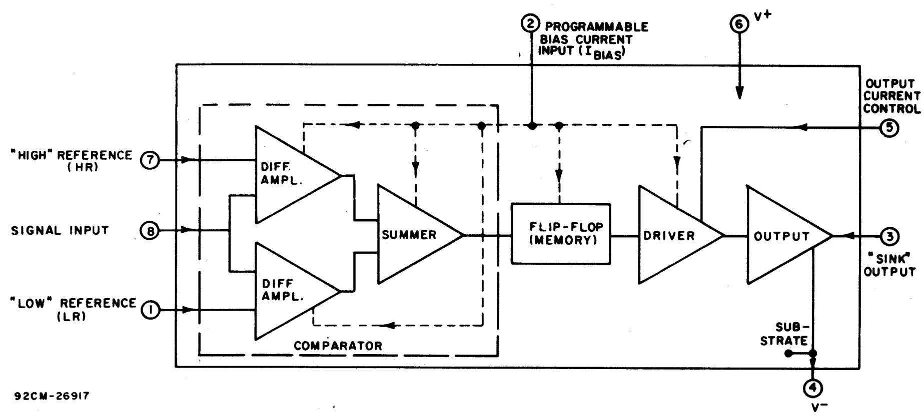


Fig. 1 – Block diagram of CA3098 programmable Schmitt trigger.

Maximum Ratings, *Absolute-Maximum Values at T_A = 25°C:*

Supply Voltage Between Terminals 6 and 4	16	V
Output Voltage Between Terminals 7 and 4, and 3 and 4	16	V
Differential Input Voltage Between Terminals 8 and 1, and Terminals 7 and 8	10	V
Operating Voltage Range:		
Term. 8	V− to V+	
Term. 7	(V− plus 2.0 V) to V+	
Term. 1	(V−) to (V+ minus 2.0 V)	
Load Current (Term. 3)	150	mA
Input Current to Voltage Regulator (Term. 5)	25	mA
Programmable Bias Current (Term. 2)	1	mA
Output Current Control (Term. 5)	15	mA
Power Dissipation:		
Without Heat Sink:		
Up to T_A = 55°C		
CA3098S, CA3098T	630	mW
CA3098E	630	mW
Above T_A = 55°C Derate linearly at	6.67	mW/°C
With Heat Sink:		
Up to T_A = 55°C		
CA3098S, CA3098T	1.6	W
Above T_A = 55°C		
CA3098S, CA3098T Derate linearly at	16.67	mW/°C
Ambient Temperature Range (All Packages):		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	265	°C

CA3098 Types

General Description of Circuit Operation (Refer to Figs. 2, 3, 4)

When the signal-input voltage of the CA3098 is equal to or less than the "low" reference voltage (LR), current flows from an external power supply through a load connected to terminal 3 ("sink" output). This condition is maintained until the signal-input voltage rises to or exceeds the "high" reference voltage (HR), thereby effecting a change in the state of the flip-flop (memory) such that the output stage interrupts current flow in the external load. This condition, in turn, is maintained until such time as the signal again becomes equal to or less than the "low" reference voltage (VR).

The CA3098 comparator is unique in that it contains circuit provisions to permit programmability. This feature provides flexibility to the designer to optimize quiescent power consumption, input-circuit characteristics, hysteresis, and additionally permits independent control of the comparator, namely, pulsing, strobing, keying, squelching, etc. Programmability is accomplished by means of the bias current (I_{bias}) supplied to terminal 2.

An auxiliary means of controlling the magnitude of load-current flow at terminal 3 is provided by "sinking" current into terminal 5. Figs. 3 and 4 highlight the operation of the CA3098 when connected as a simple hysteresis switch (Schmitt trigger).

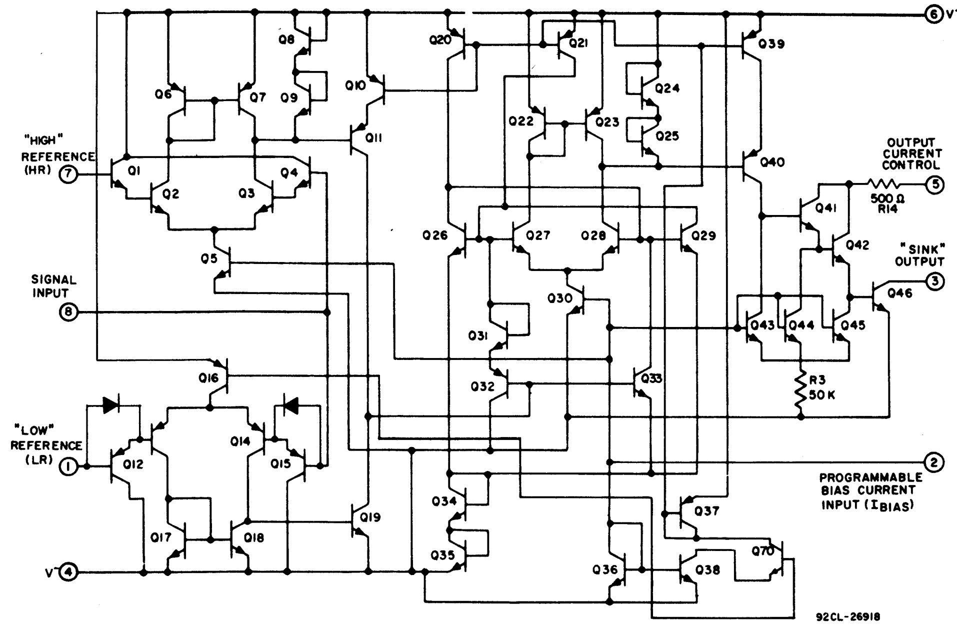


Fig. 2 – Schematic Diagram of CA3098.

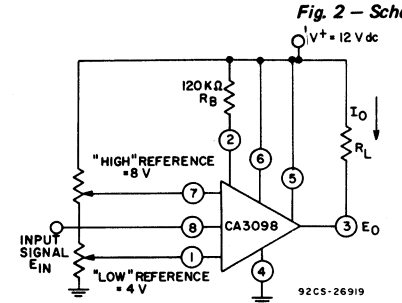


Fig. 3 – Basic hysteresis switch (Schmitt trigger).

Sequence	Input Signal Level	Output Voltage (V) (Term. 3)
1	$4 \geq E_{IN} > 0$	0
2	$8 \geq E_{IN} > 4$	0
3	$E_{IN} > 8$	12
2	$8 \geq E_{IN} > 4$	12
1	$4 \geq E_{IN} > 0$	0

Fig. 4 – Resultant output states of the CA3098, shown in Fig. 3 as a function of various input signal levels.

TYPICAL CHARACTERISTIC CURVES

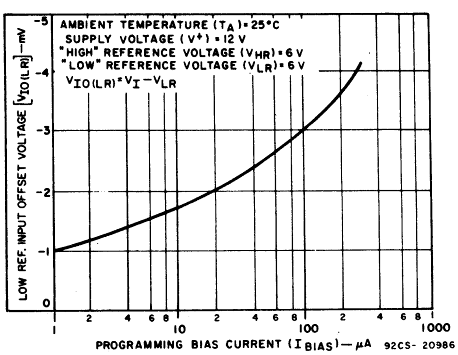


Fig. 5 – Input-offset voltage ("low" reference) vs. programming bias current.

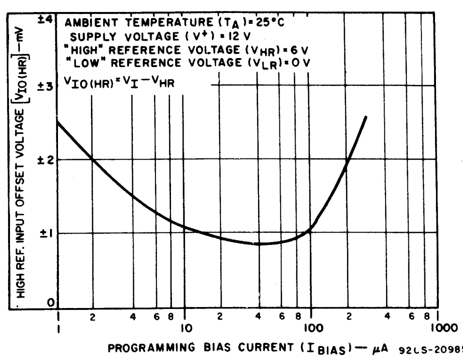


Fig. 6 – Input-offset voltage ("high" reference) vs. programming bias current.

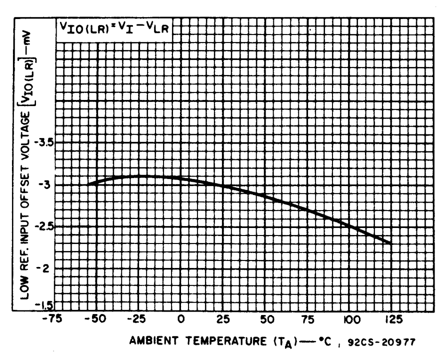


Fig. 7 – Input-offset voltage ("low reference) vs. ambient temperature.

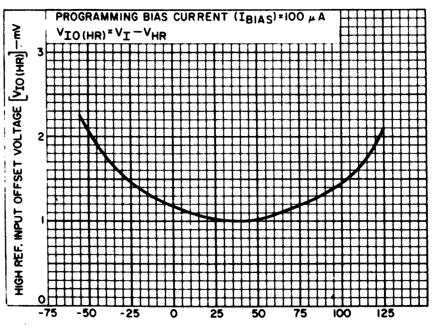


Fig. 8 – Input-offset voltage ("high reference) vs. ambient temperature.

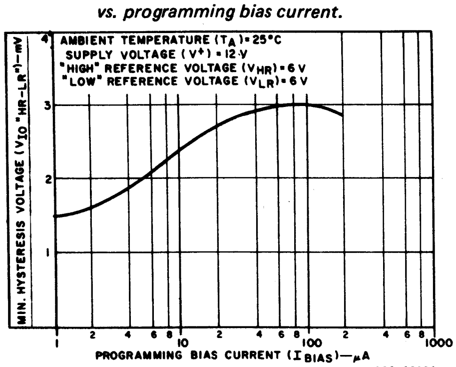


Fig. 9 – Min. hysteresis voltage vs. programming bias current.

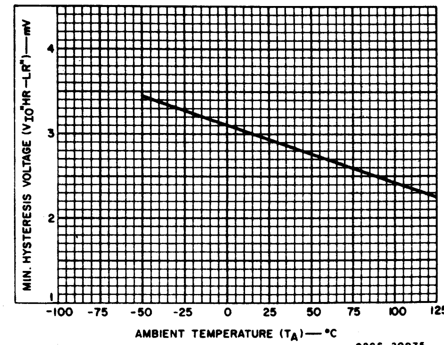


Fig. 10 – Min. hysteresis voltage vs. ambient temperature.

CA3098 Types

ELECTRICAL CHARACTERISTICS at T_A = 25°C Unless Otherwise Specified

CHARACTERISTIC	TEST CONDITIONS	Fig. No.	LIMITS Min.	Typ.	Max.	UNITS
Input Offset Voltage: "Low" Ref., $V_{IO(LR)}$	V_{LR} = Gnd, V_{HR} = 3 V, I_{BIAS} = 100 μA	5	−15	−3	6	mV
"High" Ref., $V_{IO(HR)}$	V_{HR} = Gnd, V_{LR} = −3 V, I_{BIAS} = 100 μA	6	−10	±10	10	
Temp. Coeff: "Low" Ref.	−55 °C to + 125 °C	7	–	4.5	–	μV/°C
"High" Ref.	−55 °C to + 125 °C	8	–	±8.2	–	
Min. Hysteresis Voltage $V_{IO(HR-LR)}$:	V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	9	–	3	20	mV
Temp. Coeff.	−55°C to + 125 °C	10	–	6.7	–	μV/°C
Output Saturation Voltage, $V_{CE}(SAT)$	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	11,12	–	0.72	1.2	V
Total Supply Current, I_{TOTAL}: "ON"	V_I = 4 V, V_{REG} = 6 V; V^+ = 12 V, I_{BIAS} = 100 μA	13,14	500	710	800	μA
"OFF"	V_I = 8 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA		400	560	750	μA
Input Bias Current, I_{IB}: $I_{B(p-n-p)}$	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	15	–	42	100	nA
$I_{B(n-p-n)}$	V_I = 8 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA		–	28	100	nA
Output Leakage Current, $I_{CE(OFF)}$	Current from Term. 3 when Q46 is "OFF"	–	–	–	10	μA
Switching Times: Delay, t_d	I_C = 100 μA	18	–	600	–	ns
Fall, t_f	I_{BIAS} = 100 μA		–	50	–	ns
Rise, t_r	V^+ = 5 V		–	500	–	ns
Storage, t_s	V_{REG} = 2.5 V		–	4.5	–	μs
Output Current, I_O	V^+ = 12 V, I_{BIAS} = 50 μA	–	100	–	–	mA

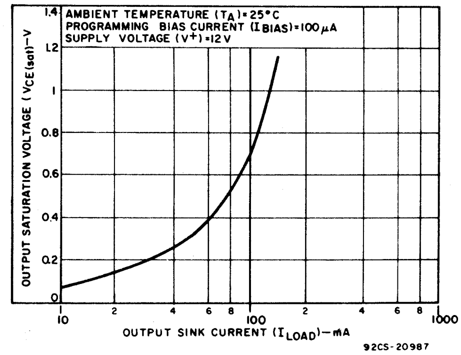


Fig. 11 — Output saturation voltage vs. output sink current.

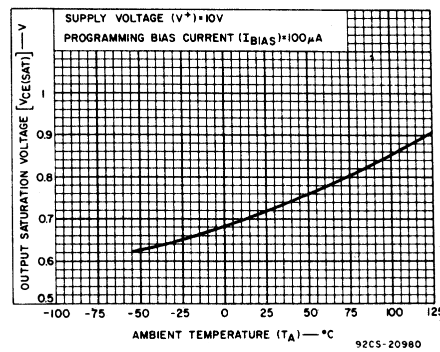


Fig. 12 — Output saturation voltage vs. ambient temperature.

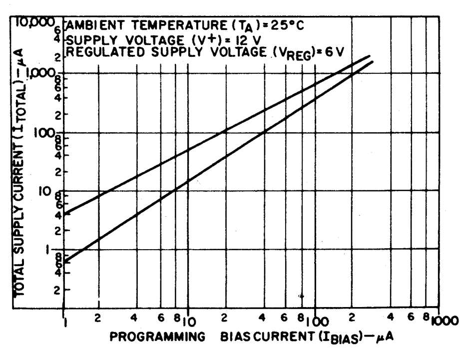


Fig. 13 — Total supply current vs. programming bias current.

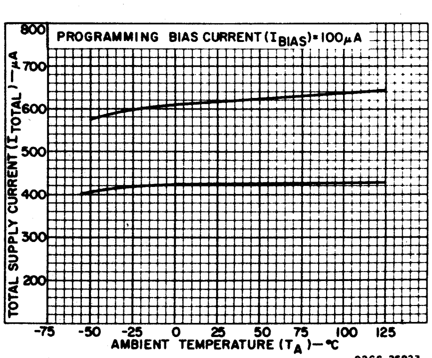


Fig. 14 — Total supply current vs. ambient temperature.

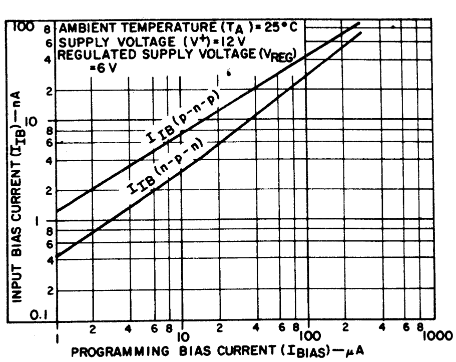


Fig. 15 — Input bias current vs. programming bias current.

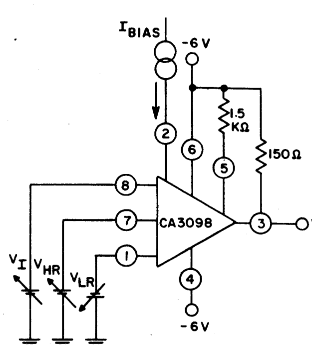


Fig. 16 — Input-offset voltage test circuit.

CA3098 Types

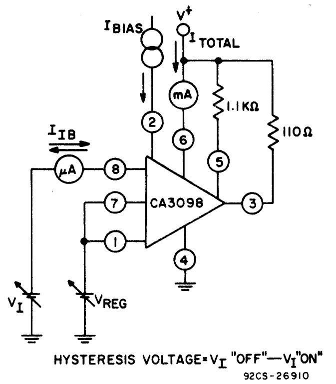


Fig. 17 – Min. hysteresis voltage, total supply current, and input-bias-current test circuit.

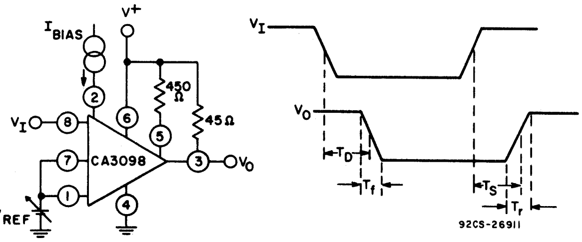


Fig. 18 – Switching time test circuit.

TYPICAL APPLICATIONS

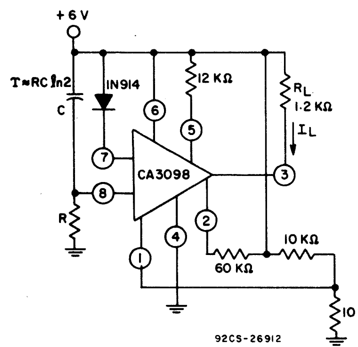


Fig. 19 – Time delay circuit: Terminal 3 "sinks" after τ seconds.

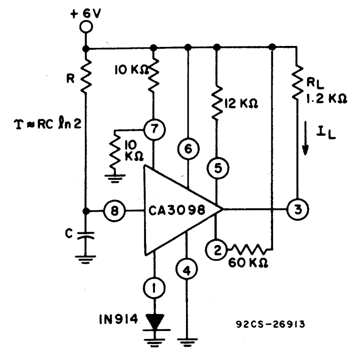


Fig. 20 – Time delay circuit: "sink" current interrupted after T seconds.

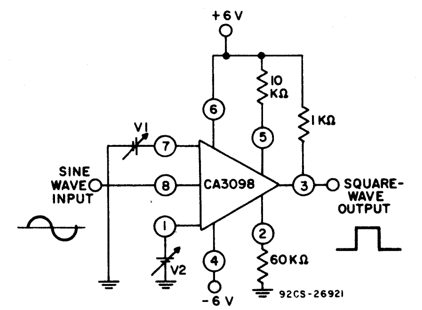
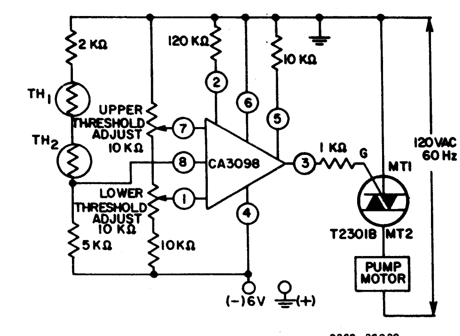


Fig. 21 – Sine-wave to square-wave converter with duty-cycle adjustment (V_1 and V_2).



Notes (a) Motor pump is "ON" when water level rises above thermistor TH_2.

(b) Motor pump remains "ON" until water level falls below thermistor TH_1.

(c) Thermistors, operate in self-heating mode.

Fig. 22(a) – Water-level control.

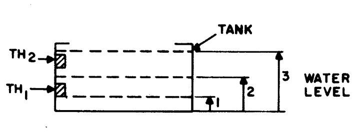


Fig. 22(b) – Water level diagram for circuit of Fig. 22(a).

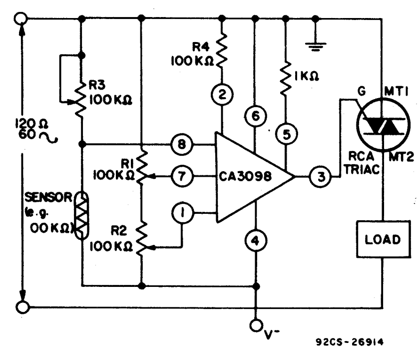
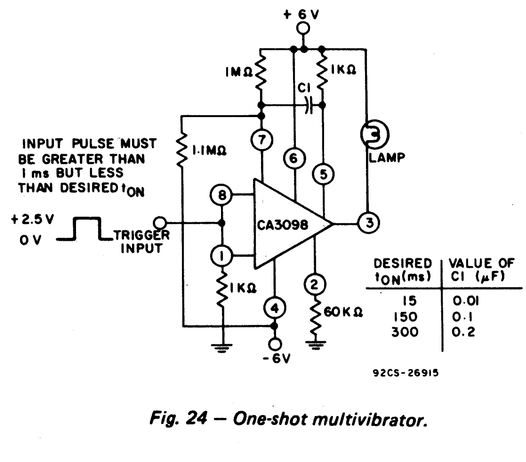


Fig. 23 – OFF/ON control of triac with programmable hysteresis.



DESIRED t_{ON}(ms)	VALUE OF C1 (μF)
15	0.01
150	0.1
300	0.2

Fig. 24 – One-shot multivibrator.

CA3099E

Programmable Comparator . . With Memory

RCA-CA3099E Programmable Comparator is a monolithic silicon integrated circuit designed to control high-operating-current loads such as thyristors, lamps, relays, etc. The CA3099E can be operated with either a single power supply with maximum operating voltage of 16 volts, or a dual power supply with a maximum operating voltage of ± 8 volts. It can directly control currents up to 150 mA. It operates with microwatt standby power dissipation when the current to be controlled is less than 30 mA. The CA3099E contains the following six (6) major circuit-function features (Figure 1):

1. **Differential amplifiers and summer;** the circuit uses two differential amplifiers, one to compare the input voltage with the "high" reference, and the other to compare the input with the "low" reference. The resultant output of the differential amplifiers actuates a summer circuit which delivers a trigger that initiates a change in state of a flip-flop.
2. **Flip-flop;** the flip-flop functions as a bistable "memory" element that changes state in response to each trigger command.
3. **Driver and output stages;** these stages permit the circuit to "sink" maximum peak load currents up to 150 mA at terminal 3.
4. **Programmable operating current;** the circuit incorporates a separate terminal to permit programming the desired quiescent operating current and performance parameters.
5. **Internal sources of reference voltage and programmable bias current;** an integral circuit supplies a temperature-compensated reference voltage ($V_b/2$) which is about 1/2 of the externally applied bias voltage (V_b). Additionally, integral circuitry can optionally be used to supply an uncompensated constant-current source of bias (I_{bias}).
6. **Voltage regulator;** provides optional on-chip voltage regulation when power for the CA3099E is provided by an unregulated supply.

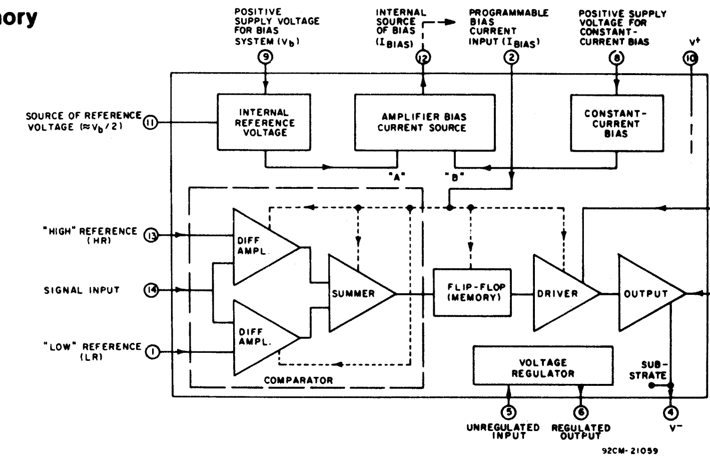


Fig.1—Block diagram of CA3099E programmable comparator. (See page 3 for general description of circuit operation.)

Features:

- Programmable operating current
- Micro-power standby dissipation
- Directly controls current up to 150 mA
- Low input on/off current of less than 1 nA for programmable bias current of 1 µA
- Built-in hysteresis: 10 mV max.
- Programmable hysteresis: 10 mV to V+
- Dual reference input
- High sensor range: 100 Ω to 100 MΩ
- Stable predictable switching levels
- Temperature-compensated reference voltage

Applications:

- Control of relays, heaters, LED's, lamps, photo-sensitive devices, thyristors, solenoids, etc.
- Signal reconditioning
- Phase and frequency modulators
- On/off motor switching
- Schmitt triggers, level detectors
- Time delays
- Overvoltage, overcurrent, overtemperature protection
- Battery-operated equipment
- Square and triangular-wave generators

Maximum Ratings, ***Absolute-Maximum Values at T_A = 25°C:***

Supply Voltage Between Terminals 10 and 4, 9 and 4, 8 and 4	16	V
Output Voltage Between Terminals 7 and 4, and 3 and 4	16	V
Differential Input Voltage Between Terminals 14 and 1, and Terminals 13 and 14	10	V
Operating Voltage Range:		
Term. 14	0 V to V+	
Term. 13	2.0 V to V+	
Term. 1	0 V to V+ minus 2.0 V	
Load Current (Term. 3)	150	mA
Input Current to Voltage Regulator (Term. 5)	25	mA
Programming Bias Current (Term. 2)	1	mA
Output Current Control (Term. 7)	15	mA
Power Dissipation:		
Up to T_A = 55°C	750	mW
Above T_A = 55°C . . . . Derate Linearly at	6.67	mW/°C
Ambient Temperature Range:		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering): At distance not less than 1/32 inch (0.79 mm) from seating plane for 10 s maximum	+265	°C

ELECTRICAL CHARACTERISTICS AT T_A = 25°C *(Unless otherwise indicated)*

CHARACTERISTICS	SYMBOL	TEST CONDITIONS T_A = 25°C Unless Otherwise Indicated	FIG. No.	LIMITS MIN.	TYP.	MAX.	UNIT
Reference Voltage	V_{REF}	Term. 9 = 12 V, Term.4 = Grd, Term.11 = Test	–	5.7	6	6.3	V
Reference Voltage Temperature Coefficient			–	–	100	–	µV/°C
Regulated Supply Voltage	V_{REG}	Term.5 1K to 12V, Term.4 = Grd, Term.6 10K to Grd	5	6	7.2	8	V
Regulated Supply Voltage Temperature Coefficient			5	–	2.9	–	mV/°C
Input Offset Voltage: "Low" Reference	V_{IO} (LR)	V_{LR} = Grd, V_{HR} = 3 V, I_{BIAS} = 100 µA	20, 6	−8	−3	2	mV
"High" Reference	V_{IO} (HR)	V_{HR} = Grd, V_{LR} = −3 V, I_{BIAS} = 100 µA	20, 7	−5	±1	5	
"Low" Reference Temp. Coefficient		−55°C to +125°C	20, 8	–	4.5	20	µV/°C
"High" Reference Temp. Coefficient		−55°C to +125°C	20, 9	–	±8.2	±20	
Min. Hysteresis Voltage	$V_{IO(HR-LR)}$	V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 µA	21, 10	–	3	10	mV
Min. Hysteresis Voltage Temperature Coefficient		−55°C to +125°C	11	–	6.7	20	µV/°C
Output Saturation Voltage	V_{CE}(SAT)	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 µA	21,12,13	–	0.72	1.2	V
Total Supply Current: I_{TOTAL} "ON"	I_{TOTAL}	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 µA	21,14,15	600	710	800	µA
I_{TOTAL} "OFF"		V_I = 8 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 µA	21,14,15	420	560	750	
Input Bias Current: $I_{B(p\text{-}n\text{-}p)}$	I_{IB}	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 µA	21,16,17	–	33	200	nA
$I_{B(n\text{-}p\text{-}n)}$		V_I = 8 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 µA	21,16,17	–	20	60	
Output Leakage Current	$I_{CE(OFF)}$	Current from Term.3 when Q46 is "OFF"	–	–	–	10	µA
Internal Bias Current	I_{IBC}		18,19	120	200	280	
Switching Times: Delay	t_d	I_C = 100 µA, I_{BIAS} = 100 µA, V^+ = 5 V, V_{REG} = 2.5 V	22	–	600	–	ns
Fall	t_f		22	–	50	–	
Rise	t_r		22	–	500	–	
Storage	t_s		22	–	4.5	–	µS

CA3099E

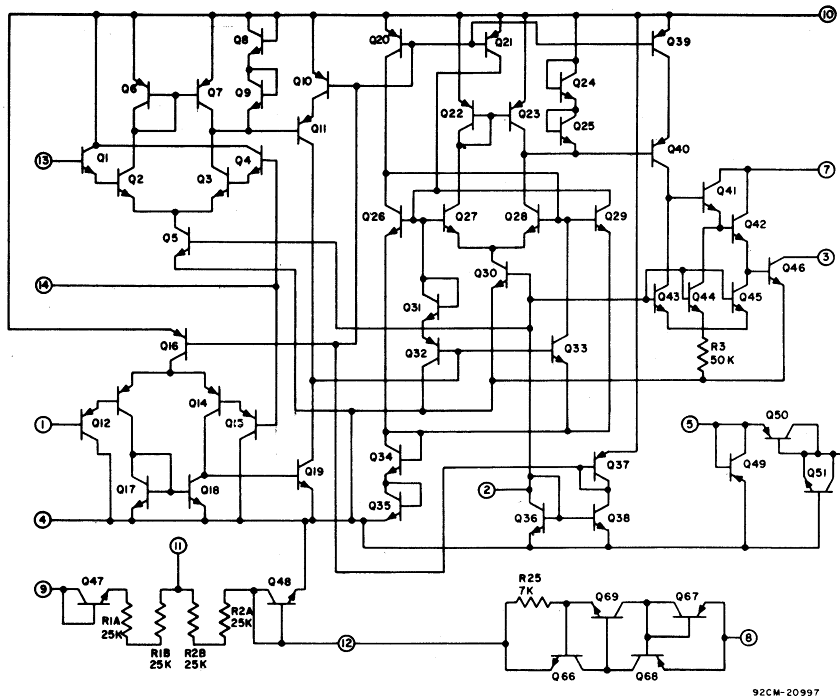


Fig.2—Schematic diagram of CA3099E.

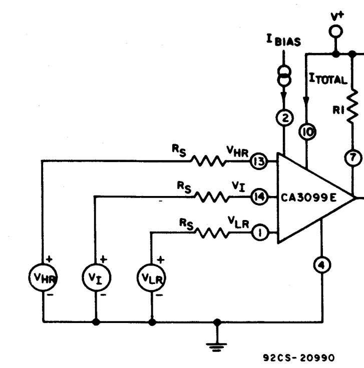


Fig. 3 – Functional diagram.

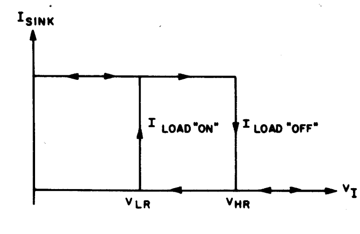


Fig. 4 – Logic diagram.

General Description of Circuit Operation (Refer to Fig.1)

When the signal-input voltage of the CA3099E is equal to or less than the "low" reference voltage (LR), current flows from an external power supply through a load connected to terminal 3 ("sink" output). This condition is maintained until the signal-input voltage rises to or exceeds the "high" reference voltage (HR), thereby effecting a change in the state of the flip-flop (memory) such that the output stage interrupts current flow in the external load. This condition, in turn, is maintained until such time as the signal again becomes equal to or less than the "low" reference voltage (VR).

The CA3099E comparator is unique in that it contains circuit provisions to permit programmability. This feature provides flexibility to the designer to optimize quiescent power consumption, input-circuit characteristics, hysteresis, and additionally permits independent control of the comparator, namely, pulsing, strobing, keying, squelching, etc. Programmability is accomplished by means of the bias current (I_{bias}) supplied to terminal 2. As an alternative to externally supplied bias current, the CA3099E contains an internal source of regulated bias current accessible at terminal 12. This internal source of bias current is developed by two alternative methods; in the first method, bias voltage (V_b) applied at terminal 9 develops a source of temperature-compensated reference voltage ($\approx V_b/2$) at terminal 11 and additionally supplies a source of bias current at terminal 12 via line "A". Alternately, when a positive supply voltage is applied at terminal 8, a source of constant-current biasing is provided at terminal 12 via line "B".

An auxiliary means of controlling the magnitude of load-current flow at terminal 3 is provided by "sinking" current into terminal 7. The CA3099E contains an on-chip voltage regulator which may optionally be used to regulate the voltages and bias currents (exclusive of the load current at terminal 3) needed for the operation of the IC.

Fig. 2 is the schematic diagram of the CA3099E. Figs. 3 and 4 are, respectively, functional and logic diagrams of CA3099E operation.

TYPICAL CHARACTERISTIC CURVES

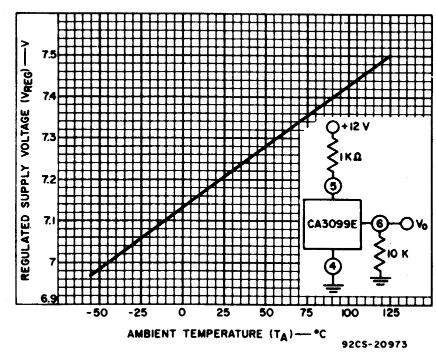


Fig. 5 – Regulated supply voltage vs. ambient temperature.

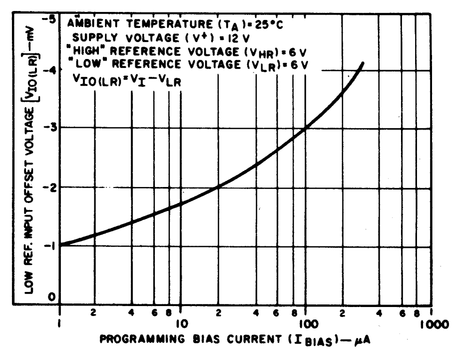


Fig. 6 – Input-offset voltage ("low" reference) vs. programming bias current.

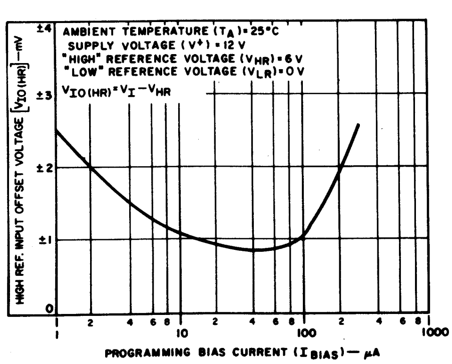


Fig. 7 – Input-offset voltage ("high" reference) vs. programming bias current.

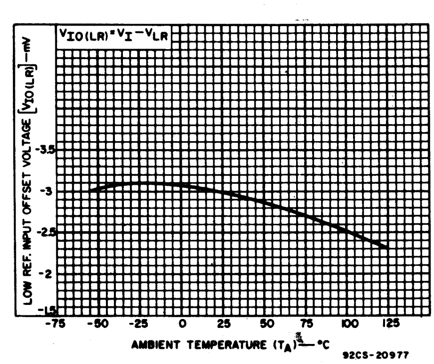


Fig. 8 – Input-offset voltage ("low" reference) vs. ambient temperature.

CA3099E

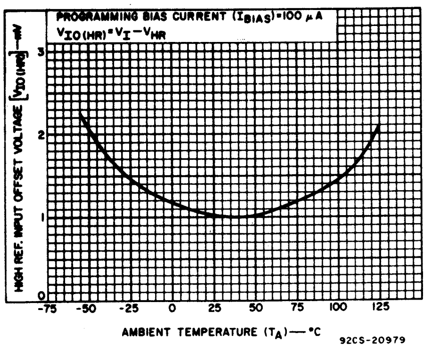


Fig. 9 – Input-offset voltage ("high" reference) vs. ambient temperature.

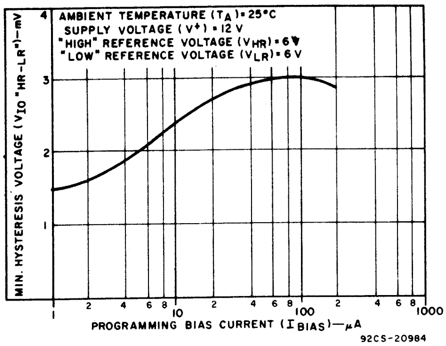


Fig. 10 – Min. hysteresis voltage vs. programming bias current.

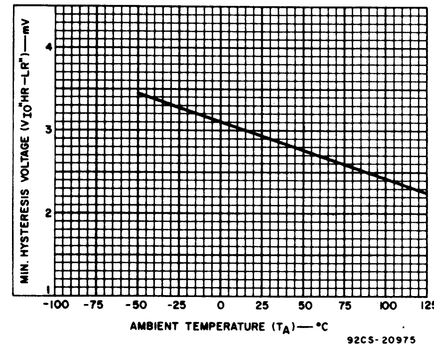


Fig. 11 – Min. hysteresis voltage vs. ambient temperature.

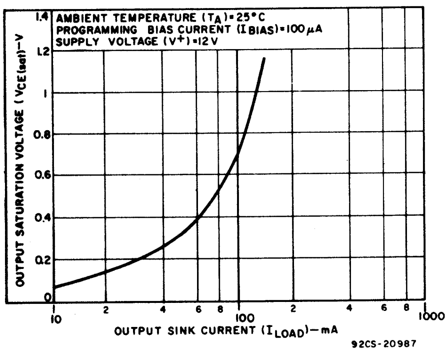


Fig. 12 – Output saturation voltage vs. output sink current.

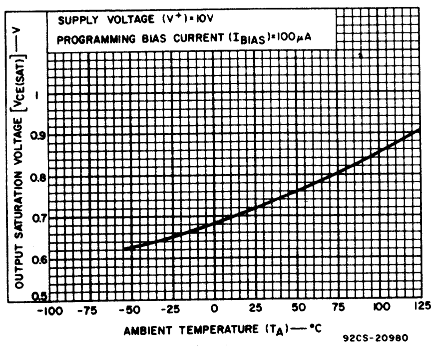


Fig. 13 – Output saturation voltage vs. ambient temperature.

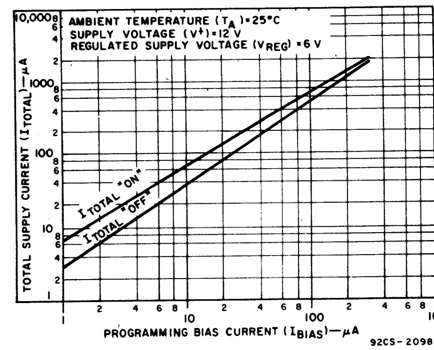


Fig. 14 – Total supply current vs. programming bias current.

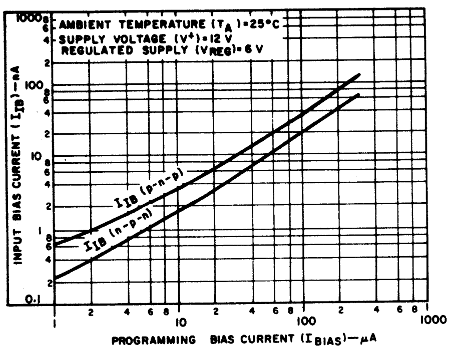


Fig. 15 - Input bias current vs. programming bias current.

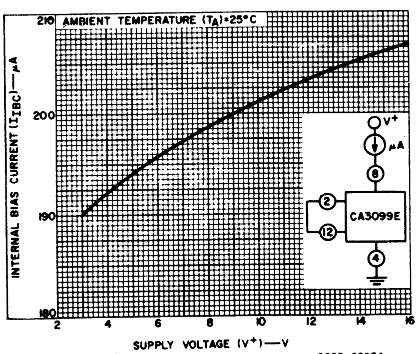


Fig. 16 – Internal bias current vs. supply voltage.

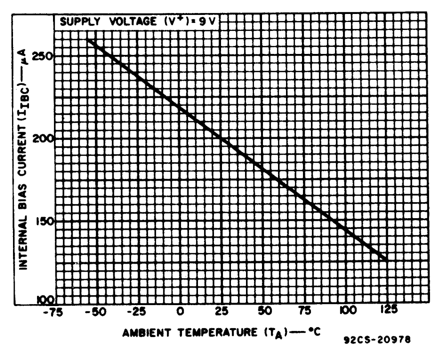


Fig. 17 – Internal bias current vs. ambient temperature.

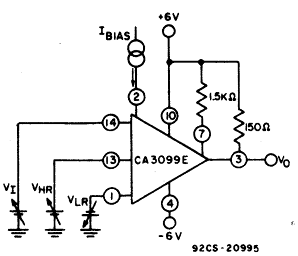


Fig. 18 – Input-offset voltage test circuit.

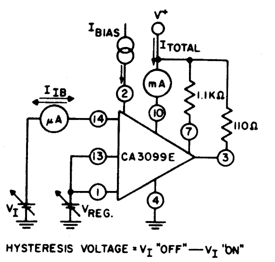


Fig. 19 – Min. hysteresis voltage, total supply current, and input bias current test circuit.

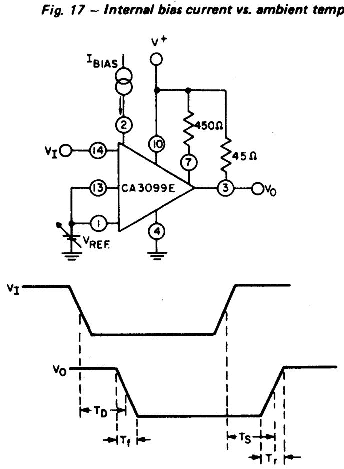


Fig. 20 - Switching time test circuit.

For application information, see Data Bulletin File No. 620.