CA3120E, CA3142E

TV Signal Processors ("Jungle" Circuits)

For Color and Monochrome Receivers

The RCA-CA3120E and CA3142E are monolithic silicon integrated circuit TV signal processors for use in color or monochrome receivers. These circuits provide low-impedance video output signals, stripped synchronization signals in both polarities, and AGC output signals for IF (reverse) and tuner (forward and/or reverse).

The circuit designs of the CA3120E and CA3142E feature impulse noise inversion, delay techniques to reduce the deleterious effects of impulse noise in the receiver AGC and sync circuits. In addition, they incorporate standard AGC strobing techniques. The AGC noise lockout circuit is deleted in the CA3142E.

Features:

- **Internal impulse noise processing**
- **Sync separator – low impedance, dual polarity**
- **Strobed AGC system**
- **IF AGC output**
- **Delayed outputs for forward or reverse AGC tuners**
- **Automatic noise threshold and AGC detector level control**
- **High-impedance video input**
- **Low-impedance video output**
- **Choice of external time constants for sync separator**
- **Negative power supply not required**
- **RF AGC delay externally controlled**

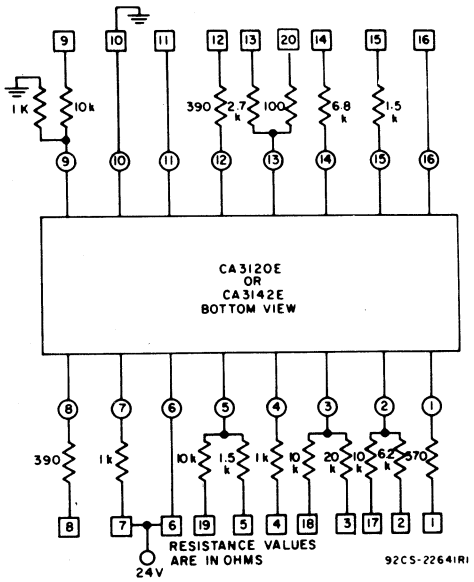


Fig. 2 – Test circuit for measuring electrical characteristics of the CA3120E and CA3142E. Refer to Figs. 7 and 8 for switch selector positions.

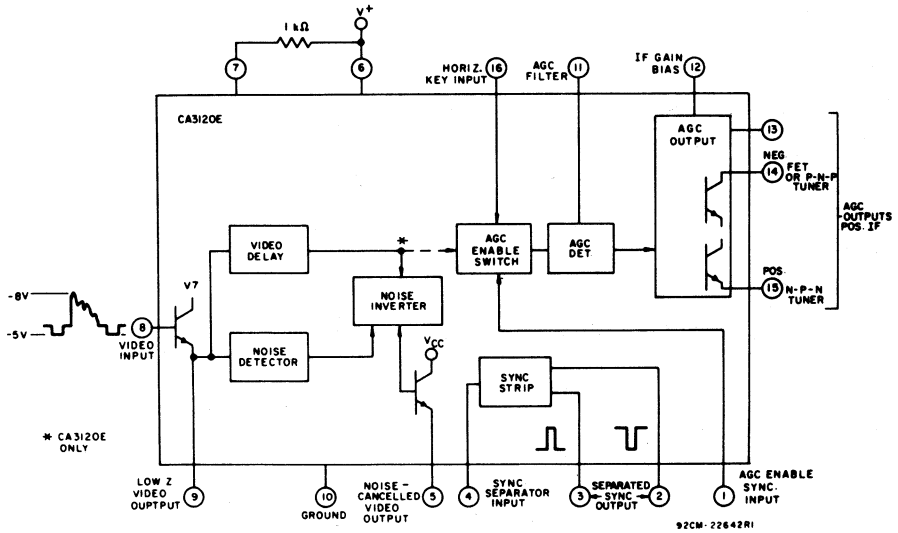


Fig. 1 – Simplified block diagram of the CA3120E and CA3142E.

MAXIMUM RATINGS, Absolute-Maximum Values at $T_A = 25^oC$

DC SUPPLY VOLTAGE	30 V
DEVICE DISSIPATION:	
Up to $T_A = 55^oC$	750 mW
Above $T_A = 55^oC$. . . . . Derate linearly at 7.9	mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	–40 to +85 °C
Storage	–65 to +150 °C
LEAD TEMPERATURE (During soldering):	
At a distance not less than 1/32" (0.79 mm) from case for 10 seconds max.	+265 °C

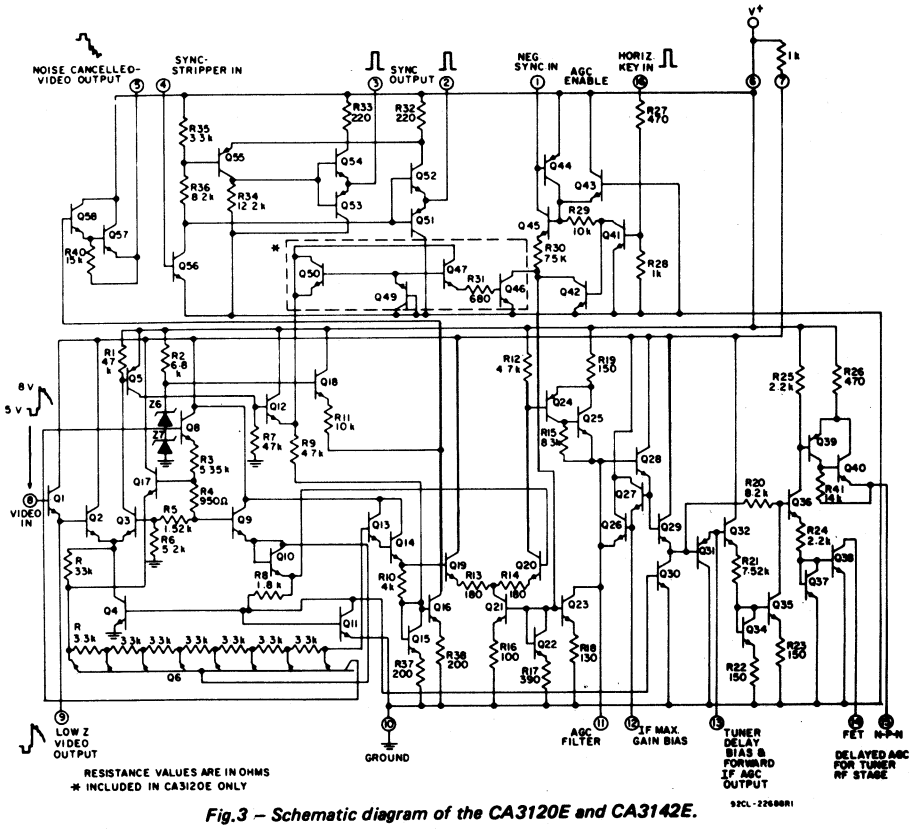


Fig. 3 – Schematic diagram of the CA3120E and CA3142E.

CA3120E, CA3142E

CIRCUIT DESCRIPTION*

An AGC sample-and-hold system generates control voltages proportional to the video level. The sync-tip voltage is compared to an internal reference voltage during the horizontal synchronization (retrace) interval. The control voltages (AGC outputs) are supplied to the tuner's RF stage and the IF amplifier to maintain the video level at a constant value.

The composite positive and negative output sync signals are developed across a low impedance source (totem-pole circuit) at an amplitude of approximately 20 volts peak-to-peak.

Video Chain and Impulse Noise Inverter – The input video signal applied at Terminal 8 is white "positive" with a required amplitude in the range of 2 to 4 volts. The DC level of the sync peaks, AGC threshold voltage (V_{TH}) is approximately 5 volts. The level is maintained at 5 volts by the AGC loop in the circuit, comprised of the CA3120E or CA3142E and the TV receiver RF and IF amplifiers. A low source impedance video signal is available from the emitter of Q1 (Terminal 9 in Fig. 3). The external resistor (R_{X1} in Fig.9) reduces the dissipation of Q1. The emitter-follower output of Q1 is directly coupled to a differential comparator stage (Q2, Q3). Unless a negative-going pulse is present, Q2 functions as an emitter follower and also cuts off transistors Q3, Q5, and Q12.

The output of Q2 is applied through a signal delay network, consisting of transistor Q60 and associated resistors, to the Darlington followers (Q13 and Q14). The delayed video signal at Q14 is fed via its emitter to an AGC comparator Q19 and to the junction of a noise-cancelling amplifier stage (Q16). The noise-cancelled video signal is inverted and amplified by Q16 and then connected to a Darlington emitter-follower output stage (Q57, Q58).

If impulse noise is present on the video signal, Q3 conducts and turns on transistors Q5 and Q12. Q5 inverts and "stretches" the noise pulse width. The output of Q5 is applied to an emitter follower stage (Q12). The signal from Q12, in turn, is applied to the summing junction to the noise-cancelling amplifier Q16. The noise pulse, which has now been amplified, inverted and stretched, is added to the delayed video signal from the emitter of Q14.

Because the video signal has been delayed approximately 300 nanoseconds and the noise pulse has been widened ("stretched") approximately 500 nanoseconds, the output of the combined signal no longer contains impulse noise signals. The derived noise-gating pulse "surrounds" and effectively eliminates the effects of the impulse noise.

The noise-cancelled video signal, amplified and buffered, is available at Terminal 5 for use in the sync-separator stage. The peak-to-peak amplitude of the noise-cancelled output signal is approximately twice the amplitude of the input video signal at Terminal 8.

Sync Separator (See Figure 4) – The sync separator stage (Q56) clamps the detected sync tips to a fixed reference voltage (≅ 0.7 V) across its base-emitter junction, and amplifies a portion of the sync signal to provide dual polarity sync-signal outputs at Terminals 2 (negative) and 3 (positive). The output signals are derived from low-impedance complementary emitter-follower stages; a base current of 100 microamperes into Terminal 4 is sufficient to generate full-amplitude sync signals.

The choice of coupling the noise-cancelled video-signal from the emitter-follower (Terminal 5) to the sync separator (Terminal 4) is a user option. Fig. 5 shows three typical coupling networks.

Fig. 6 illustrates the operation of the AGC circuits. An input ramp signal, simulating the potential to which the AGC filter capacitor may be charged, is applied to Terminal 11. The forward IF AGC output voltage appears at Terminal 13. Under low-signal level conditions (represented by A to B in Fig. 6) the output level is approximately 1.4 volts less than the voltage applied to Terminal 12.

The circuit designer should select the voltage at Terminal 12 to provide the maximum IF gain required for the system. At intermediate signal level conditions (represented by B to C in Fig. 6), the IF AGC signal follows the AGC filter potential. The tuner(s) will operate at maximum gain for good signal-to-noise ratios at these equivalent input signal levels. Point C is a turnover point determined by the open-circuit potential of the tuner-delay bias potentiometer. At this potential, further change in the IF AGC output is inhibited (for good dynamic range) and the tuner AGC potentials are activated (represented by C to D).

The output at Terminal 14 with suitable level shifting is used for tuners requiring reverse AGC, such as MOSFET or electron-tube types. The output at Terminal 15 is used for tuners requiring forward AGC, such as tuners utilizing n-p-n bipolar transistors.

* For additional information refer to the IEEE Transactions on Broadcast and TV Receivers," August 1970, pp. 185–195, Vol. BTR No.3.

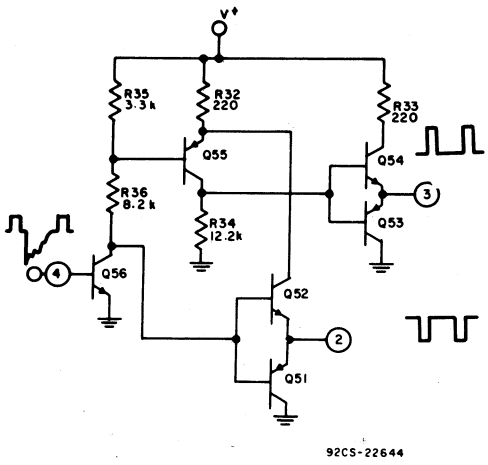


Fig. 4 – Sync separator stage.

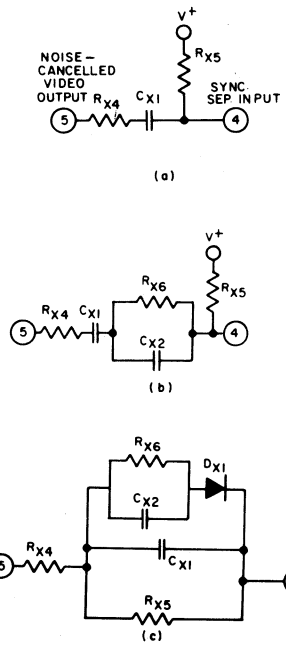


Fig. 5 – Typical coupling networks (Term. 5 to Term. 4).

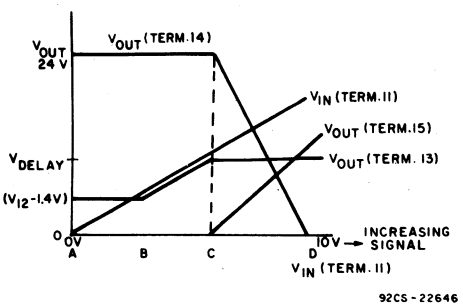


Fig. 6 – Typical operation of the AGC circuits using the CA3120E and CA3142E.

CA3120E, CA3142E

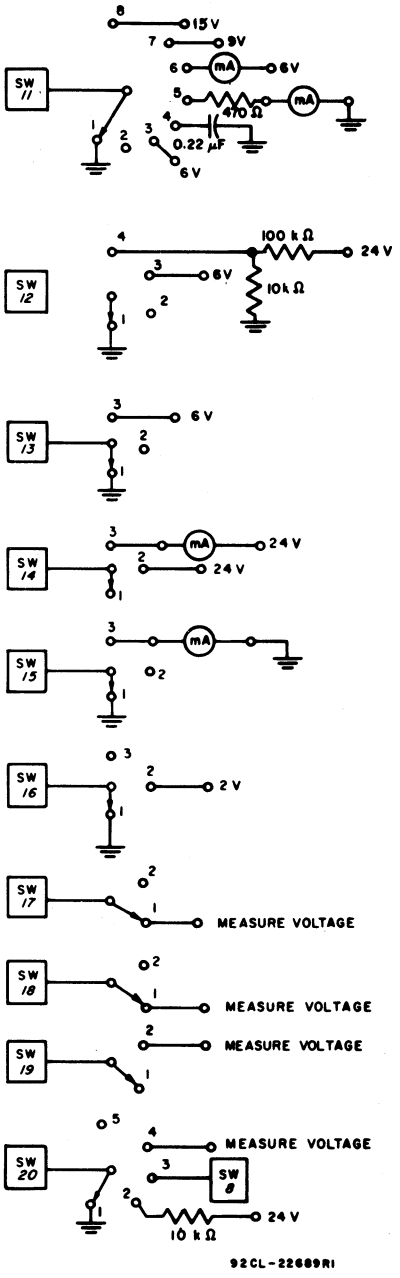
CHARACTERISTIC	TEST CONDITIONS — SWITCH NUMBERS / SWITCH POSITION																		TERMINAL MEASURED
	1	2	3	4	5	8	9	11	12	13	14	15	16	17	18	19	20	
I_{T24}	2	3	1	2	1	2	3	1	1	3	2	1	2	2	2	1	5	2 6 7 9 14
V_{TH}	2	1	2	1	1	4	3	4	4	3	1	2	2	2	2	1	3	8
V_5	2	1	2	1	1	4	3	4	4	3	1	2	2	2	2	2	3	19
$V_{TH(SEP)}$	3	1	2	1	1	*	3	3	4	1	1	2	1	2	2	2	1	*
$I_{4(OFF)}$	3	1	2	4	2	1	1	1	1	1	1	2	1	2	2	1	1	I_4
V_{2L}	1	2	2	3	2	1	1	1	1	1	1	2	1	1	2	1	1	V_{17}
V_{2H}	3	3	1	1	2	1	1	1	1	1	1	2	1	1	2	1	1	V_{17}
V_{3L}	3	3	1	1	2	1	1	1	1	1	1	2	1	2	1	1	1	V_{18}
V_{3H}	3	3	1	3	2	1	1	1	1	1	1	2	1	2	1	1	1	V_{18}
$I_{11(CH)}$	2	1	2	5	2	1	1	5	4	3	1	2	2	2	2	1	5	I_{11}
$I_{11(DISCH)}$	2	1	2	5	1	2	3	6	4	3	1	2	2	2	2	1	5	I_{11}
$I_{11(LEAK)}$	2	1	2	5	2	1	1	6	4	3	2	2	1	2	2	1	5	I_{11}
V_{11}	2	1	2	5	1	2	3	2	3	3	1	2	2	2	2	1	5	V_{11}
V_{12}	3	1	2	5	2	1	1	3	4	3	1	2	1	2	2	1	5	V_{12}
$V_{13(LOW)}$	3	1	2	5	2	2	3	1	1	2	1	2	1	2	2	1	2	V_{13}
$V_{13(HIGH)}$	3	1	2	5	2	2	3	7	4	3	2	1	1	2	2	1	4	V_{20}
$I_{14(OFF)}$	3	1	2	5	2	2	3	3	4	3	3	1	1	2	2	1	5	I_{14}
$I_{14(ON)}$	3	1	2	5	2	2	3	8	4	3	3	1	1	2	2	1	5	I_{14}
$I_{15(OFF)}$	3	1	2	5	2	2	3	3	4	3	2	3	1	2	2	1	5	I_{15}
$I_{15(ON)}$	3	1	2	5	2	2	3	8	4	3	2	3	1	2	2	1	5	I_{15}

CAUTION: Remove power before selecting or adjusting switches.

* Reduce voltage at Terminal 8 until V_{19} decreases. $V_{TH(SEP)} = V_{TH} - V_8$.

NOTE: Switch numbers in italics correspond to numbers in square boxes in Figs. 2 and 8.

Fig.7 – Test condition values for associated switches 1 through 20 (switches 6, 7, and 10 are omitted). Refer to Figs. 2 and 8 for test circuit and test-condition selector-switch arrangements.



NOTE: The italicized numbers in the square boxes refer to the 17 switches (switches 6, 7, and 10 are omitted) of the test circuit and correspond to those given in Figs. 2 and 7.

CAUTION: Remove power before selecting or adjusting switches

Fig.8 – Test condition selector switch arrangement for measuring the electrical characteristics of the CA3120E and CA3142E.

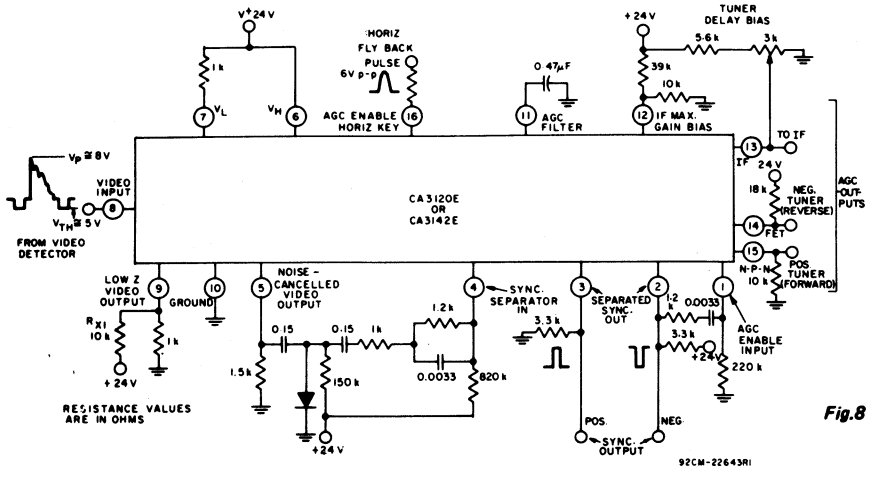


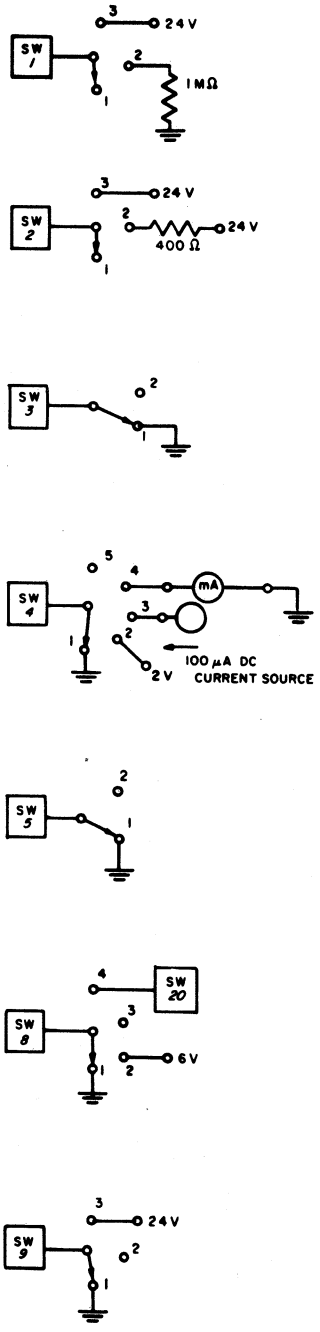
Fig.9 – Typical application using the CA3120E and CA3142E.

(Figure 8 continued on the next page)

CA3120E, CA3142E

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$, Supply Voltage (V^+) = 24 V and Referenced to Test Circuits and Test Conditions (Figs. 2, 7, and 8).

CHARACTERISTICS	TERMINAL MEASURED AND SYMBOL	CA3120E CA3142E LIMITS			UNITS
		Min.	Typ.	Max.	
Supply Current (Pulse Test)	I_{T24}	20	–	40	mA
AGC Threshold (Sync Tip Level at Video Input)	V_{TH}	4.5	–	5.5	V
Video Input Amplitude (White Positive)	V_8	–	3	–	Vp-p
Video Output Amplitude (Low Impedance)	V_9	–	3	–	Vp-p
Noise Cancelled Video Output at V_{TH} (Black Positive, Gain ≅ 2)	V_5	3.6	–	9.2	V
AGC to Noise Separation	$V_{TH\ (SEP)}$	1.1	–	2.2	V
Sync Input Current for Full Amplitude Outputs	$I_{4\ (ON)}$	–	–	100	μA
Maximum Leakage Current at Terminal 4	$I_{4\ (OFF)}$	–	–	±6	μA
Sync Outputs:					
Negative Sync Low	$V_{2(L)}$	0	–	2.6	V
Negative Sync High	$V_{2(H)}$	23.8	–	24	V
Positive Sync Low	$V_{3(L)}$	0	–	0.2	V
Positive Sync High	$V_{3(H)}$	20.1	–	24	V
AGC Filter:					
Charge Current (Pulse Test)	$I_{11(CH)}$	12	–	36	mA
Discharge Current	$I_{11(DISCH)}$	1.1	–	2.6	mA
Leakage Current	$I_{11(LEAK)}$	–	–	±6	μA
AGC Enable:					
Horizontal Keying	$V_{16\ (ON)}$	3	–	6	V
Negative Sync Input Current	$I_{1\ (ON)}$	–	1	–	mA
Maximum IF Gain-Clamp Voltage	V_{11}	4.8	–	5.7	V
Maximum IF Gain Bias	V_{12}	4.2	–	5.2	V
IF AGC Voltage:					
Low	$V_{13\ (LOW)}$	0	–	3.3	V
High	$V_{13(HIGH)}$	5.7	–	6	V
Tuner Currents:					
Reverse AGC (FET) OFF Current	$I_{14\ (OFF)}$	–	–	±6	μA
Reverse AGC (FET) ON Current	$I_{14\ (ON)}$	1.8	–	5.5	mA
Forward AGC (n-p-n) OFF Current	$I_{15\ (OFF)}$	–	–	±6	μA
Reverse AGC (n-p-n) ON Current	$I_{15\ (ON)}$	4.5	–	15	mA
Internal Noise-Lockout Time (CA3120E only)	T	1	–	63	μs



NOTE: The italicized numbers in the square boxes refer to the 17 switches (switches 6, 7, and 10 are omitted) of the test circuit and correspond to those given in Figs. 2 and 7.

CAUTION: Remove power before selecting or adjusting switches

Fig.8 – Test condition selector switch arrangement for measuring the electrical characteristics of the CA3120E and CA3142E.

CA3121E

TV Chroma Amplifier/Demodulator

Provides Complete System for Processing Chroma When Used with RCA-CA3070

RCA-CA3121E is a monolithic silicon integrated circuit chroma amplifier/demodulator with ACC and killer control for color-TV receivers. It is designed to function compatibly with the CA3070 in a two package chroma system. Fig. 4 shows a functional block diagram and the outboard circuitry of a typical two-package chroma system incorporating the CA3121E and CA3070, respectively.

The CA3121E is supplied in a 16-lead dual-in-line plastic package.

Features

- **Excellent linearity in dc chroma gain-controlled circuit**
- **Improved filtering reduces 7.2 MHz output from the color demodulators**
- **Current limiting for short-circuit protection**
- **Good tolerance to B+ supply variations**
- **Good temperature coefficient stability**

MAXIMUM RATINGS at T_A = 25°C

Supply Voltage	30 V
Device Dissipation:	
Up to T_A = 55°C	750 mW
Above T_A = 55°C	derate linearly 7.9 mW/°C
Operating Temperature Range	−40 to +85°C
Lead Temperature (During Soldering)	
At distance 1/16" ±1/32" (1.59 ±0.79 mm) from case for 10 s max.	+265°C

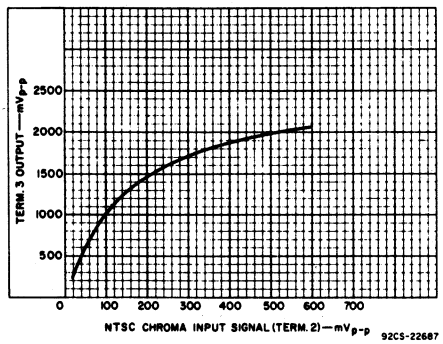


Fig. 2 – Typical ACC plot for the CA3121E when used with the CA3070.

CIRCUIT OPERATION

The CA3121E consists of three basic circuit sections: (1) amplifier No. 1, (2) amplifier No. 2, and (3) demodulator. Amplifier No. 1 contains the circuitry for automatic chroma control (ACC) and color-killer sensing. The output of amplifier No. 1 (Terminal 3) is coupled to the Chroma Signal Processor (CA3070 or equivalent) for ACC and automatic phase control (APC) operation and to the input of amplifier No. 2 (Terminal 4) containing the chroma gain control circuitry. The signal from the color-killer circuit in amplifier No. 1 acts upon amplifier No. 2 to greatly reduce its gain.

The output from amplifier No. 2 (Terminal 14) is applied, through a filtering network, to the demodulator input (Terminal 13). The demodulator also receives the R-Y and B-Y demodulation subcarrier signals (Terminals 7 and 8) from the oscillator output of the chroma signal processor. The R-Y and B-Y demodulators and the matrix network contained in the demodulator section of the CA3121E reconstruct the G-Y signal to achieve the R-Y, G-Y, and B-Y color difference signals. These high-level outputs signals with low impedance outputs are suitable for driving high-level R, G, B output amplifiers. Internal capacitors are included on each output to filter out unwanted harmonics. For additional operating information and signal waveforms, refer to Television Chroma System (utilizing RCA-CA3070, CA3071, CA3072), File No. 468.

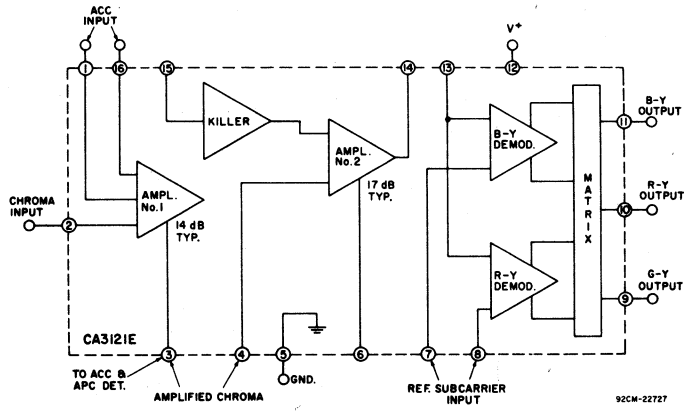


Fig. 1 – Functional block diagram of the CA3121E.

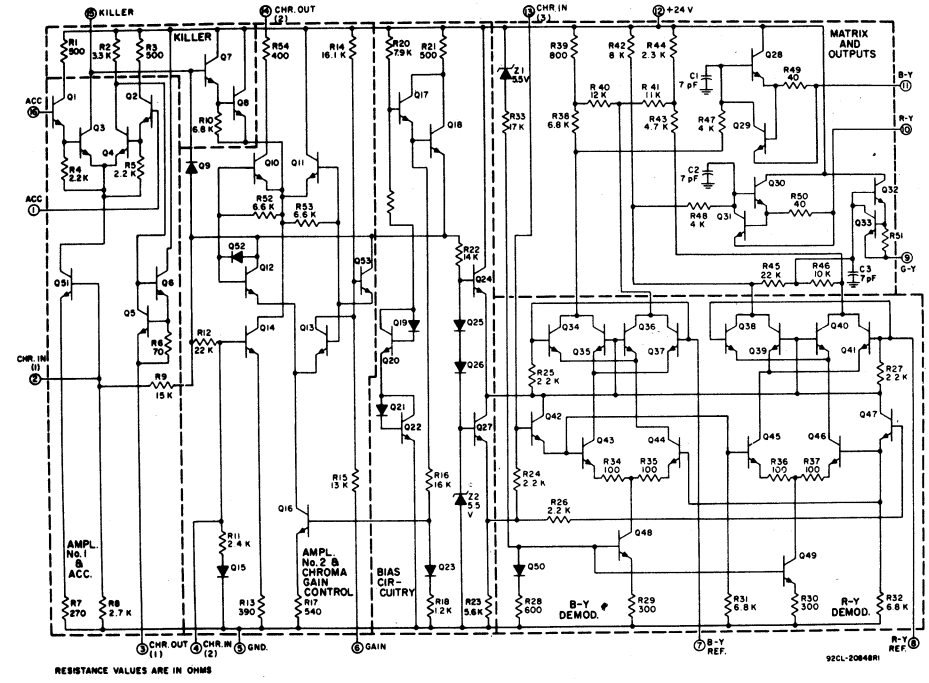


Fig. 3 – Schematic diagram of the CA3121E.

ELECTRICAL CHARACTERISTICS at T_A = 25°C and Referenced to Test Circuit (Fig. 5)

CHARACTERISTIC	TERMINAL MEASURED AND SYMBOL	TEST CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Supply Current	I_T	–	–	40	44	mA
Input Sensitivity	V_2	Vary Eg; set V_4 for 55 mV RMS	6	10	15	mV RMS
Second-Stage Sensitivity	V_4	Vary Eg; set V_{11} for 2 V RMS	25	55	100	mV RMS
Output Voltage (Killer off)	V_{11}	Switch Position: S1=2, S2=2, S3=2 Adjust killer potentiometer until output drops	–	–	70	mV RMS
Demodulator Characteristics:						
Output Voltages	V_9, V_{10}, V_{11}		13	14.3	15.6	V
DC Output Balance (Between any 2 outputs)	–	–	−0.6	–	+0.6	V
Unbalance	V_9, V_{10}, V_{11}	Eg=0; Switch Position: S1=1, S2=1, S3=1	–	–	0.8	Vp-p
Relative Outputs—R-Y	V_{10}	Vary Eg; set V_{11} for 2 V RMS	1.4	1.52	1.68	V RMS
G-Y	V_9		0.3	0.4	0.5	V RMS
Relative Phase—R-Y	V_{10}	Vary Eg; set V_{11} for 2 V RMS; read phase of V_{10} and V_9	−101	−106	−111	degrees
G-Y	V_9	with V_{11} as reference	112	104	96	degrees
Max. Output Voltage	V_{11}	Eg = 750 mV	2.8	–	–	V RMS

CA3121E

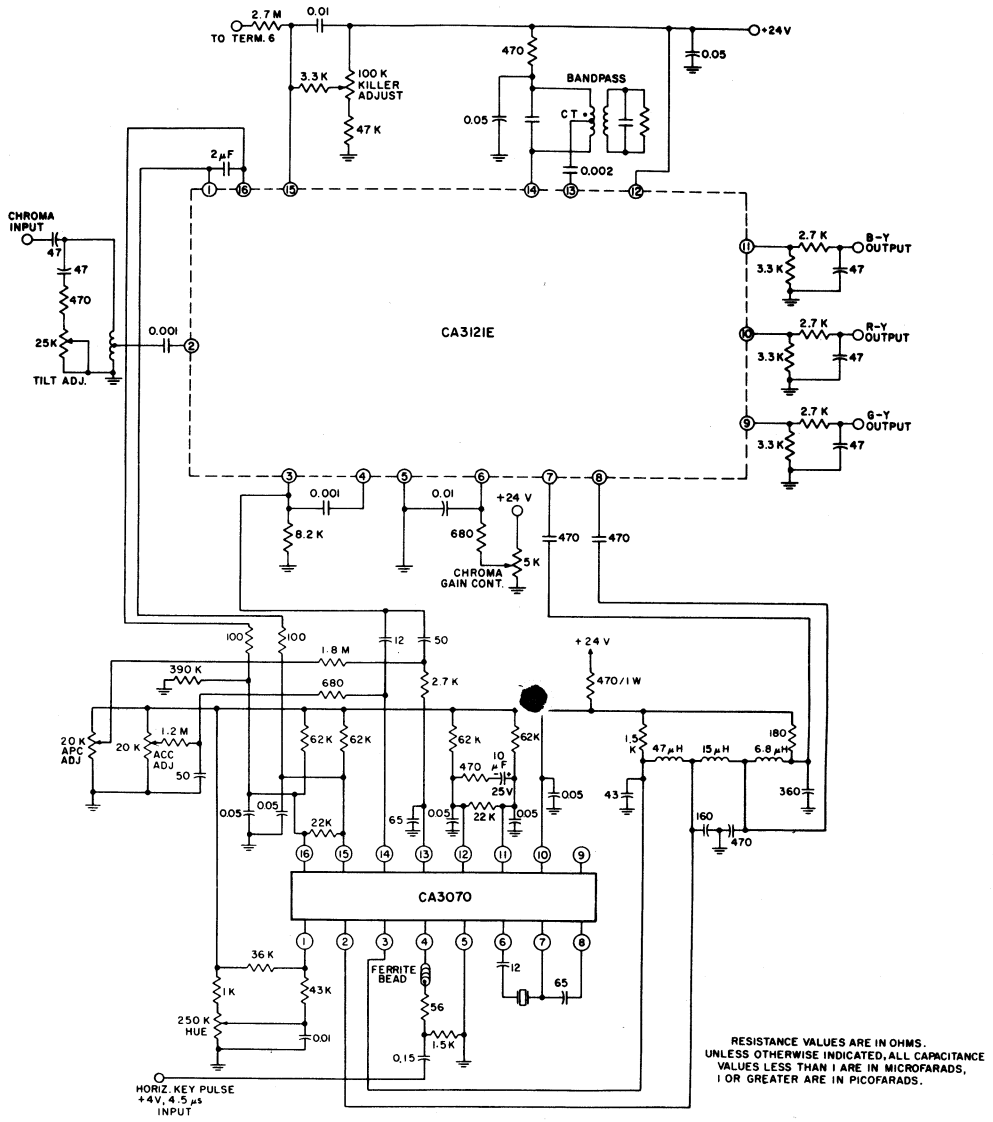


Fig. 4 – Outboard circuitry of a typical two-package chroma system for color-TV receivers utilizing the CA3121E and CA3070.

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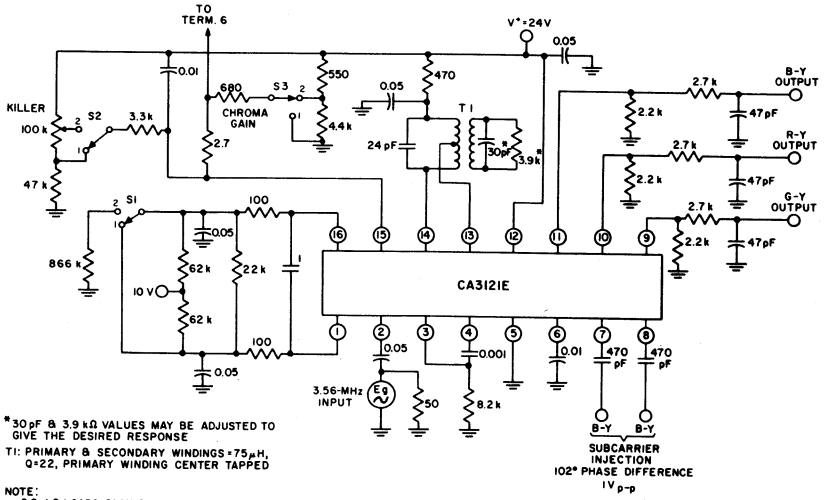


*30 pF & 3.9 kΩ VALUES MAY BE ADJUSTED TO GIVE THE DESIRED RESPONSE

T1: PRIMARY & SECONDARY WINDINGS = 75 μH, Q = 22, PRIMARY WINDING CENTER TAPPED

NOTE:
2.2-kΩ LOADS ONLY FOR TEST PURPOSE, 3.3-kΩ LOADS RECOMMENDED FOR APPLICATIONS.
RESISTANCE VALUES ARE IN OHMS.
CAPACITANCE VALUES ARE IN MICROFARADS UNLESS OTHERWISE INDICATED.

92CM-22732

Fig. 5 – Typical characteristics test circuit for the CA3121E.

CA3123E

AM Radio Receiver Subsystem

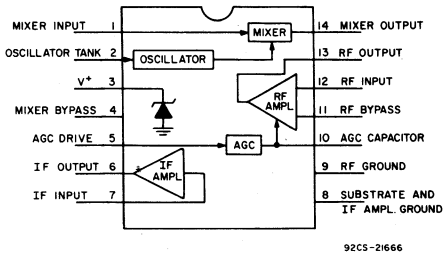
Includes RF Amplifier, IF Amplifier, Mixer, Oscillator, AGC Detector, and Voltage Regulator

The CA3123E* is a monolithic silicon integrated circuit that provides an rf amplifier, if amplifier, mixer, oscillator, AGC detector, and voltage regulator on a single chip. It is intended for use in super-heterodyne AM radio receiver applications particularly in automobiles. The CA3123E is supplied in a 14-lead dual-in-line plastic package and operates over the temperature range of −55° to 125°C.

* Formerly RCA Dev. No. TA6155

Features:

- Low-noise, low-R_b' rf stage in cascode connection — eliminates Miller-Effect regeneration and allows controlled power rise by the choice of external components
- Mixer-oscillator stage with internal feedback — eliminates need for tapped or multi-winding oscillator coils
- Cascode if amplifier with controlled output impedance and negligible Miller Effect — eliminates regeneration and selectivity skewing
- Frequency-counter AGC circuit — allows control of AGC response by selection of the coupling capacitor
- Integral regulation with built-in surge protection
- Separately accessible amplifiers



Terminal assignment diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:	
At Terminal No. 3 (V^+)	9 V
At Terminal No. 6 (IF Output)	40 V
At Terminal No. 13 (RF Output)	20 V
At Terminal No. 14 (Mixer Output)	20 V
DC CURRENT:	
Into Terminal No. 3 (V^+)	35 mA
DEVICE DISSIPATION:	
Up to T_A = 55°C	750 mW
Above T_A = 55°C	derate linearly 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to +125°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16" ± 1/3" (1.59 mm ± 0.79 mm) from case for 10 s max.	265°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Static Characteristics In Circuit of Fig. 3						
DC Voltage:						
At Terminals 1, 4	V_1,V_4			4.7		V
At Terminals 2, 3, 14	V_2,V_3,V_{14}			6.8		V
At Terminal 5	V_5			0.25		V
At Terminal 6	V_6			12		V
At Terminal 7	V_7			0.76		V
At Terminals 8, 9	V_8,V_9			0		V
At Terminals 10, 11	V_{10},V_{11}			0.71		V
At Terminal 12	V_{12}			0.71		V
At Terminal 13	V_{13}			4.0		V
DC Current:						
Into Terminals 1, 4, 5, 7 8, 9, 10, 11, 12	I_1,I_4,I_5,I_7, I_8,I_9,I_{10},I_{11},I_{12}			0		mA
Into Terminal 2	I_2			1.2		mA
Into Terminal 3	I_3			15		mA
Into Terminal 6	I_6			4.3		mA
Into Terminal 13	I_{13}			4.5		mA
Into Terminal 14	I_{14}			0.170		mA
Performance Characteristics In Circuit of Fig. 3						
Sensitivity		Input Signal to Dummy Antenna at f_{IN}=1 MHz, 30% AM Modulation at f_{MOD}=400 Hz, for 11 mV output at V_O	–	2.3	5	μV
Signal-to-Noise Ratio	S/N	Ratio of Output at V_O with Modulation ON and then OFF, Input Signal=100 μV, 30% AM Modulation at f_{MOD}=400 Hz	34	43	–	dB
Overload Distortion		Input Signal set at 1 MHz, 90% AM Modulation, Distortion at V_O must be ≤ 10%	160000	400000	–	μV

Dynamic Characteristics For Indicated Stages In Circuit of Fig. 3

Stage	Parallel Capacitance Input pF	Parallel Capacitance Output pF	Parallel Resistance Input Ω	Parallel Resistance Output Ω	Transconductance μmhos
RF Amplifier	80	6	750	2 x 10^6 min.	140000
IF Amplifier	35	3.5	950	10^4	80000
Mixer	6	2	2000	2 x 10^6 min.	2500 (Mixer) 3000 (Amplifier)

TYPICAL CHARACTERISTICS

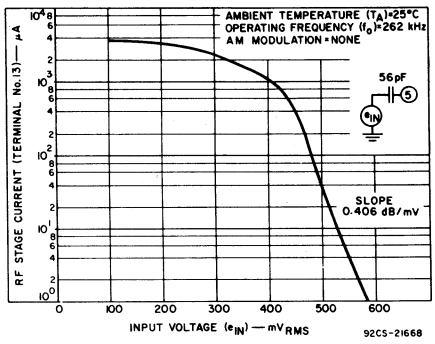


Fig. 1 — Control of RF stage by signal into Terminal No.5.

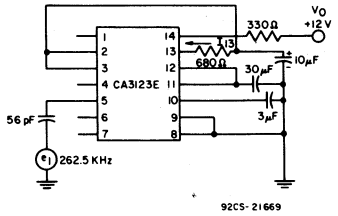
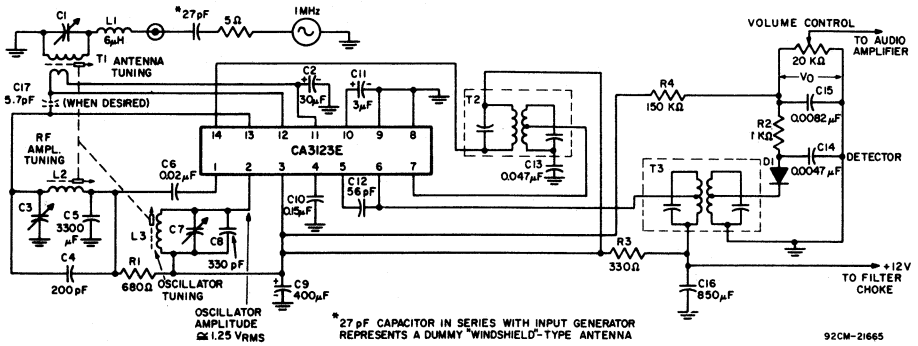


Fig. 2—Test circuit for Fig. 1.

CA3123E



Transformer	Symbol	Frequency	Inductance μh (≈)	Capacitance pF (≈)	Q (≈)	Total Turns To Tap Turns Ratio	Coupling
First IF: Primary	T_2	262 kHz	2840	130	60	none	critical ≈0.017 ≈1/Q
Secondary			2840	130	60	or 30:1 31:1	
Second IF: Primary	T_3	262 kHz	2840	130	60	8.5:1	–
Secondary			2840	130	60	8.5:1	critical ≈0.017 ≈1/Q
Antenna: Primary	T_1	1 MHz	195	$(C_1)-130$	65		
Secondary		Adjusted to an impedance of 75 Ω with primary resonant at 1 MHz. Coupling should be as tight as practical. Wire should be wound around end of coil away from tuning core.					
Coils	L_1	7.9 MHz	6		50		
	L_2	1 MHz	55		50		
	L_3	1.262 MHz	41		40		

Fig. 3– Schematic diagram of AM radio receiver using CA3123E.

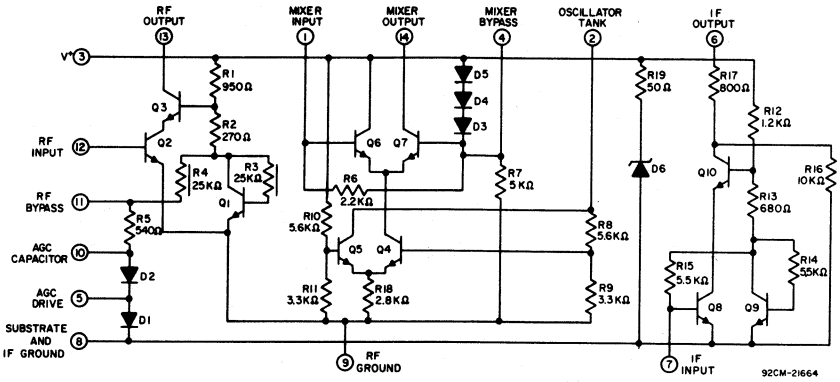


Fig. 4 – Schematic diagram of CA3123E.

PERFORMANCE CHARACTERISTICS IN CIRCUIT OF FIG. 3

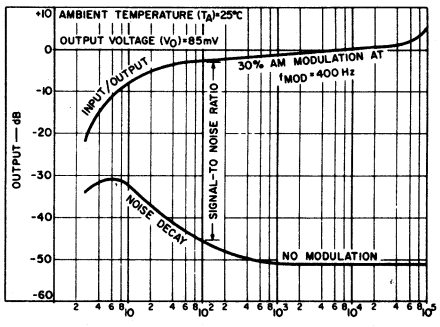


Fig.5 – Signal-to-noise performance.

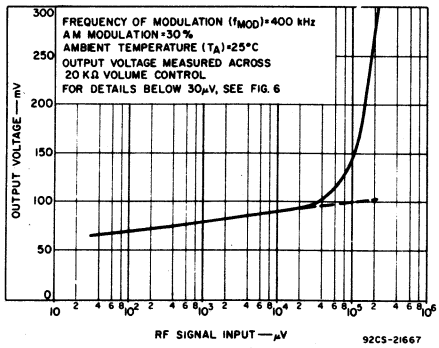


Fig.6 – AGC curve showing voltage rise (controlled by external capacitance of 5.7 pF: C_{17}, Fig.3).

Change in slope in the vicinity of 40000 μV signal input voltage is the result of the use of C_{17} (5.7 pF) in Fig.3. The dotted curve indicates expected performance if $C_{17} = 0$.

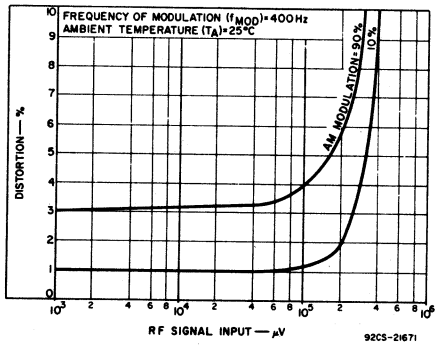


Fig.7 – Overload response.