élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2001/EL2001C
Low Power, 70 MHz Buffer Amplifier

Features
- 1.3 mA supply current
- 70 MHz bandwidth
- 2000 V/μs slew rate
- Low bias current, 1 μA typical
- 100 mA output current
- Short circuit protected
- Low cost
- Stable with capacitive loads
- Wide supply range ±5 V to ±15 V
- No thermal runaway

Applications
- Op-amp output current booster
- Cable/line driver
- A/D input buffer
- Low standby current systems

Ordering Information

Part No.	Temp. Range	Package	Outline # *
EL2001ACJ	−25 to +85°C	Cerdip	MDP0010
EL2001ACJ/E+	−25 to +85°C	Cerdip	MDP0010
EL2001ACN	−25 to +85°C	P-Dip	MDP0006
EL2001ACN/E+	−25 to +85°C	P-Dip	MDP0006
EL2001AJ	−55 to +125°C	Cerdip	MDP0010
EL2001AJ/883B	−55 to +125°C	Cerdip	MDP0010
EL2001AL	−55 to +125°C	20 pad LCC	MDP0007
EL2001AL/883B	−55 to +125°C	20 pad LCC	MDP0007
EL2001CJ	−25 to +85°C	Cerdip	MDP0010
EL2001CJ/E+	−25 to +85°C	Cerdip	MDP0010
EL2001CM	−25 to +85°C	20 lead SOL	MDP0027
EL2001CN	−25 to +85°C	P-Dip	MDP0006
EL2001CN/E+	−25 to +85°C	P-Dip	MDP0006
EL2001J	−55 to +125°C	Cerdip	MDP0010
EL2001J/883B	−55 to +125°C	Cerdip	MDP0010
EL2001L	−55 to +125°C	20 pad LCC	MDP0007
EL2001L/883B	−55 to +125°C	20 pad LCC	MDP0007

* For package outline drawings, see Elantec 1988 Databook

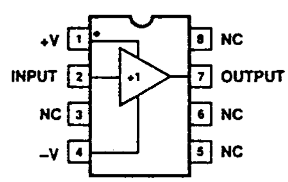
General Description
The EL2001 is a low cost monolithic, high slew rate, buffer amplifier. Built using the Elantec monolithic dielectric isolation process, this patents pending buffer has a −3 dB bandwidth of 70 MHz, and delivers 100 mA, yet draws only 1.3 mA of supply current. It typically operates from ±15 V power supplies but will work with as little as ±5 V.

This high speed buffer may be used in a wide variety of applications in military, video and medical systems. A typical example is a general purpose op-amp output current booster where the buffer must have sufficiently high bandwidth and low phase shift at the maximum frequency of the op-amp. The EL2001 is available in the 8-pin Plastic Dip and Cerdip, 20 pad LCC and 20 lead SOL packages.

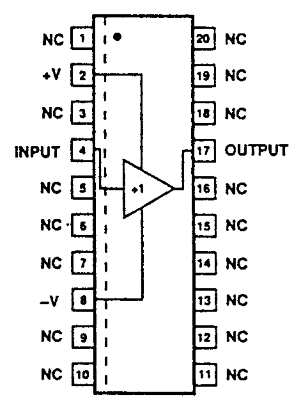
Elantec's products and facilities comply with MIL-STD-883 Revision C, MIL-I-45208A, and other applicable quality specifications. For information on Elantec's military processing, see the Elantec document, QRA-2: *Elantec's Military Processing, Monolithic Integrated Circuits.*

Connection Diagrams

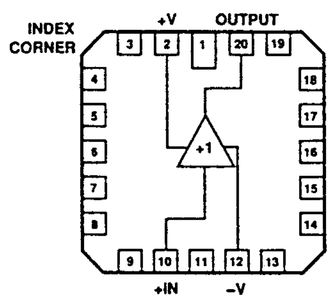
EL2001 DIP Pinout
(Top View)



EL2001 SOL Pinout
(Top View)



EL2001 LCC Pinout
(Top View)



Note: All information contained in this data sheet has been carefully checked and is believed to be accurate as of the date of publication; however, this data sheet cannot be a "controlled document". Current revisions, if any, to these specifications are maintained at the factory and are available upon request. We recommend checking the revision level before finalization of your design documentation. Patent Pending CMS#2001DS

Absolute Maximum Ratings

V_S	Supply Voltage (V^+–V^-)	±18 V or 36 V	T_J	Operating Junction Temperature	
V_{IN}	Input Voltage (Note 1)	±15 V or V_S		Ceramic Packages	+175°C
I_{IN}	Input Current (Note 1)	±50 mA		Plastic Packages	+150°C
P_D	Power Dissipation (Note 2)	See Curves	T_{ST}	Storage Temperature	–65°C to +150°C
	Output Short Circuit			Lead Temperature	
	Duration (Note 3)	Continuous		DIP Package (soldering, <10 sec.)	+300°C
T_A	Operating Temperature Range:			SOL Package	
	EL2001A/EL2001	–55°C to +125°C		Vapor Phase (60 sec.)	+215°C
	EL2001AC/EL2001C	–25°C to +85°C		Infrared (15 sec.)	+220°C

Important Note: **All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX 77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.**

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C, and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value for information purposes only.

Electrical Characteristics V_S = ±15 V, R_S = 50 Ω, Unless Otherwise Specified

	Parameter	Test Conditions V_{in}	Test Conditions Load	Test Conditions Temp	Limits Min.	Limits Typ.	Limits Max.	EL2001A EL2001 Test Level	EL2001AC EL2001C Test Level	Units
V_{OS}	Offset Voltage									
	EL2001A/EL2001AC	0	∞	25°C	–10	2	+10	I	I	mV
				T_{min}, T_{max}	–15		+15	I	III	mV
	EL2001/EL2001C	0	∞	25°C	–30	2	+30	I	I	mV
				T_{min}, T_{max}	–40		+40	I	III	mV
I_{in}	Input Current									
	EL2001A/EL2001AC	0	∞	25°C	–3	1	+3	I	I	μA
				T_{min}, T_{max}	–6		+6	I	III	μA
	EL2001/EL2001C	0	∞	25°C	–5	1	+5	I	I	μA
				T_{min}, T_{max}	–10		+10	I	III	μA
R_{in}	Input Resistance	±12V	100Ω	25°	3	8		I	I	MΩ
				T_{min}, T_{max}	1			I	III	MΩ

Electrical Characteristics – Continued $V_S = \pm 15$ V, $R_S = 50\ \Omega$, Unless Otherwise Specified

	Parameter	Test Conditions V_{in}	Load	Temp	Limits Min.	Typ.	Max.	EL2001A EL2001 Test Level	EL2001AC EL2001C Test Level	Units
A_{v1}	Voltage Gain	±12V	∞	25°C	0.990	0.998		I	I	V/V
				T_{min}, T_{max}	0.985			I	III	V/V
A_{v2}	Voltage Gain	±10V	100Ω	25°C	0.83	0.93		I	I	V/V
				T_{min}, T_{max}	0.80			I	III	V/V
A_{v3}	Voltage Gain with $V_S = \pm 5$V	±3V	100Ω	25°C	0.82	0.89		I	I	V/V
				T_{min}, T_{max}	0.79			I	III	V/V
V_O	Output Voltage Swing	±12V	100Ω	25°C	±10	±11		I	I	V
				T_{min}, T_{max}	±9.5			I	III	V
R_{OUT}	Output Resistance	±2V	100Ω	25°C		10	15	I	I	Ω
				T_{min}, T_{max}			18	I	III	Ω
I_{OUT}	Output Current	±12V	Note 4	25°C	±100	±160		I	I	mA
				T_{min}, T_{max}	±95			I	III	mA
I_s	Supply Current	0	∞	25°C		1.3	2.0	I	I	mA
				T_{min}, T_{max}			2.5	I	III	mA
PSRR	Supply Rejection, Note 5	0	∞	25°C	60	75		I	I	dB
				T_{min}, T_{max}	50			I	III	dB
t_r	Rise Time	0.5V	100Ω	25°C		4.2		V	V	ns
t_d	Propagation Delay	0.5V	100Ω	25°C		2.0		V	V	ns
SR	Slew Rate, Note 6	±10V	100Ω	25°C	1200	2000		IV	IV	V/µs

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input to output voltage exceeds ±7.5 V then the input current must be limited to ±50 mA. See the applications section for more information.

Note 2: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.

Note 3: A heat sink is required to keep the junction temperature below the absolute maximum when the output is short circuited.

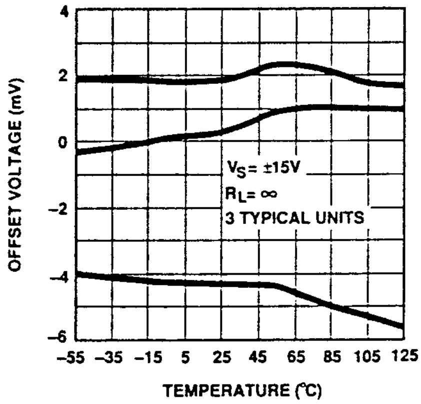
Note 4: Force the input to +12 V and the output to +10 V and measure the output current. Repeat with −12 V_{in} and −10 V on the output.

Note 5: V_{OS} is measured at $V_S+ = +4.5$ V, $V_S- = -4.5$ V and at $V_S+ = +18$ V, $V_S- = 18$ V. Both supplies are changed simultaneously.

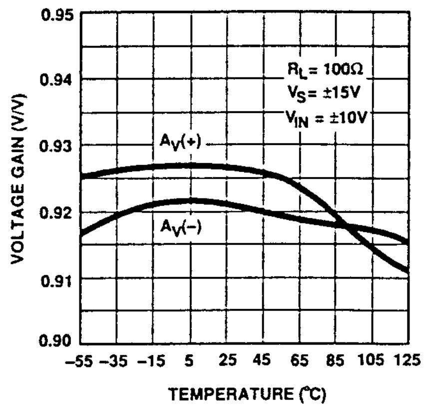
Note 6: Slew rate is measured between $V_{out} = +5$ V and −5 V.

Typical Performance Curves

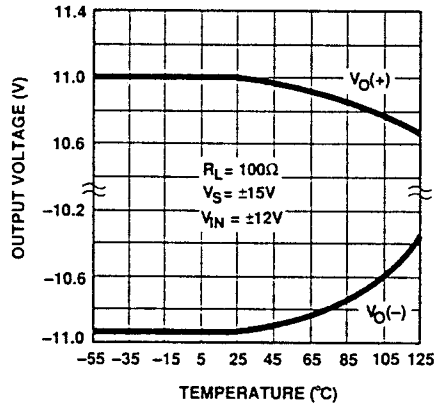
Offset Voltage vs Temperature



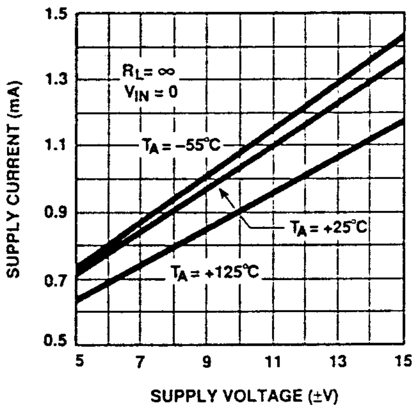
Voltage Gain vs Temperature



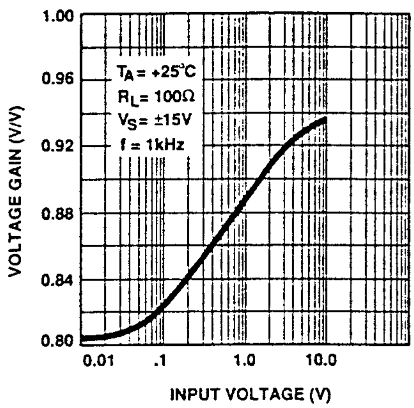
Output Voltage Swing vs Temperature



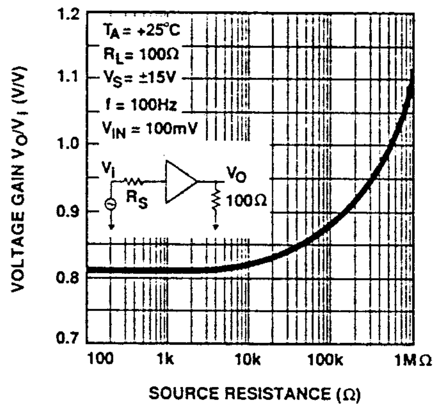
Supply Current vs Supply Voltage



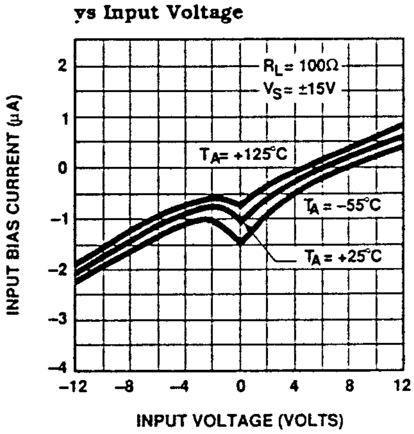
Voltage Gain vs Input Voltage



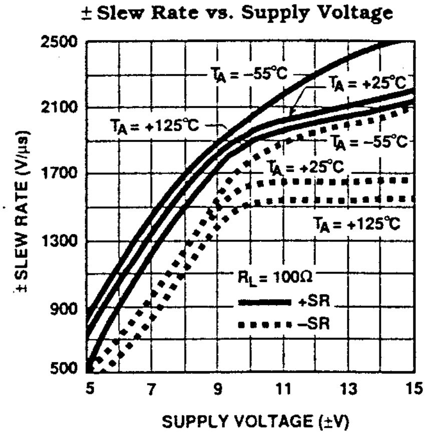
Voltage Gain vs Source Resistance



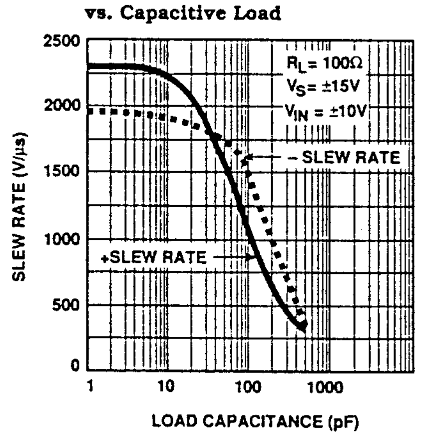
Input Bias Current vs Input Voltage



± Slew Rate vs. Supply Voltage

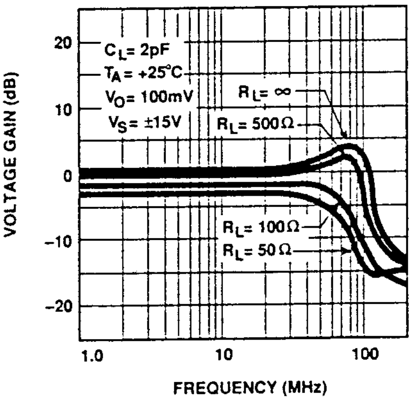


± Slew Rate vs. Capacitive Load

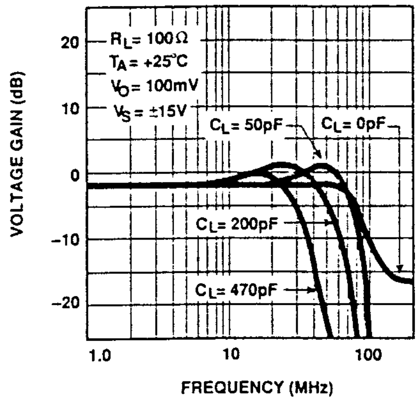


Typical Performance Curves — Continued

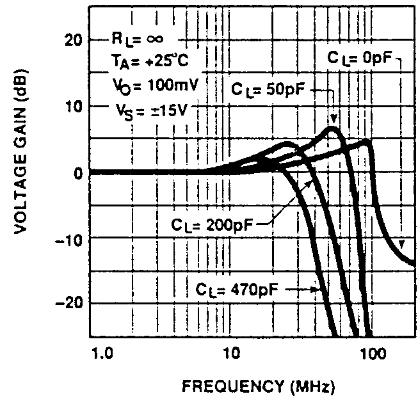
Voltage Gain vs Frequency for Various Resistive Loads



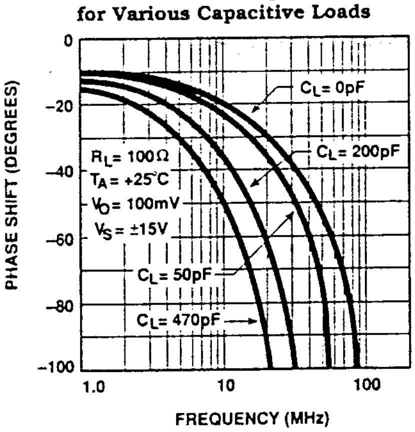
Voltage Gain vs Frequency for Various Capacitive Loads; R_L = 100 Ω



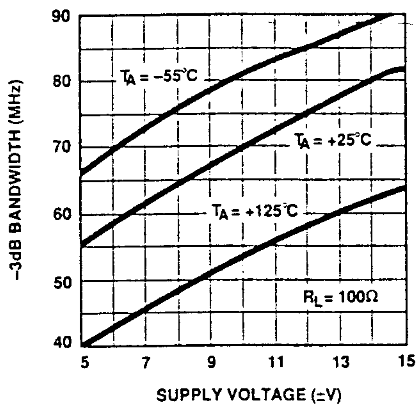
Voltage Gain vs Frequency for Various Capacitive Loads; R_L = ∞



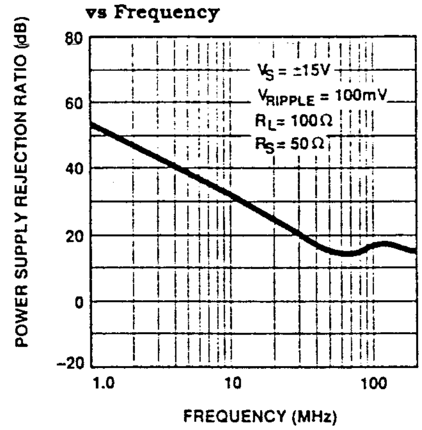
Phase Shift vs Frequency for Various Capacitive Loads



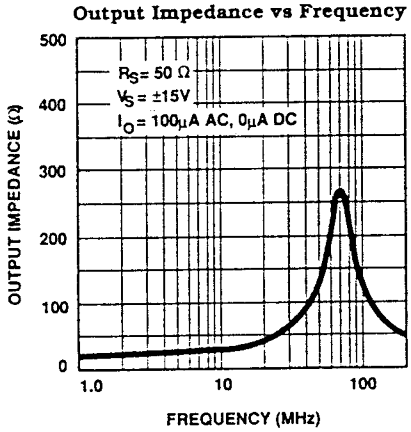
−3dB Bandwidth vs. Supply Voltage



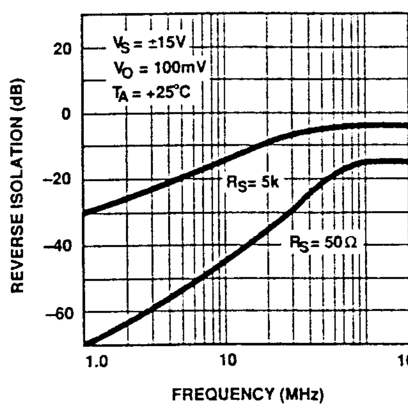
Power Supply Rejection Ratio vs Frequency



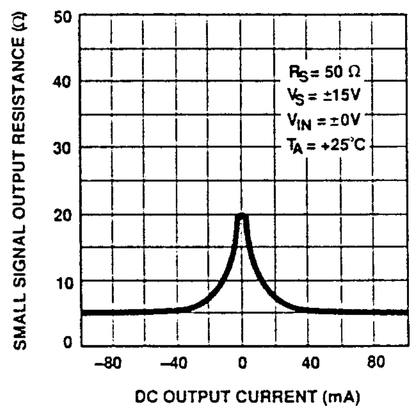
Output Impedance vs Frequency



Reverse Isolation vs Frequency

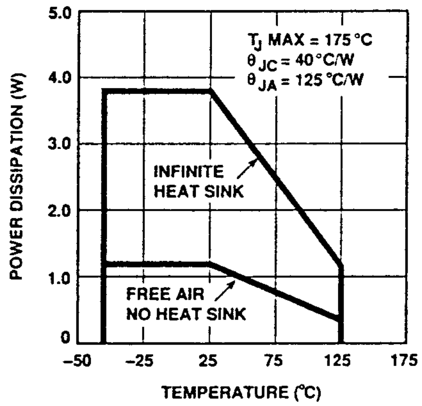


Small Signal Output Resistance vs Output Current

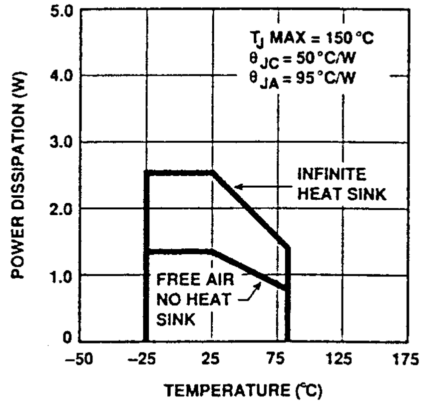


Typical Performance Curves — Continued

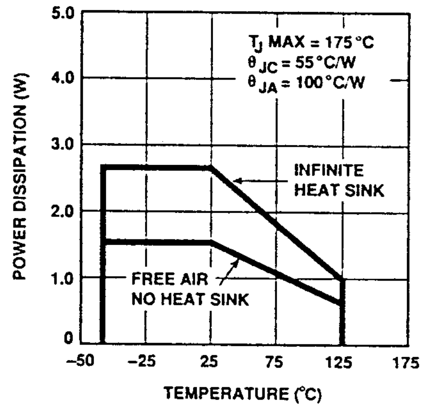
8-Lead CerDIP Maximum Power Dissipation vs Ambient Temperature



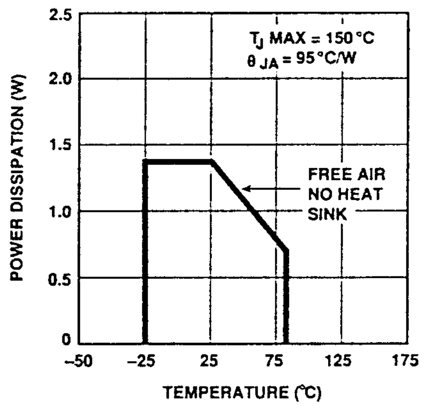
8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



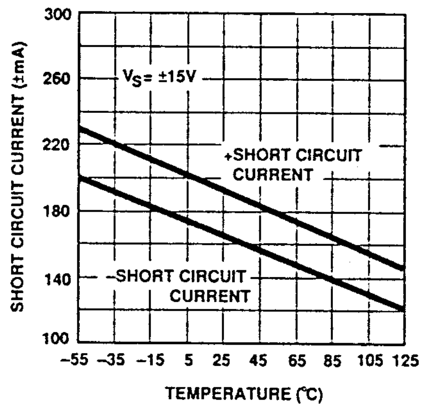
20-Pad LCC Maximum Power Dissipation vs Ambient Temperature



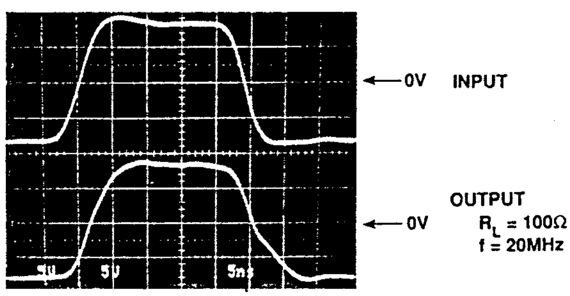
20-Lead SOL Maximum Power Dissipation vs Ambient Temperature



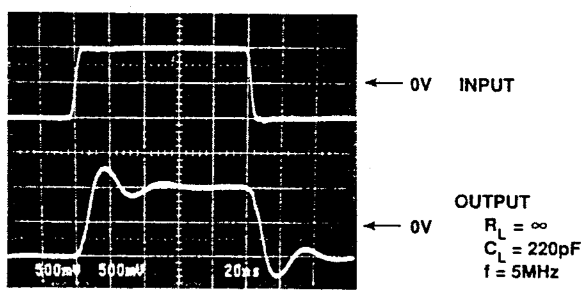
Short Circuit Current vs Temperature



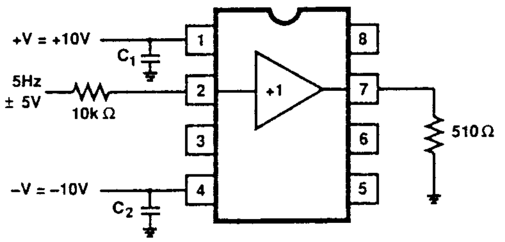
Large Signal Response



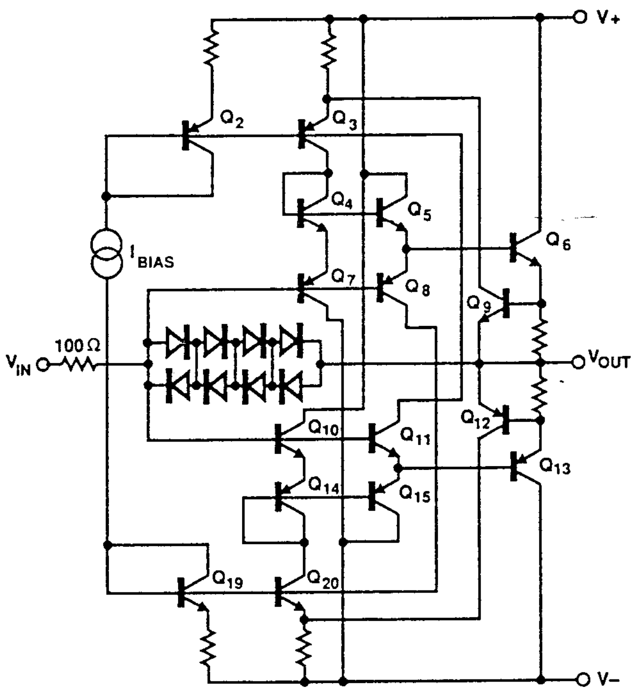
Small Signal Response



Burn-In Circuit



Simplified Schematic



Application Information

The EL2001 is a monolithic buffer amplifier built on Elantec's proprietary dielectric isolation process that produces NPN and PNP transistors with essentially identical DC and AC characteristics. The EL2001 takes full advantage of the complementary process with a unique circuit topology.

Elantec has applied for two patents based on the EL2001's topology. The patents relate to the base drive and feedback mechanism in the buffer. This feedback makes 2000 V/µs slew rates with 100 Ω loads possible with very low supply current.

Power Supplies

The EL2001 may be operated with single or split supplies with total voltage difference between 10 V (±5 V) and 36 V (±18 V). It is not necessary to use equal split value supplies. For example −5 V and +12 V would be excellent for signals from −2 V to +9 V.

Bypass capacitors from each supply pin to ground are highly recommended to reduce supply ringing and the interference it can cause. At a minimum, 1 µF tantalum capacitor with short leads should be used for both supplies.

Input Characteristics

The input to the EL2001 looks like a resistance in parallel with about 3.5 picofarads in addition to a DC bias current. The DC bias current is due to the miss-match in beta and collector current between the NPN and PNP transistors connected to the input pin. The bias current can be either positive or negative. The change in input current with input voltage (R_{in}) is affected by the output load, beta and the internal boost. R_{in} can actually appear negative over portions of the input range; typical input current curves are shown in the characteristic curves. Internal clamp diodes from the input to the output are provided. These diodes protect the transistor base emitter junctions and limit the boost current during slew to avoid saturation of internal transistors. The diodes begin conduction at about ±2.5 V input to output differential. When that happens the input resistance drops dramatically. The diodes are rated at 50 mA. When conducting they have a series resistance of about 20 ohms. There is also 100 ohms in series with the input that limits input current. Above +/−7.5 V differential input to output, additional series resistance should be added.

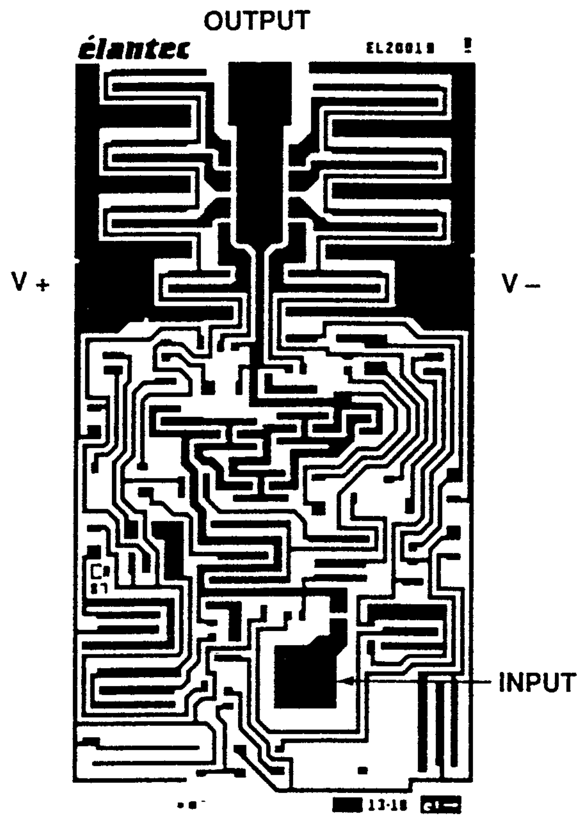
Source Impedance

The EL2001 has good input to output isolation. When the buffer is not used in a feedback loop, capacitive and resistive sources up to 1 Meg present no oscillation problems. Care must be used in board layout to minimize output to input coupling. CAUTION: When using high source impedances (R_s > 100 k ohms), significant gain errors can be observed due to output offset, load resistor, and the action of the boost circuit. See typical performance curves.

EL2001/EL2001C

Low Power, 70 MHz Buffer Amplifier

Die Layout



Die Size:
35 x 59 MILS^2

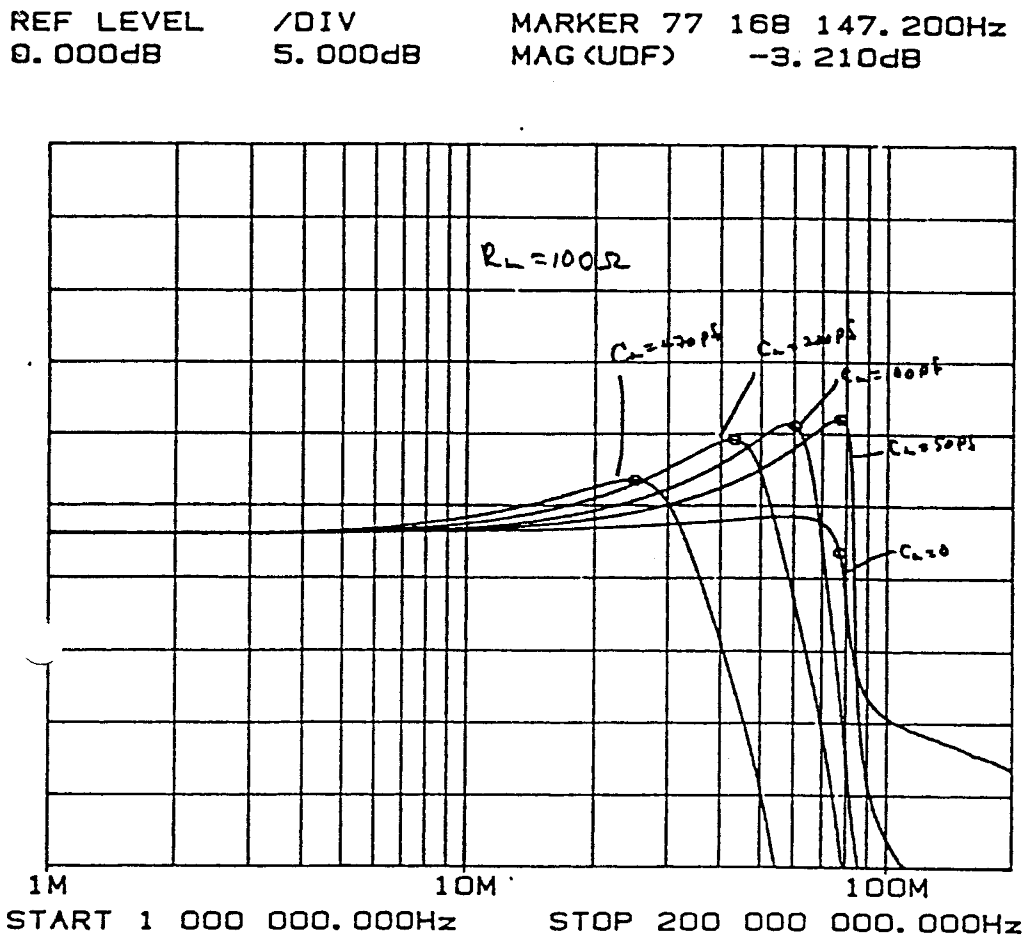
élantec

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

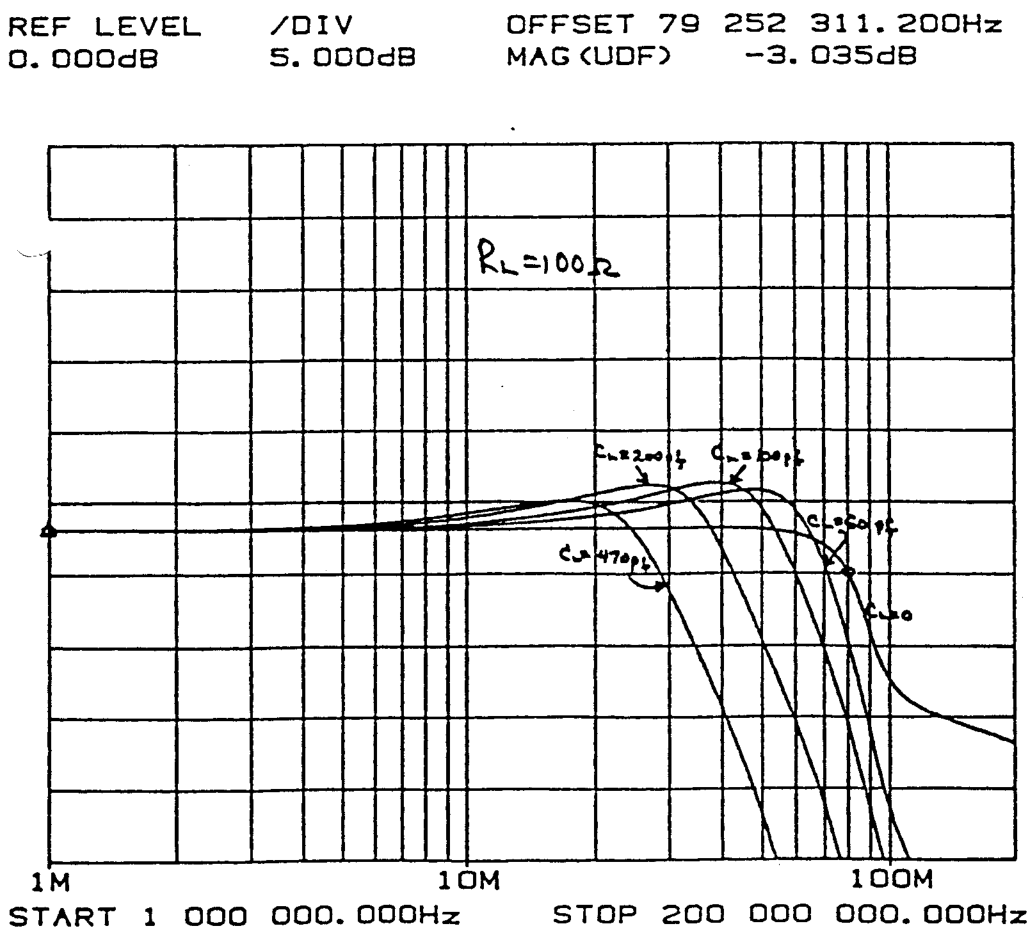
Elantec, Inc.
1996 Tarob Court
Milpitas, CA 95035
Telephone: (408) 945-1323
TWX: 910-997-0649
Fax: (408) 945-9305
800#—outside CA only:
800-821-7429

Printed in U.S.A.

EL2001



The plot on the left is of the early samples of the EL2001 date code 8851A. A change has been made in the design to reduce the peaking caused by capacitive loads.



The plot on the left shows the response of the current production EL2001. Note that the bandwidth is the same as the early parts but the peaking has been reduced.