élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2003/2003C/2033/2033C
100 MHz Video Line Driver

Features

- Differential gain 0.1%
- Differential phase 0.1°
- 100 mA continuous output current guaranteed
- Short circuit protected
- Wide bandwidth—100 MHz
- High slew rate—1200 V/μs
- High input impedance—2 MΩ
- Low quiescent current drain
- EL2003—Pin compatible with LH0002CN, LH0002H, HA2-5002
- EL2033—Pin compatible with HA3-5002, HA7-5002, HA3-5033, HA7-5033

Applications

- Co-ax cable driver
- Flash converter driver
- Video DAC buffer
- Op amp booster

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2003CJ	0°C to +75°C	CerDIP	MDP0010
EL2003CN	0°C to +75°C	P-DIP	MDP0031
EL2003CH	0°C to +75°C	TO-99	MDP0004
EL2003CM	0°C to +75°C	20-Lead SOL	MDP0027
EL2003H	−55°C to +125°C	TO-99	MDP0004
EL2003H/883B	−55°C to +125°C	TO-99	MDP0004
EL2003J	−55°C to +125°C	CerDIP	MDP0010
EL2003J/883B	−55°C to +125°C	CerDIP	MDP0010
EL2003L	−55°C to +125°C	20-PAD LCC	MDP0007
EL2003L/883B	−55°C to +125°C	20-PAD LCC	MDP0007
EL2033CN	0°C to +75°C	P-DIP	MDP0031
EL2033CJ	0°C to +75°C	CerDIP	MDP0010
EL2033J	−55°C to +125°C	CerDIP	MDP0010
EL2033J/883B	−55°C to +125°C	CerDIP	MDP0010

5962-89623 is the SMD version of this device.

General Description

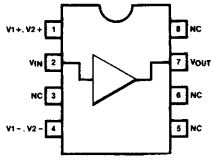
The EL2003/EL2033 are general purpose monolithic unity gain buffers featuring 100 MHz, −3 dB bandwidth and 4 ns small signal rise time. These buffers are capable of delivering a ±100 mA current to a resistive load and are oscillation free into capacitive loads. In addition, the EL2003/EL2033 have internal output short circuit current limiting which will protect the devices under both a DC fault condition and AC operation with reactive loads. The extremely fast slew rate of 1200 V/μs, wide bandwidth, and high output drive make the EL2003/EL2033 ideal choices for closed loop buffer applications with wide band op amps. These same characteristics and excellent DC performance make the EL2003/EL2033 excellent choices for open loop applications such as driving coaxial and twisted pair cables.

The EL2003/EL2033 are constructed using Elantec's proprietary dielectric isolation process that produces PNP and NPN transistors with essentially identical AC and DC characteristics.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, request our brochure: *Elantec's Military Processing—Monolithic Products.*

Connection Diagrams

EL2003, N, J Packages



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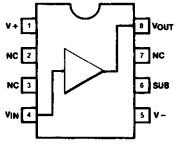
Top View

EL2033 N, J Packages



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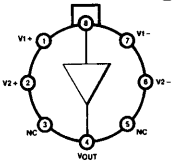
Top View

EL2003 H Package



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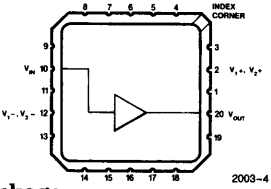
EL2003 L Package



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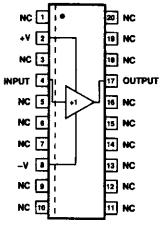
EL2003 M Package



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Absolute Maximum Ratings

V_S	Supply Voltage (V+ − V−)	±18V or 36V
V_{IN}	Input Voltage (Note 1)	±15V or V_S
I_{IN}	Input Current (Note 1)	±50 mA
P_D	Power Dissipation (Note 2)	See Curves
	Output Short Circuit Duration (Note 3)	Continuous
T_A	Operating Temperature Range	
	EL2003/2033	−55°C to +125°C
	EL2003C/2033C	0°C to +75°C
T_J	Operating Junction Temperature	
	Metal Can, CerDIP	175°C
	Plastic	150°C
T_{ST}	Storage Temperature	−65°C to +150°C
	Lead Temperature (Soldering, <10 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics V_S = ±15V, R_S = 50Ω

Parameter	Description	Test Conditions			Limits			Test Level		Units
		V_{IN}	Load	Temp	Min	Typ	Max	2003 2033	2003C 2033C	
V_{OS}	Output Offset Voltage	0	∞	25°C	−40	5	40	I	I	mV
				T_{MIN}, T_{MAX}	−50		50	I	III	mV
I_{IN}	Input Current	0	∞	25°C, T_{MAX}	−25	−5	25	I	II	μA
				T_{MIN}	−50		50	I	III	μA
R_{IN}	Input Resistance	±12V	100Ω	25°C, T_{MAX}	1	2		I	II	MΩ
				T_{MIN}	0.1			I	III	MΩ
A_{V1}	Voltage Gain	±12V	1 kΩ	25°C	0.98	0.99		I	I	V/V
				T_{MIN}, T_{MAX}	0.97			I	III	V/V
A_{V2}	Voltage Gain	±6V	50Ω	25°C	0.83	0.90		I	I	V/V
				T_{MIN}, T_{MAX}	0.80			I	III	V/V
A_{V3}	Voltage Gain with V_S = ±5V	±3V	50Ω	25°C	0.82	0.89		I	I	V/V
				T_{MIN}, T_{MAX}	0.79			I	III	V/V
V_{O1}	Output Voltage Swing	±14V	1 kΩ	25°C	±13	±13.5		I	I	V
				T_{MIN}, T_{MAX}	±12.5			I	III	V
V_{O2}	Output Voltage Swing	±12V	100Ω	25°C	±10.5	±11.3		I	I	V
				T_{MIN}, T_{MAX}	±10			I	III	V

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Electrical Characteristics $V_S = \pm 15V, R_S = 50\Omega$ — Contd.

Parameter	Description	Test Conditions			Limits			Test Level		Units
		V_{IN}	Load	Temp	Min	Typ	Max	2003 2033	2003C 2033C	
R_{OUT}	Output Resistance	±2V	50Ω	25°C		7	10	I	I	Ω
				T_{MIN}, T_{MAX}			12	I	III	Ω
I_{OUT}	Output Current	±12V	(Note 4)	25°C	±105	±230		I	I	mA
				T_{MIN}, T_{MAX}	±100			I	III	mA
I_S	Supply Current	0	∞	25°C, T_{MAX}		10	15	I	II	mA
				T_{MIN}			20	I	III	mA
PSRR	Supply Rejection, (Note 5)	0	∞	25°C	60	80		I	I	dB
				T_{MIN}, T_{MAX}	50			I	III	dB
SR1	Slew Rate, (Note 6)	±10V	1 kΩ	25°C	600	1200		I	I	V/µs
SR2	Slew Rate, (Note 7)	±5V	50Ω	25°C	200	400		I	I	V/µs
THD	Distortion @ 1 kHz	4 V_{rms}	50Ω	25°C		0.2	1	I	I	%

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input to output voltage exceeds ±7.5V then the input current must be limited to ±50 mA. See the application hints for more information.

Note 2: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.

Note 3: A heat sink is required to keep the junction temperature below the absolute maximum when the output is short circuited.

Note 4: Force the input to +12V and the output to +10V and measure the output current. Repeat with −12V in and −10V on the output.

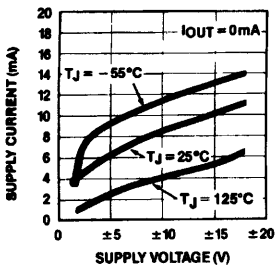
Note 5: $V_S = \pm 4.5V$ to ±18V.

Note 6: Slew rate is measured between $V_{OUT} = +5V$ and −5V.

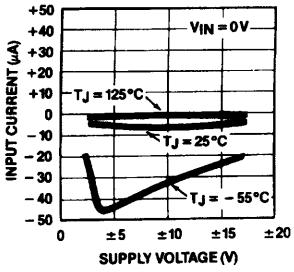
Note 7: Slew rate is measured between $V_{OUT} = +2.5V$ and −2.5V.

Typical Performance Curves

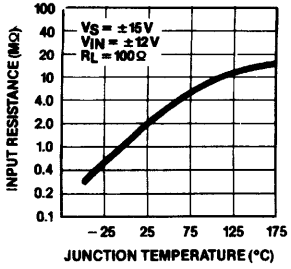
Quiescent Supply Current vs Supply Voltage



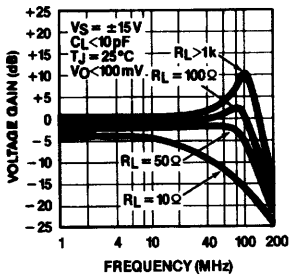
Input Current vs Supply Voltage



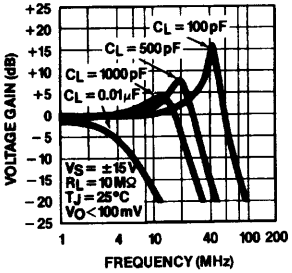
Input Resistance vs Temperature



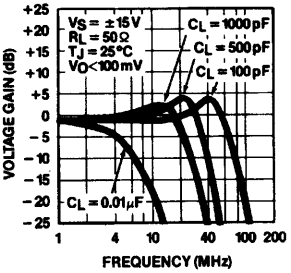
Voltage Gain vs Frequency Various Resistive Loads



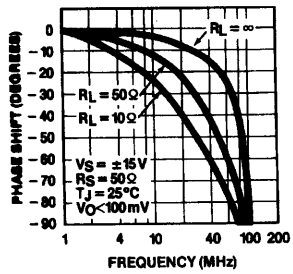
Voltage Gain vs Frequency No Resistive Load Various Capacitive Loads



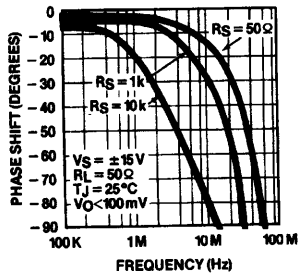
Voltage Gain vs Frequency 50Ω Resistive Load Various Capacitive Loads



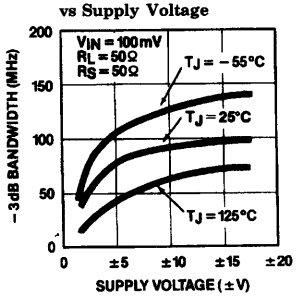
Phase Shift vs Frequency Various Resistive Loads



Phase Shift vs Frequency Various Source Resistors



−3 dB Bandwidth vs Supply Voltage



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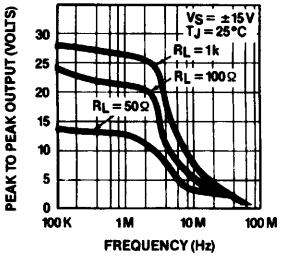
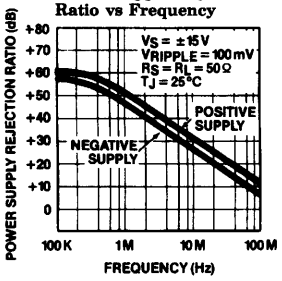
Typical Performance Curves — Contd.

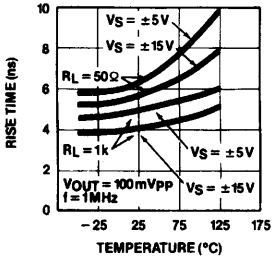
Maximum Undistorted Output Voltage vs Frequency



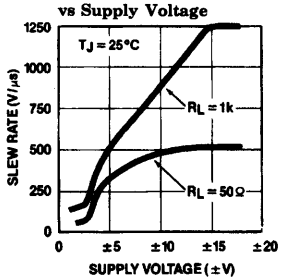
Power Supply Rejection Ratio vs Frequency



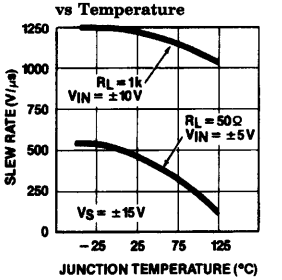
Rise Time vs Temperature



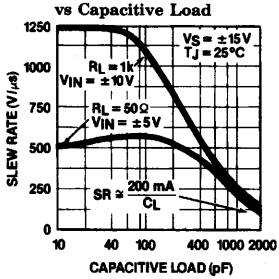
Slew Rate vs Supply Voltage



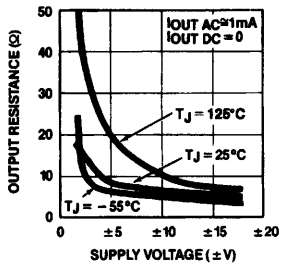
Slew Rate vs Temperature



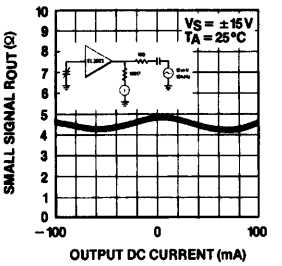
Slew Rate vs Capacitive Load



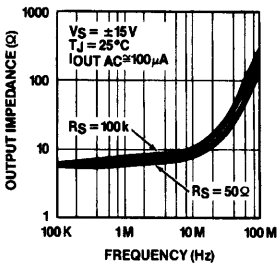
Output Resistance vs Supply Voltage



Small Signal Output Resistance vs DC Output Current



Output Impedance vs Frequency



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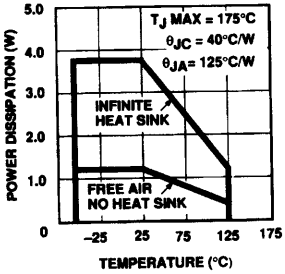
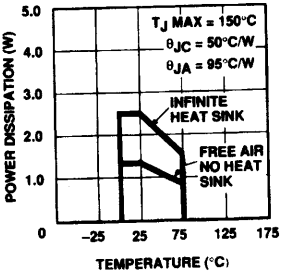
Typical Performance Curves — Contd.

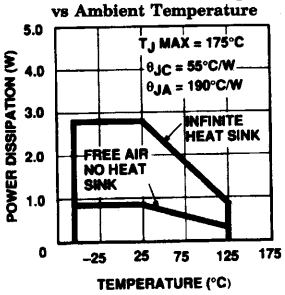
8-Lead CerDIP Maximum Power Dissipation vs Ambient Temperature



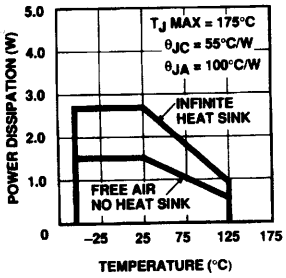
8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



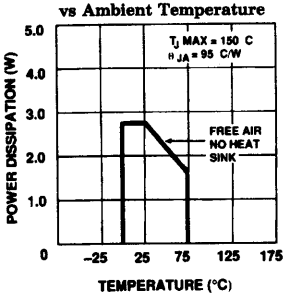
8-Lead TO-99 Metal Can Maximum Power Dissipation vs Ambient Temperature



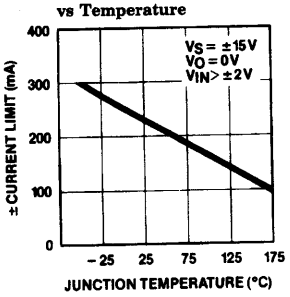
20-Pad LCC Maximum Power Dissipation vs Ambient Temperature



20-Lead SOL Maximum Power Dissipation vs Ambient Temperature



Current Limit vs Temperature



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EL2003/2003C/2033/2033C
100 MHz Video Line Driver

Applications Hints

The EL2003/EL2033 are monolithic buffer amplifiers built with Elantec's proprietary dielectric isolation process that produces NPN and PNP complimentary transistors. The circuits are connection of symmetrical common collector transistors that provide both sink and source current capability independent of output voltage while maintaining constant output and input impedances. The high slew rate and wide bandwidth of the EL2003 and EL2033 make them useful beyond video frequencies.

Power Supplies

The EL2003/EL2033 may be operated with single or split supplies as low as ±2.5V (5V total) to as high as ±18V (36V total). However, the bandwidth, slew rate and output impedance degrade significantly for supply voltages less than ±5V (10V total) as shown in the characteristic curves. It is not necessary to use equal value split supplies, for example −5V and +12V would be excellent for 0V to 1V video signals.

Bypass capacitors from each supply pin to a ground plane are recommended. The EL2003/EL2033 will not oscillate even with minimal bypassing, however, the supply will ring excessively with inadequate capacitance. To eliminate a supply ringing and the interference it can cause, a 10 μF tantalum capacitor with short leads is recommended for both supplies. Inadequate supply bypassing can also result in lower slew rates and longer settling times.

The EL2003 metal can package has the collectors of the output transistors brought out separately from the input supplies for pin compatibility with the ELH0002H. If the collectors operate on lower supplies than the input stage, the internal power dissipation can be reduced. However, the output transistors can be driven into hard saturation when the input voltage exceeds the collector supply voltage. The recovery time to come out of saturation will be 2 μs or 3 μs and the output may oscillate during this recovery period.

Input Range

The input to the EL2003/EL2033 looks like a high resistance in parallel with a few picofarads in addition to a DC bias current. The input characteristics change very little with output loading, even when the amplifier is in current limit. However, there are clamp diodes from the input to the output that protect the transistor base emitter junctions. These diodes start to conduct at about ±9.5V input to output differential voltage. Of course the input resistance drops dramatically when the diodes start conducting; the diodes are rated at ±50 mA.

The input characteristics also change when the input voltage exceeds either supply by 0.5V. This happens because the input transistor's base-collector junctions forward bias. If the input exceeds the supply by LESS than 0.5V and then returns to the normal input range, the output will recover in less than 10 ns. However, if the input exceeds the supply by MORE than 0.5V, the recovery time can be 100's of nanoseconds. For this reason it is recommended that schottky diode clamps from input to supply be used if a fast recovery from large input overloads is required.

Source Impedance

The EL2003/EL2033 have excellent input-output isolation and are very tolerant of variations in source impedances. Capacitive sources cause no problems at all, resistive sources up to 100 kΩ present no problems as long as care is used in board layout to minimize output to input coupling. Inductive sources can cause oscillations; a 1 kΩ resistor in series with the buffer input lead will usually eliminate problems without sacrificing too much speed. An unterminated cable or other resonant source can also cause oscillations. Again, an isolating resistor will eliminate the problem.

Current Limit

The EL2003/EL2033 have internal current limits that protect the output transistors. The current limit goes down with junction temperature rise as shown in the characteristic curves. At a junction temperature of +175°C the current limits are at about 100 mA. If the EL2003 or EL2033 output is shorted to ground when operating on ±15V supplies, the power dissipation will be greater than 1.5W. A heat sink is required in order for the EL2003 or EL2033 to survive an indefinite short. Recovery time to come out of current limit is about 250 ns.

Applications Hints — Contd.

Heat Sinking

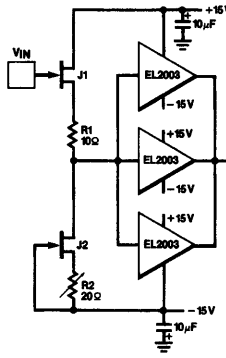
When operating the EL2003/EL2033 in elevated ambient temperatures and/or high supply voltages and low impedance loads, the internal power dissipation can force the junction temperature above the maximum rating (175°C for the metal can package and 150°C for the plastic DIP). Also, an indefinite short of the output to ground will cause excessive power dissipation.

The thermal resistance junction to case is 55°C per Watt for the metal can package and 50°C/W for the plastic DIP. A suitable heat sink will increase the power dissipation capability significantly beyond that of the package alone. Several companies make standard heat sinks for both packages. Aavid and Thermalloy heat sinks have been used successfully.

Parallel Operation

If more than 100 mA output is required or if heat management is a problem, several EL2003s or EL2033s may be paralleled together. The result is as though each device was driving only part of the load. For example, if two units are paralleled then a 50Ω load looks like 100Ω to each EL2003. Parallel operation results in lower input and output impedances, increased bias current but no increase in offset voltage. An example showing three EL2003s in parallel and also the addition of a FET input buffer stage is shown below. By using a dual FET the circuit complexity is minimal and the performance is excellent. Take care to minimize the stray capacitance at the input of the EL2003s for maximum slew rate and bandwidth.

FET Input Buffer with High Output Currents



Parallel Operation
$I_{OUT} \geq \pm 300$ mA
$R_{OUT} \cong 2\Omega$
BW ≅ 100 MHz
SR = 1000 V/µs

J1, J2 2N5911 Dual FET
R1, R2 Offset Adjust

2003-9

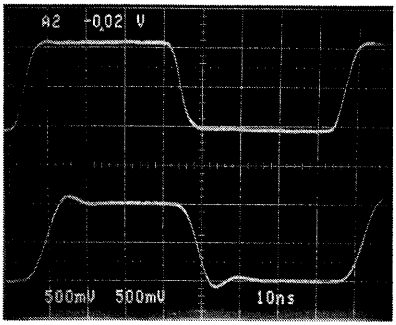
Resistive Loads

The DC gain of the EL2003/EL2033 is the product of the unloaded gain (0.995) and the voltage divider formed by the device output resistance and the load resistance.

$$A_V = 0.995 * R_L/(R_L + R_{OUT})$$

The high frequency response of the EL2003/EL2033 varies with the value of the load resistance as shown in the characteristic curves. If the 100 MHz peaking is undesirable when driving load resistors greater than 50Ω, an RC snubber circuit can be used from the output to ground. The snubber circuit works by presenting a high frequency load resistance of less than 50Ω while having no loading effect at low frequencies.

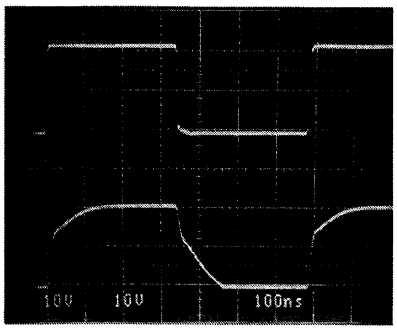
Small Signal Response



$R_L = 50\Omega$, $C_L = 10$ pF, $V_S = \pm 15$V
Top is V_{IN}, Bottom is V_{OUT}

2003-10

Large Signal Response



$R_L = 100\Omega$, $C_L = 10$ pF, $V_S = \pm 15$V
Top is V_{IN}, Bottom is V_{OUT}

2003-11

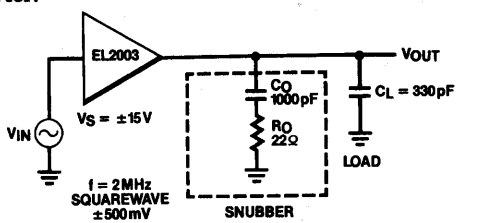
EL2003/2003C/2033/2033C
100 MHz Video Line Driver

Applications Hints — Contd.

Capacitive Loads

The EL2003/EL2033 are stable driving any type of capacitive load. However, when driving a pure capacitance of less than a thousand picofarads the frequency response has excessive peaking as shown in the characteristic curves. The squarewave response will have large overshoots and will ring for several hundred ns.

If the peaking and ringing cause system problems they can be eliminated with an RC snubber circuit from the output to ground. The values can be found empirically by observing a squarewave or the frequency response. First just put the resistor alone from output to ground until the desired response is obtained. Of course the gain will be reduced due to R_{OUT}. Then put capacitance in series with the resistor to restore the gain at low frequencies. Start with a small capacitor and increase until the response is optimum. Too large a capacitor will roll the gain off prematurely and result in a longer settling time. The figure below shows an example of an EL2003 driving a 330 pF load, which is similar to the input of a flash converter.



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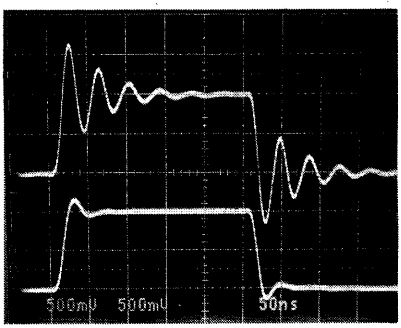
Driving a Pure Capacitance



Top Trace is without Snubber.
Bottom Trace is with Snubber Circuit.

2003-13

Inductive Loads

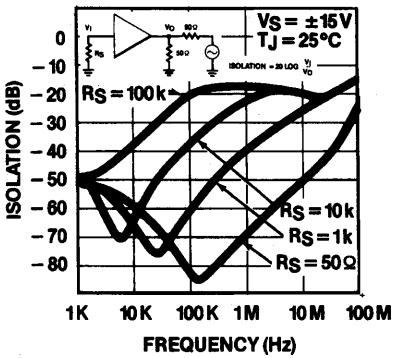
The EL2003/EL2033 can drive small motors, solenoids, LDT's and other inductive loads. Foldback current limiting is NOT used in the EL2003 or EL2033 and current limiting into an inductive load does NOT in and of itself cause spikes or kickbacks. However, if the EL2003 or EL2033 is in current limit and the input voltage is changing quickly (i.e., a squarewave) the inductive load can kick the output beyond the supply voltage. Motors are also able to generate kickbacks when the EL2003 or EL2033 is in current limit.

To prevent damage to the EL2003/EL2033 when the output kicks beyond the supplies it is recommended that catch diodes be placed from each supply to the output.

Reverse Isolation

The EL2003/EL2033 have excellent output to input isolation over a wide frequency range. This characteristic is very important when the buffer is used to drive signals between different equipment over cables. Often the cable is not perfect or the termination is improper and reflections occur that act like a signal source at the output of the buffer. Worst case the cable is connected to a source instead of where it is supposed to go. In both situations the buffer must keep these signals from its input. The following curve shows the reverse isolation of the EL2003/EL2033 verses frequency for various source resistors.

Reverse Isolation vs. Frequency



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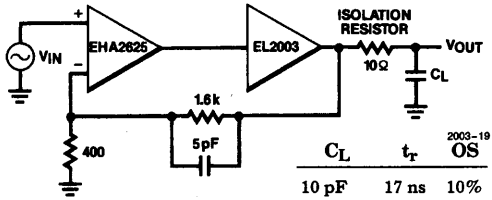
EL2003/2003C/2033/2033C
100 MHz Video Line Driver

Applications Hints — Contd.

Driving capacitive loads with any closed loop amplifier creates special problems. The open loop output impedance works into the load capacitance to generate phase lag which can make the loop unstable. The output impedance of the EL2003 or EL2033 is less than 10Ω from DC to about 10 MHz, but a capacitive load of 1000 pF will generate about 45 degrees phase shift at 10 MHz and make high speed op amps unstable. Obviously more capacitance will cause the same problem but at lower frequencies, and slower op amps as well would become unstable.

The easiest way to drive capacitive loads is to isolate them from the feedback with a series resistor. Ten to twenty ohms is usually enough but the final value depends on the op amp used and the range of load capacitance.

Op Amp Booster with Capacitive Load



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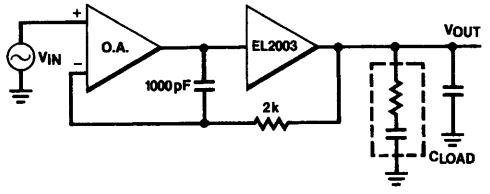
C_L	t_r	OS
10 pF	17 ns	10%
470 pF	20 ns	50%
0.001 μF	30 ns	35%
0.005 μF	80 ns	0
0.01 μF	220 ns	0
0.05 μF	1.1 μs	0
0.1 μF	2.2 μs	0

10Ω is enough isolation and speed is determined by the isolation resistor and capacitive load time constant.

If the system requirements will not tolerate the isolation resistor, then additional high frequency feedback from the op amp output (the buffer input) and an isolating resistor from the buffer output is required. This requires that the op amp be unity gain stable.

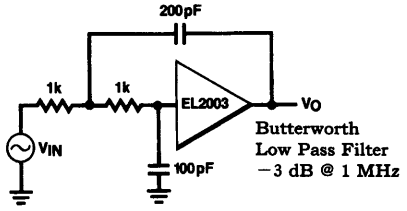
Complex Feedback with the Buffer to Drive Capacitive Loads



2003-20

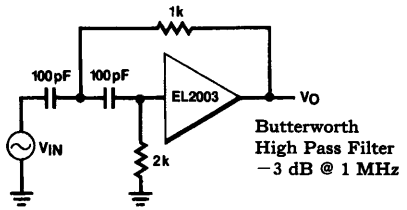
This works with any unity gain stable OA. Snubber Circuit (51Ω 470 pF) is optional.

Typical Applications



Butterworth Low Pass Filter −3 dB @ 1 MHz

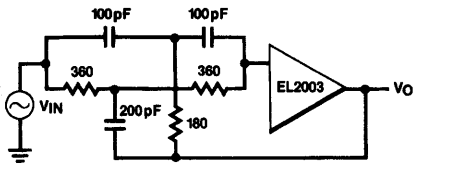
2003-21



Butterworth High Pass Filter −3 dB @ 1 MHz

2003-22

High Q Notch Filter



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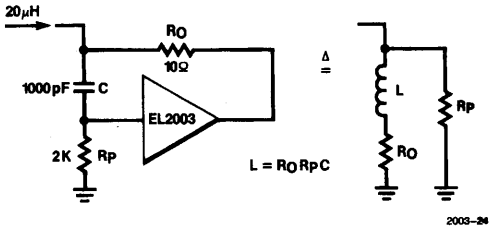
$$f_O = \frac{1}{2\pi\,(100\text{ pF})\,(360)} \approx 4.4\text{ MHz}$$

Simulated Inductor



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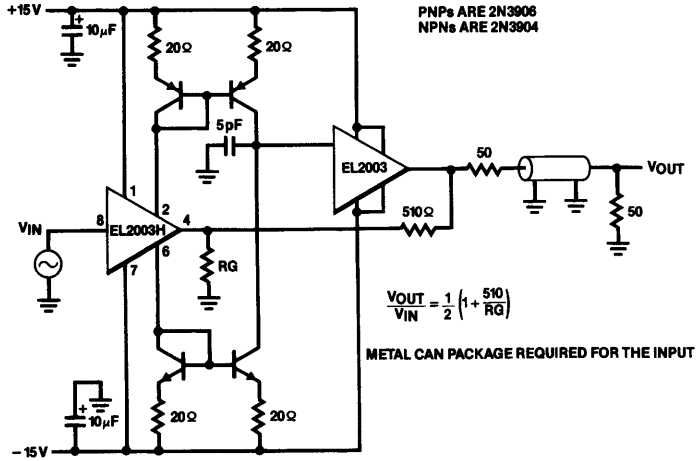
Typical Applications — Contd.

Turbo Amplifier, BW = 30 MHz for Gains from 1 to 5



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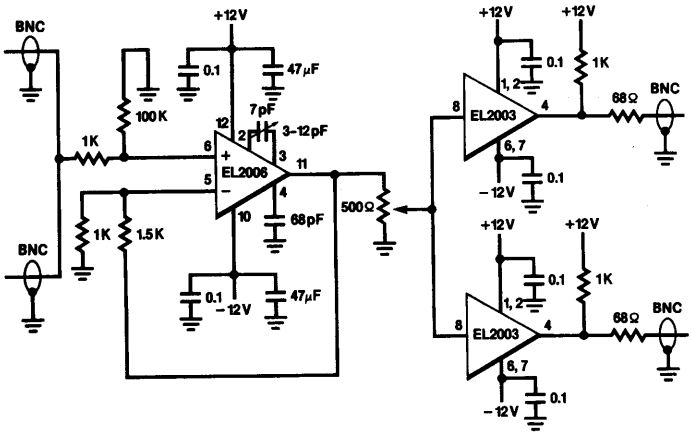
Video Distribution Amplifier

In this broadcast quality circuit, the EL2006 FET input amplifier provides a very high input impedance so that it may be used with a wide variety of signal sources including video DACs, CCD cameras, video switches or 75Ω cables. The EL2006 provides a voltage gain of 2.5 while the potentiometer allows the overall gain to be adjusted to drive the standard signal levels into the back matched 75Ω cables. Back matching prevents multiple reflections in the event that the remote end of the cable is not properly terminated. The 1k pull up resistors reduce the differential gain error from 0.15% to less than 0.1%.

Video Distribution Amplifier



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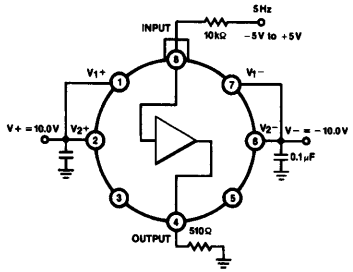
EL2003/2003C/2033/2033C
100 MHz Video Line Driver

Burn-In Circuits

EL2003 Metal Can



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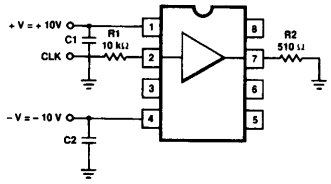
EL2003 DIP



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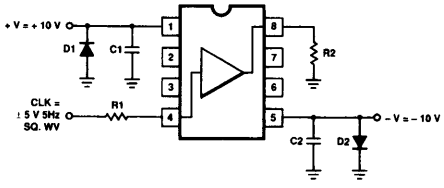
EL2033 DIP



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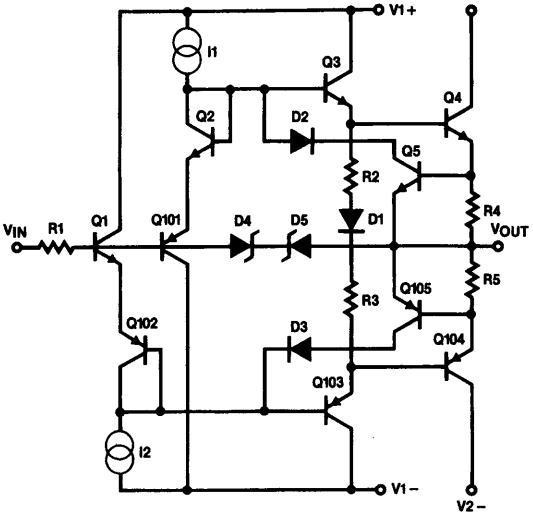
Simplified Schematic



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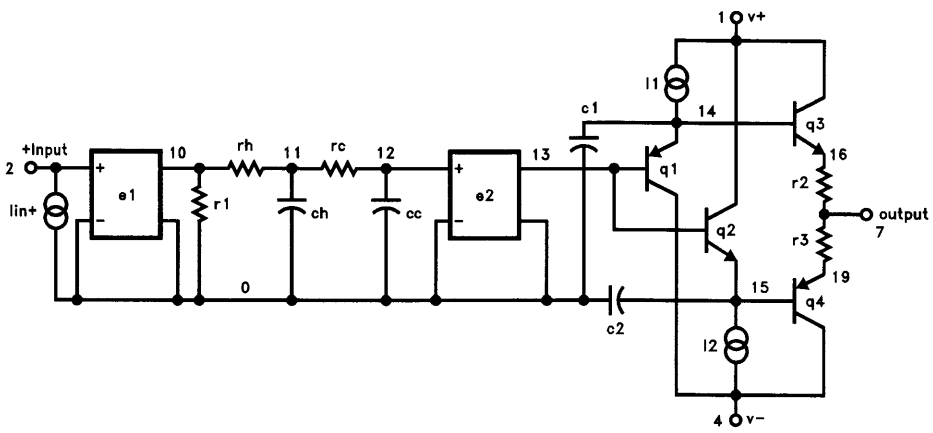
Clip!

EL2003 Macromodel

```
* Connections:      + input
*                   |     + Vsupply
*                   |     |     - Vsupply
*                   |     |     |     output
*                   |     |     |     |
.subckt M2003       2     1     4     7
* Input Stage
e1 10 0 2 0 1.0
r1 10 0 1K
rh 10 11 150
ch 11 0 10pF
rc 11 12 100
cc 12 0 3pF
e2 13 0 12 0 1.0
* Output Stage
q1 4 13 14 qp
q2 1 13 15 qn
q3 1 14 16 qn
q4 4 15 19 qp
r2 16 7 5
r3 19 7 5
c1 14 0 3pF
c2 15 0 3pF
i1 1 14 3mA
i2 15 4 3mA
* Bias Current
iin + 2 0 5uA
* Models
.model qn npn(is = 5e - 15 bf = 150 rb = 350 ptf = 45 cjc = 2pF tf = 0.3nS)
.model qp pnp(is = 5e - 15 bf = 150 rb = 350 ptf = 45 cjc = 2pF tf = 0.3nS)
.ends
```

EL2003 Macromodel — Contd.



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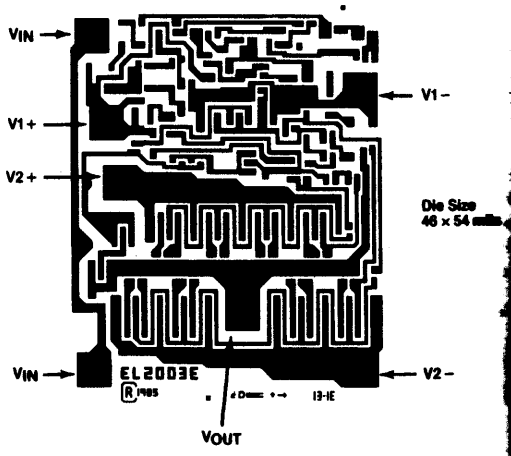
EL2003D Die
100 MHz Video Line Driver

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage (V+ – V–)	±18V or ±36V
V_{IN}	Input Voltage (Note 1)	±15V or V_S
I_{IN}	Input Current (Note 1)	±50 mA
	Output Short Circuit Duration (Note 3)	Continuous
T_J	Maximum Junction Temperature	175°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



DC Electrical Characteristics V_S = ±15V, R_S = 50Ω, T_A = 25°C

Parameter	Description	Test Conditions		Limits			Test Level	Units
		V_{IN}	Load	Min	Typ	Max		
V_{OS}	Output Offset Voltage	0	∞	–40	5	40	I	mV
I_{IN}	Input Current	0	∞	–25		25	I	µA
R_{IN}	Input Resistance	±12V	100Ω	1	2		I	MΩ
A_{V1}	Voltage Gain	±12V	1 kΩ	0.98	0.99		I	V/V
A_{V2}	Voltage Gain	±6V	50Ω	0.83	0.90		I	V/V
A_{V3}	Voltage Gain, V_S = ±15V	±3V	50Ω	0.82	0.89		I	V/V
V_{O1}	Output Voltage Swing	±14V	1 kΩ	±13	±13.5		I	V
V_{O2}	Output Voltage Swing	±12V	100Ω	±10.5	±11.3		I	V
R_{OUT}	Output Resistance	±2V	50Ω		7	10	I	Ω
I_{OUT}	Output Current	±12V	(Note 2)	±105	±230		I	mA
I_S	Supply Current	0	∞		10	15	I	mA
PSRR	Supply Rejection (Note 3)	0	∞	60	80		I	dB

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input to output voltage exceeds ±7.5V then the input current must be limited to ±50 mA. See the application hints for more information.

Note 2: Force the input to +12V and the output to +10V and measure the output current. Repeat with –12V in and –10V out output.

Note 3: V_S = ±4.5V to ±18V.