élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2012
Closed Loop Buffer

Features

- 80 MHz bandwidth with 50Ω load
- 250 mA output current
- Gain = 0.999+ with 50Ω load
- V_{OS} ±4 mV
- Short circuit protected
- Power package with isolated metal tab

Applications

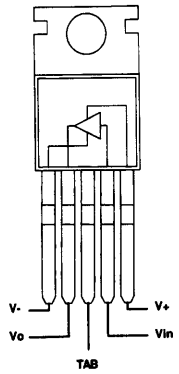
- Line driver
- Data acquisition
- Current booster
- Sample and holds

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2012CT	0°C to +75°C	TO-220	MDP0028

Connection Diagram

5-Pin TO-220



2012-5

Top View

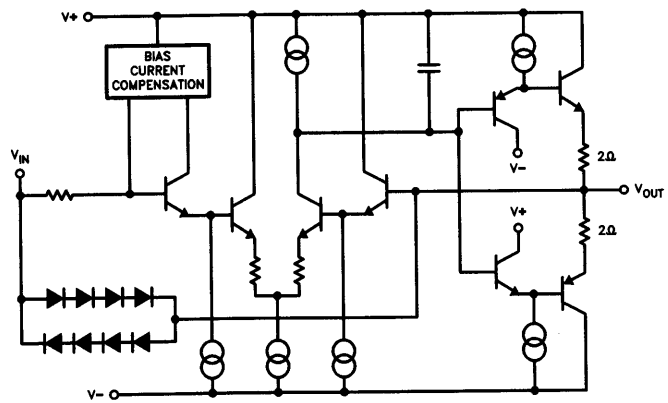
General Description

The EL2012 is a high speed bipolar monolithic buffer designed to provide 250 mA output current. This is two or more times the load driving capability of most other monolithic buffers. At the same time the closed loop topology of the EL2012 overcomes the gain accuracy problems of most other buffers. In many applications the high gain accuracy will eliminate the need for an op amp to compensate for the buffer losses. The EL2012 has output short circuit current limiting which will protect the device under both a DC fault condition and AC operation with reactive loads.

The EL2012 is constructed using Elantec's proprietary Complementary Bipolar process that produces PNP and NPN transistors with essentially identical AC and DC characteristics. In the EL2012 the Complementary Bipolar process also insulates the package's metal heat sink tab from all supply voltages. Therefore, the tab may be mounted to an external heat sink or the chassis without an insulator.

The EL2012 is specified for operation over the 0°C to +75°C temperature range and is provided in a 5-lead TO-220 plastic power package.

Simplified Schematic



2012-1

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage (V+ − V−)	±18V or 36V	T_A	Operating Temperature Range	0°C to +75°C
V_{IN}	Input Voltage (Note 1)	±15V or Vs	T_J	Operating Junction Temp.	175°C
I_{IN}	Input Current (Note 1)	±50 mA	T_{ST}	Storage Temp. Range	−65°C to +150°C
P_D	Power Dissipation (Note 2)	See Table	T_{LD}	Lead Solder Temp. <10 Sec.	300°C
t_{SH}	Output Short Circuit Duration (Note 3)	Continuous			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15.0V, R_S = 50Ω, unless otherwise specified

Parameter	Description	Test Conditions			Limits			Test Level	Units
		V_{IN}	Load	Temp	Min	Typ	Max		
V_{OS}	Output Offset Voltage	0V	∞	25°C	−4	0	+4	I	mV
				T_{MIN}, T_{MAX}	−4		+4	IV	mV
I_{IN}	Input Current	0V	∞	25°C	−1	1	+2	I	µA
				T_{MIN}, T_{MAX}	−1	1	+3	IV	µA
R_{IN}	Input Resistance	±12V	50Ω	25°C	10	20		I	MΩ
				T_{MIN}, T_{MAX}	10	20		IV	MΩ
A_{V1}	Voltage Gain	±12V	∞	25°C	0.999	0.9993		I	V/V
				T_{MIN}, T_{MAX}	0.999	0.9993		IV	V/V
A_{V2}	Voltage Gain	±10V	50Ω	25°C	0.999			I	V/V
				T_{MIN}, T_{MAX}	0.999			IV	V/V
V_{O1}	Output Voltage Swing	±14V	∞	25°C	−12.5, +13			I	V
				T_{MIN}, T_{MAX}		±13		V	V
V_{O2}	Output Voltage Swing	±12V	50Ω	25°C	±11.5	±11.99		I	V
				T_{MIN}, T_{MAX}	±11	±11.8		IV	V
I_{OUT}	Output Current	±12V (Note 4)	—	25°C	±225	±350		I	mA
				T_{MIN}, T_{MAX}	±200	±300		IV	mA
I_S	Supply Current	0V	∞	25°C	13	17	21	I	mA
				T_{MIN}, T_{MAX}	12		22	IV	mA
PSRR	Supply Rejection	0V (Note 5)	50Ω	25°C	70	85		I	dB
				T_{MIN}, T_{MAX}	65			IV	dB

EL2012
Closed Loop Buffer

DC Electrical Characteristics $V_S = \pm 15.0V$, $R_S = 50\Omega$, unless otherwise specified — Contd.

Parameter	Description	Test Conditions			Limits			Test Level	Units
		V_{IN}	Load	Temp	Min	Typ	Max		
SSEN	Supply Sensitivity	0V (Note 6)	50Ω	25°C	60	66		I	dB
				T_{MIN}, T_{MAX}	60			IV	dB
θ_{JC}	Infinite Heat Sink					4		V	C°/W
θ_{JA}	Free Air					65		V	C°/W

AC Electrical Characteristics $V_S = \pm 15.0V$, $R_S = 50\Omega$, unless otherwise specified

Parameter	Description	Test Conditions			Limits			Test Level	Units
		V_{IN}	Load	Temp	Min	Typ	Max		
SR	Slew Rate	±10V (Note 7)	50Ω	25°C	200			I	V/μs
				T_{MIN}, T_{MAX}	180			IV	V/μs
THD	Distortion @1 kHz	4 Vrms	50Ω	25°C		0.04	0.08	I	%
BW	−3 dB Bandwidth	100 mV	50Ω	25°C		100		V	MHz
C_{IN}	Input Capacitance			25°C		5		V	pF
t_{PD}	Propagation Delay	100 mV	50Ω	25°C		6		V	ns
t_r, t_f	Rise and Fall Time	100 mV		25°C		5		V	ns

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input to output voltage exceeds ±7.5V then the input current must be limited to ±50 mA. See the applications section for more information.

Note 2: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.

Note 3: A heat sink is required to keep the junction temperature below the absolute maximum when the output is short circuited.

Note 4: Force the input to +12V and the output to +10V and measure the output current. Repeat with −12 V_{IN} and −10V on the output.

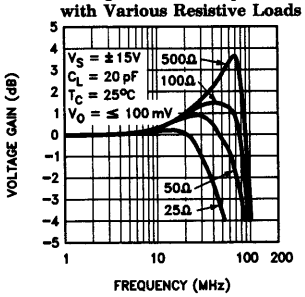
Note 5: V_{OS} is measured at $V_S+ = +4.5V$, $V_S- = -4.5V$ and at $V_S+ = +18V$, $V_S- = +18V$. Both supplies are changed simultaneously.

Note 6: $V_S+ = +15V$, $V_S- = -4.5V$ then V_S- is changed to −18V and $V_S- = -15V$, $V_S+ = +4.5V$ then V_S+ is changed to +18V.

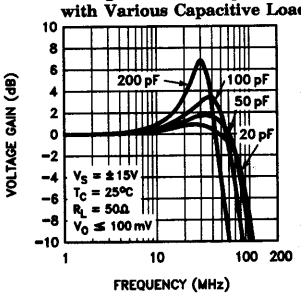
Note 7: Slew rate is measured between $V_{OUT} = +5V$ and −5V. V_{IN} slew rate = 400 V/μs.

Typical Performance Curves

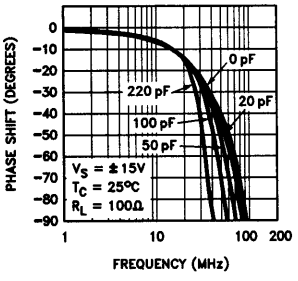
Voltage Gain vs Frequency with Various Resistive Loads



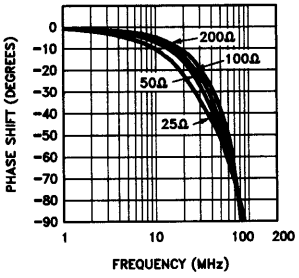
Voltage Gain vs Frequency with Various Capacitive Loads



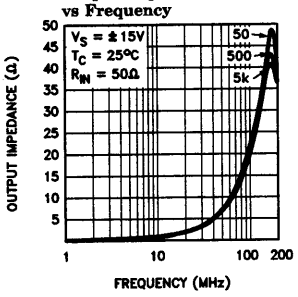
Phase Shift vs Frequency with Various Capacitive Loads



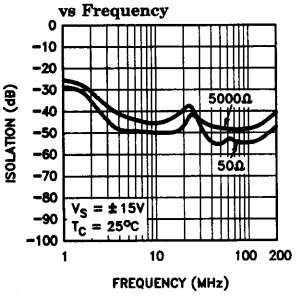
Phase Shift vs Frequency with Various Resistive Loads



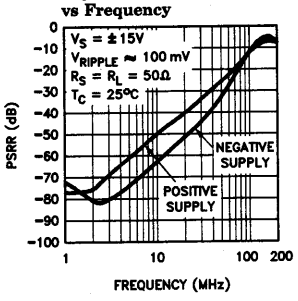
Output Impedance vs Frequency



Reverse Isolation vs Frequency



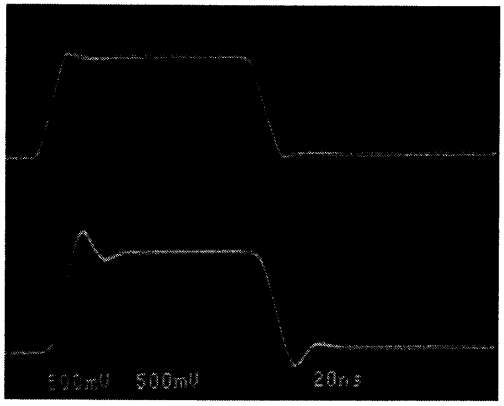
Power Supply Rejection Ratio vs Frequency



2012-2

EL2012
Closed Loop Buffer

Small Signal Response



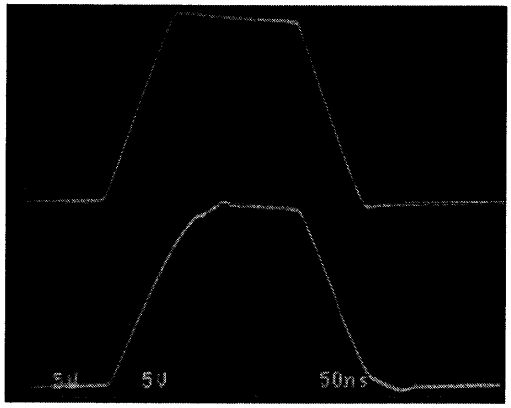
V_{IN} = ±500 mV

← 0V INPUT

← 0V OUTPUT
R_L = 50Ω
C_L = 50 pF

2012-3

Large Signal Response



V_{IN} = ±10V

← 0V INPUT

← 0V OUTPUT
R_L = 50Ω
C_L = 50 pF

2012-4

Application Information

The EL2012 is a monolithic buffer built on Elantec's complementary bipolar process that produces NPN and PNP transistors with essentially identical characteristics. The EL2012 takes full advantage of the complementary process.

Power Supplies

The EL2012 may operate with single or split supplies with a total voltage difference between 10V (±5V) and 36V (±18V). It is not necessary to use equal split supplies. For example −5V and +12V would be excellent for signals between −2V and +9V.

Bypass capacitors from each supply to ground are highly recommended to reduce supply ringing and the interference it can cause. At a minmum a 5 μF tantalum capacitor in parallel with a 0.1 μF capacitor with short leads should be used for both supplies.

Input Characteristics

The input to the EL2012 looks lke a 20 MΩ resistance in parallel with about 5 pF in addition to about 0.5 μA DC bias current. The input bias current over temperature is in the same range as many FET input buffers. The input impedance is 10 or more times that of most bipolar buffers.

Application Information — Contd.

Internal clamp diodes from the input to the output are provided to protect the transistor base emitter junctions. The diodes begin to conduct at about ±2.5V input to output differential. When that happens the input resistance drops dramatically. When conducting, the diodes have a series resistance of about 150Ω. The diodes can conduct 50 mA without damage. If the device driving the EL2012 can supply more than 50 mA to ground and the EL2012 could be shorted to ground then extra series resistance should be placed in series with the EL2012's input.

Source Impedance

The EL2012 has good input to output isolation. When the buffer is not used in a feedback loop, capacitive and resistive sources present no oscillation problems. High source resistances will produce V_{OS} errors due to the input bias current and will limit the bandwidth due to the input capacitance. But since R_{IN} is > 20 MΩ source resistances up to 10 kΩ will still maintain a gain of 0.995.

Current Limit

The EL2012 has internal current limiting to protect the output transistors. This limit is above 300 mA with the output shorted to ground and 500 mA with the output shorted to ±15V. The EL2012 does survive seconds long shorts to either supply voltage as long as heat sinking is sufficient to keep the junction temperatures below 200°C.

Parallel Operation

DO NOT CONNECT EL2012'S IN PARALLEL! The EL2012's closed loop topology and finite offset voltage will cause parallel units to fight each other, each trying to force the common output to a slightly different voltage. Large quiescent supply currents will result.

Transient Performance and Settling Times

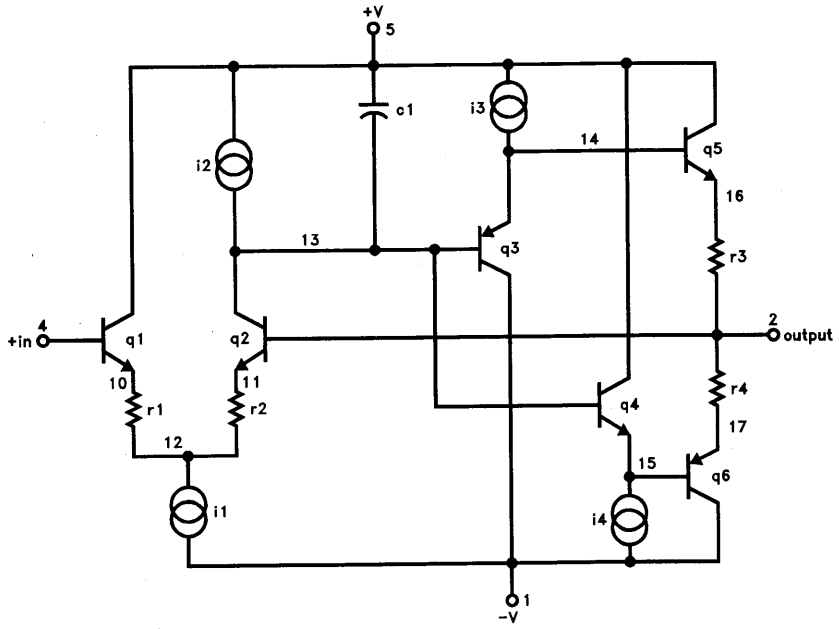
The EL2012 is considerably more complex than the simplified schematic implies. This extra internal circuitry does require certain precautions to maximize the EL2012's performance. The input signal slew rate should be limited to 400V per microsecond or less. If it is not, the output waveform will suffer unusual distortions and settling times will more than double. One simple way to deal with very fast input signals is to place a series resistor at the EL2012's input. The resistor and the input capacitance form a simple filter. With a limited slew rate input signal the typical 0.1% settling time is 75 ns for a 10V step with a 50Ω and 50 pF load and 65 ns for a 2V step with a 50Ω and 50 pF load.

EL2012
Closed Loop Buffer

EL2012 Macromodel

```
* Macromodel
* Connections:      +input
*                   |     +Vsupply
*                   |     |     -Vsupply
*                   |     |     |     output
*                   |     |     |     |
.subckt M2012       4     5     1     2
* Input Stage
q1 5 4 10 qn
q2 13 2 11 qn
r1 10 12 200
r2 11 12 200
il 12 1 2.6mA
i2 5 13 1.3mA
c1 5 13 6pF
* Output Stage
i3 5 14 3mA
i4 15 1 3mA
q3 1 13 14 qp
q4 5 13 15 qn
q5 5 14 16 qn
q6 1 15 17 qp
r3 16 2 0.1
r4 2 17 0.1
* Power Supply Current
ips 5 1 5mA
* Models
.model qn npn(is=800e-18 bf=500 tf = 0.2nS ptf=45 rb=250)
.model qp npn(is=800e-18 bf=500 tf = 0.2nS ptf=45 rb=250)
.ends
```

EL2012 Macromodel — Contd.



2012-6