EL2018/EL2018C

Fast, High Voltage Comparator with Transparent Latch

Features

- Fast response time—20 ns
- Wide input differential voltage range—24V to ±15V supplies
- Precision input stage—V_{OS} = 1 mV
- Low input bias current—I_B = 100 nA
- Low input offset current—I_{OS} = 30 nA
- ±4.5V to ±18V supplies
- 3-State TTL and CMOS compatible output
- No supply current glitch during switching
- High voltage gain—40 V/mV
- 50% power reduction in shutdown mode
- Input and latch remain active in shutdown mode
- P/N compatible with industry standard comparators

Applications

- Analog to digital converters
- ATE pin receiver
- Precision crystal oscillators
- Zero crossing detector
- Window detector
- Pulse width modulation generator
- "Go/no-go" detector

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2018CH	0°C to +75°C	TO-99	MDP0004
EL2018CJ	0°C to +75°C	CerDIP	MDP0010
EL2018CN	0°C to +75°C	P-DIP	MDP0031
EL2018H	−55°C to +125°C	TO-99	MDP0004
EL2018H/883B	−55°C to +125°C	TO-99	MDP0004
EL2018J	−55°C to +125°C	CerDIP	MDP0010
EL2018J/883B	−55°C to +125°C	CerDIP	MDP0010

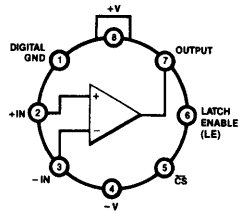
General Description

The EL2018 represents a quantum leap forward in comparator speed, accuracy and functionality. Manufactured with Elantec's proprietary Complementary Bipolar process, this device uses fast PNP and NPN transistors in the signal path. A unique circuit design gives the inputs the ability to handle large common mode and differential mode signals, yet retain high speed and excellent accuracy. Careful design of the front end insures the part maintains speed and accuracy when operating with a mix of small and large signals. The three-state output stage is designed to be TTL compatible for any power supply combination, yet it draws a constant current and does not generate glitches. When the output is disabled, the supply current consumption drops by 50%, but the input stage and latch remain active.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, see: *Elantec's Military Processing-Monolithic Products.*

Connection Diagrams

TO-99 Metal Can



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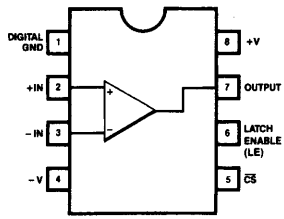
8-Pin CerDIP
8-Pin Plastic DIP



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Top View

EL2018/EL2018C

Fast, High Voltage Comparator with Transparent Latch

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V	I_O	Continuous Output Current	25 mA
V_{IN}	Input Voltage	$+V_S$ to $-V_S$	T_A	Operating Temperature Range	
ΔV_{IN}	Differential Input Voltage	Limited only by Power Supplies		EL2018	−55°C to +125°C
				EL2018C	0°C to +75°C
I_{IN}	Input Current (Pins 1, 2 or 3)	±10 mA	T_J	Operating Junction Temperature	
I_{INS}	Input Current (Pins 5 or 6)	±5 mA		Ceramic DIP Package,	
P_D	Maximum Power Dissipation			Metal Can Package	175°C
	(Note 4—See Curves)			Plastic DIP Package	150°C
	CerDIP	1.5W	T_{ST}	Storage Temperature	−65°C to +150°C
	Metal Can	1.0W		Lead Temperature	
	Plastic DIP	1.25W		(Soldering, 10 seconds)	300°C
I_{OP}	Peak Output Current	50 mA			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level		Units
						EL2018	EL2018C	
V_{OS}	Input Offset Voltage (Note 1) V_{CM} = 0V, V_O = 1.4V	25°C		1.0	3	I	I	mV
		T_{MIN}, T_{MAX}			5	I	III	mV
I_B	Input Bias Current V_{CM} = 0V, Pin 2 or 3	25°C		100	300	I	I	nA
		T_{MIN}, T_{MAX}			500	I	III	nA
I_{OS}	Input Offset Current V_{CM} = 0V	25°C		30	150	I	I	nA
		T_{MIN}, T_{MAX}			250	I	III	nA
CMRR	Common Mode Rejection Ratio (Note 2)	25°C	85	105		I	I	dB
		T_{MIN}, T_{MAX}	80			I	III	dB
PSRR	Power Supply Rejection Ratio (Note 3)	25°C	85	100		I	I	dB
		T_{MIN}, T_{MAX}	77			I	III	dB
V_{CM}	Common Mode Input Range	25°C	±12	±13		I	I	V
		T_{MIN}, T_{MAX}	±12			I	III	V
A_V	Voltage Gain V_{OUT} = 0.8V to 2.0V	25°C	15	40		I	I	V/mV
		T_{MIN}, T_{MAX}	10			I	III	V/mV
V_{OL}	Output Voltage Logic Low I_{OL} = 0 mA to 8 mA	25°C	−0.05	0.15	0.4	I	I	V
		T_{MIN}, T_{MAX}	−0.1		0.4	I	III	V

DC Electrical Characteristics V_S = ±15V unless otherwise specified — Contd.

Parameter	Description	Temp	Min	Typ	Max	Test Level		Units
						EL2018	EL2018C	
V_{oh}	Output Voltage Logic High V_S = ±15V	25°C	3.5	4.0	4.65	I	I	V
	V_S = ±15V	T_{MIN}, T_{MAX}	3.5		4.65	I	III	V
	V_S = ±5V	25°C	2.4			I	I	V
	V_S = ±5V	T_{MIN}	2.4			I	III	V
	V_S = ±5V	T_{MAX}	2.4			I	III	V
V_{odis1}	V_{OUT} Range, Disabled, I_{OL} = −1 mA V_S = ±15V	25°C	4.65			I	I	V
	V_S = ±15V	T_{MIN}, T_{MAX}	4.65			I	II	V
	V_S = ±5V	25°C		3.5		V	V	V
V_{odis2}	V_{OUT} Range, Disabled, I_{OL} = 1 mA V_S = ±5V to ±15V	ALL	−0.3	−1		I	II	V
V_{inh}	LE or $\overline{CS}$ Inputs Logic High Input Voltage	25°C	2.0			I	I	V
		T_{MIN}, T_{MAX}	2.2			I	III	V
V_{inl}	LE or $\overline{CS}$ Inputs Logic Low Input Voltage	25°C			0.8	I	I	V
		T_{MIN}, T_{MAX}			0.8	I	III	V
I_{in}	LE or $\overline{CS}$ Inputs Logic Input Current V_{IN} = 0V to 5V	25°C			±200	I	I	µA
		T_{MIN}, T_{MAX}			±300	I	III	µA
I_{s+en}	Positive Supply Current Enabled	25°C		8.4	10	I	I	mA
		T_{MIN}, T_{MAX}			11	I	III	mA
I_{s+dis}	Positive Supply Current Disabled	25°C		4.7	6	I	I	mA
		T_{MIN}, T_{MAX}			7	I	III	mA
I_{s-en}	Negative Supply Current Enabled	25°C		13.0	17	I	I	mA
		T_{MIN}, T_{MAX}			18	I	III	mA
I_{s-dis}	Negative Supply Current Disabled	25°C		5.0	6.5	I	I	mA
		T_{MIN}, T_{MAX}			6.5	I	III	mA

EL2018/EL2018C

Fast, High Voltage Comparator with Transparent Latch

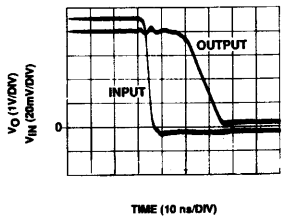
AC Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$

Parameter	Description	Min	Typ	Max	Test Level		Units
					EL2018	EL2018C	
T_{pd}	Propagation Delay, 5 mV Overdrive		20	40	I	III	ns
T_s	Setup Time		6	12	I	III	ns
T_h	Hold Time		−2	0	I	III	ns
T_{un}	Unlatch Time		23	40	I	III	ns
T_{mpw}	Minimum Clock Pulse Width		12		V	V	ns
T_{en}	Output 3-State Enable Delay		40	70	I	III	ns
T_{dis}	Output 3-State Disable Delay		150	300	I	III	ns

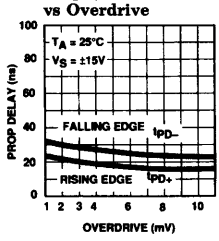
Note 1: $V_{OUT} = 1.4V$.
Note 2: $V_{CM} = 12V$ to $-12V$.
Note 3: $V_S = \pm 5V$ to $\pm 15V$.
Note 4: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the Typical Performance curves for more details.

Typical AC Performance Curves

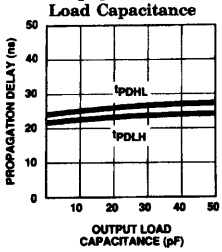
Propagation Delay (−)
5 mV Overdrive



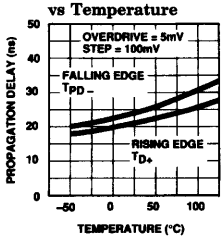
Propagation Delay
vs Overdrive



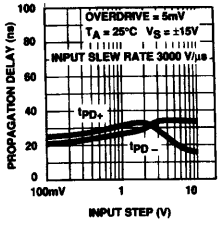
Propagation Delay vs
Load Capacitance



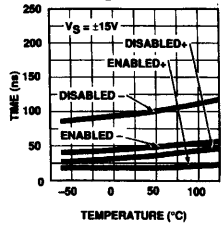
Propagation Delay
vs Temperature



Propagation Delay
vs Input Step



Enabled/Disabled Time
vs Temperature



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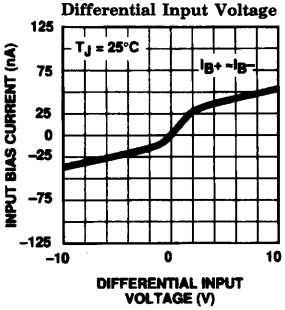
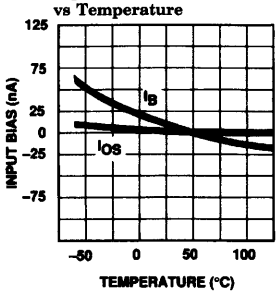
Typical AC Performance Curves — Contd.

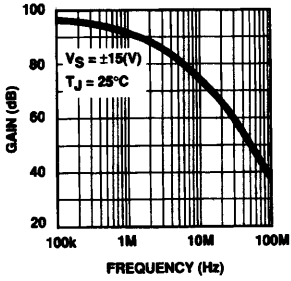
Input Bias Current vs Differential Input Voltage



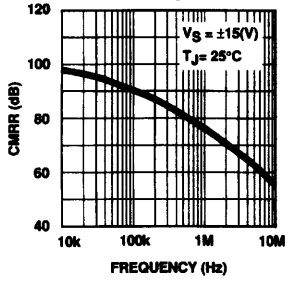
Input Bias Current vs Temperature



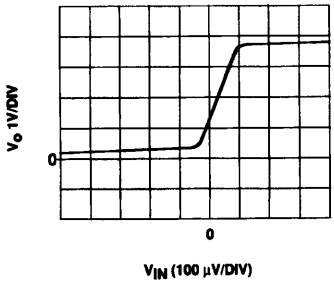
Open-Loop Gain vs Frequency



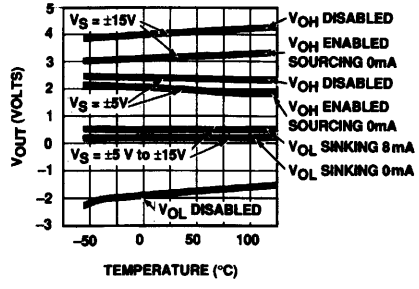
CMRR vs Frequency



V_O/V_I Transfer Characteristic



V_{OUT} vs Temperature



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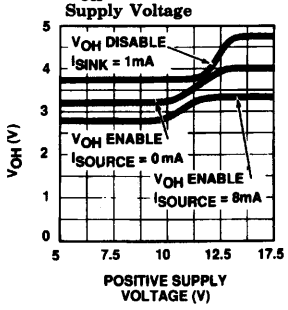
EL2018/EL2018C

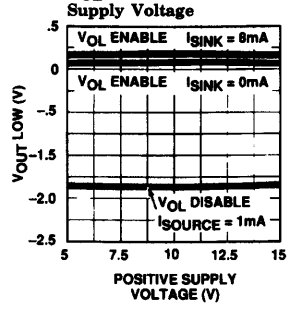
Fast, High Voltage Comparator with Transparent Latch

Typical Performance Curves — Contd.

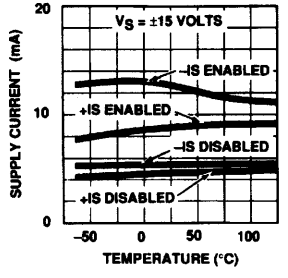
V_{OH} vs Positive Supply Voltage



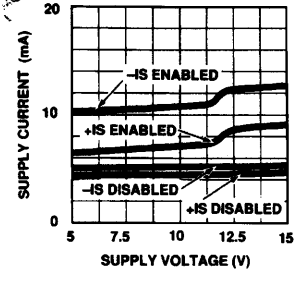
V_{OL} vs Positive Supply Voltage



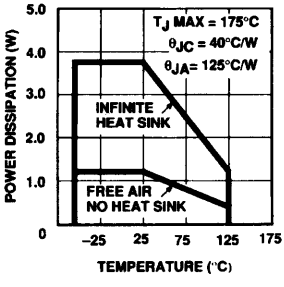
Supply Current vs Temperature



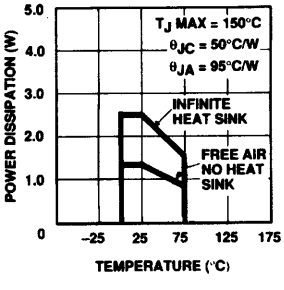
Supply Current vs Supply Voltage



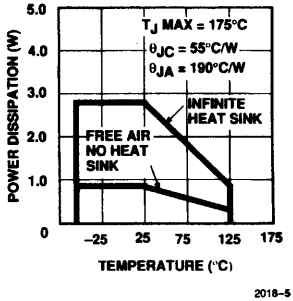
8-Lead CerDIP Maximum Power Dissipation vs Ambient Temperature



8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



8-Lead TO-99 Metal Can Maximum Power Dissipation vs Ambient Temperature



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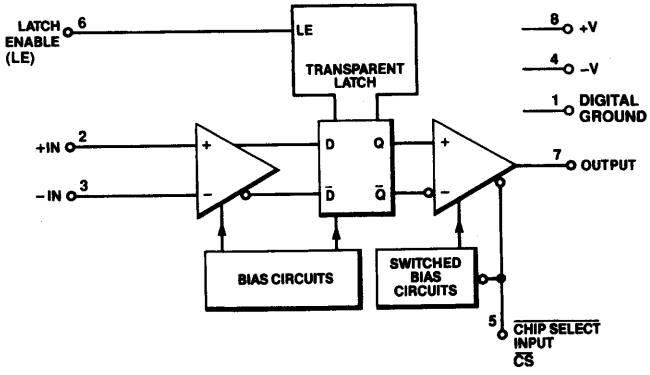
Block Diagram



Function Table

Inputs (time n−1)				Internal Q	Notes	Output
+IN	−IN	$\overline{CS}$	LE			
+	−	L	L	H	Normal Comparator Operation	H
−	+	L	L	L		L
+	−	H	L	H	Internal Normal Comparator Operation	High Z
−	+	H	L	L	Output Power Down Mode	High Z
X	X	L	H	Qn−1	Data Retained in Latch	Qn−1
X	X	H	H	Qn−1	Data Retained in Latch Power Down Mode	High Z

Application Hints

Device Overview

The EL2018 is the first comparator of its kind. It is capable of 24V differential signals, yet has excellent accuracy, linearity and voltage gain. It even has a 3-state output feature that reduces the power supply currents 50% when the output is disabled, yet the input stage and latch remain active. This extremely fast and accurate device is built with the proprietary Elantec Complementary Bipolar Dielectric Isolation Process, which is immune to power sequencing and latch up problems.

Power Supplies

The EL2018 will work with ±5V to ±18V supplies or any combination between (Example +12V and −5V). The supplies should be well bypassed with good high frequency capacitors (0.1 μF monolithic ceramic recommended) close to the power supply leads. Good ground plane construction techniques enhance stability, and the lead from pin 1 to ground should be short.

Front End

The EL2018 uses schottky diodes to make a "bullet proof" front end with very low input bias currents, even if the two inputs are tied to very large differential voltages (±24V). The transfer function of the EL2018 is linear, and the output is stable when in the linear region.

The large common mode range (±12V minimum) and differental voltage handling ability (±24V min.) of the device make it useful in ATE applications without the need for an input attenuator with its associated delay.

EL2018/EL2018C
Fast, High Voltage Comparator with Transparent Latch

Application Hints — Contd.

Recovery from Large Overdrives
Timing accuracy is excellent for all signals within the common mode range of the device (±12V with ±15V supply). When the common mode range is exceeded the input stage will saturate, input bias currents increase and it may take as much as 200 ns for the device to recover to normal operation after the inputs are returned to the common mode range. If signals greater than the common mode range of the device are anticipated, the inputs should be diode clamped to remain within the common mode range of the device.

Input Slew Rate
All comparators have input slew rate limitations. The EL2018 operates normally with any input slew rate up to 300 V/μs. Input signal slew rates over 300 V/μs induce offset voltages of 5 mV to 20 mV. This induced offset voltage settles out in about 20 ns, 20 times faster than previous high voltage comparators.

Latch
The EL2018 contains a "transparent" latch. A "transparent" latch acts as an amplifier when the LE input is low and it "latches" and holds the value it had just before the LE transition from low to high.

It is possible to make an oscillation resistant design by putting a short duration "0" on the LE input whenever you wish to make a comparison. This gates the comparator on only for a brief instant, long enough to compare, but not long enough to oscillate. The minimum duration of this pulse is specified by the minimum clock width parameter in the AC electrical tables.

The $\overline{CS}$ input may be left floating and still produce a guaranteed logic "0" input (active). Floating the LE input will normally produce a logic "0" input also, but operation is not guaranteed.

Proper RF technique suggests that these inputs be grounded or pulled to ground if they are not used.

Output Stage
The output stage of the EL2018 is a pair of complementary emitter followers operating as a linear amplifier. This makes the output stage of the EL2018 glitch free, and improves accuracy and stability when operating with small signals.

3-State Output, Power Saving Feature
The EL2018 has an output stage which can be put into a high impedance "3-state" mode. When it is in this mode, the input stage and latch remain active, yet the device dissipates only 50% of the power used when the output is active. This has advantages in a large ATE system where there may be 1000 comparators, but only 10% are in use at any one time.

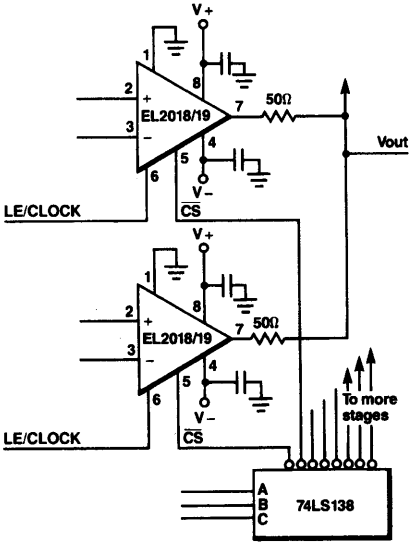
Due to the power saving feature and linear output stage, the EL2018 does not have a standard TTL 3-state output stage. As such one must be careful when using the 3-state feature with devices other than other EL2018's or EL2019's. When operating from ±15V supplies the 3-state feature is compatible with all TTL families, however CMOS families may conflict on high outputs. Since the output stage of the EL2018 turns on faster than it turns off, a 50Ω to 100Ω resistor in series with the output will limit fault currents between devices with minimum impact on logic drive capability.

System Design Considerations
The most common problem users have with high speed comparators is oscillations due to output to input feedback. This can be avoided by using a ground plane, proper supply bypassing, and routing the inputs and outputs away from each other. Since the EL2018 has a gain bandwidth product of about 40 GHz, layout and bypassing are important to a successful system design. A unique alternative to the EL2018 is the EL2019, with its edge triggered master/slave flip flop.

Device Functions
The various operating states of the EL2018 are described in the function table on page 7.

Typical Applications

Using the Power Down/ 3-State Feature



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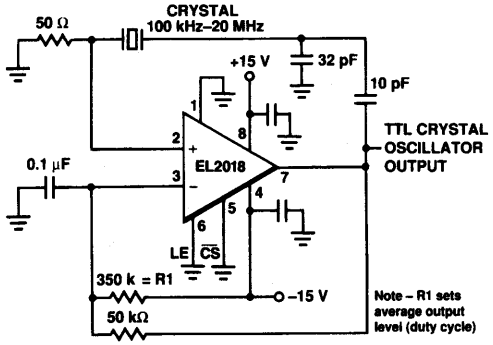
Series Resonant Crystal Oscillator



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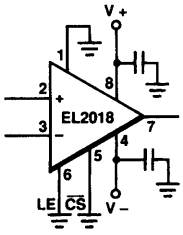
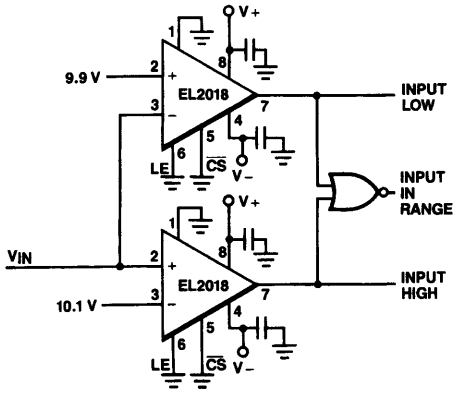
Using the EL2018 in the Transparent Mode (Latch Not Used)



2018-9

A Wide Input Range Window Comparator

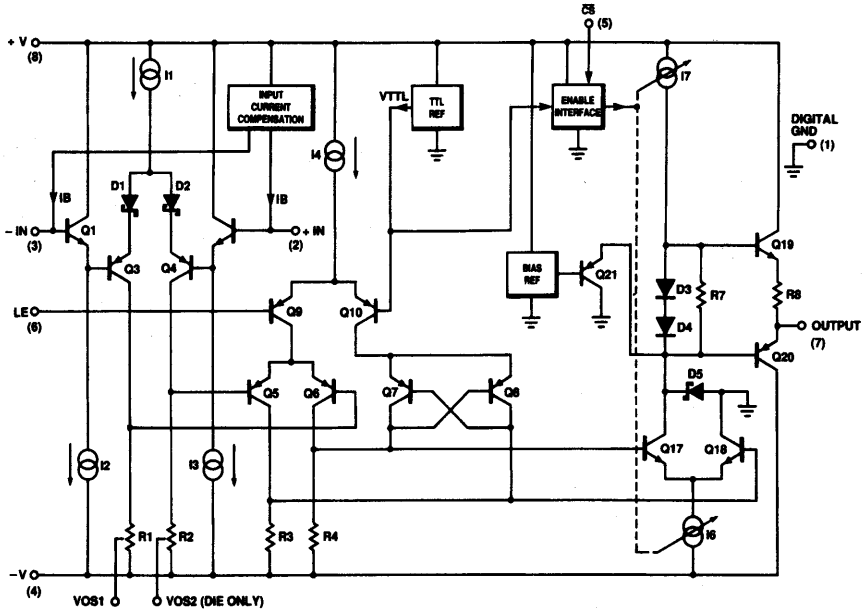


2018-10

V_{IN} Range +12V to −12V
with V_S = ±15V

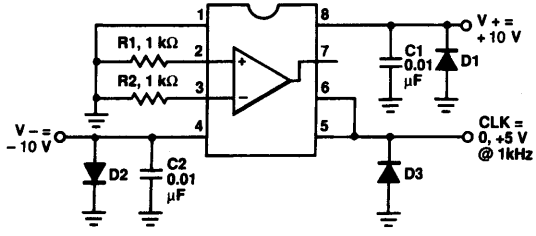
EL2018/EL2018C
Fast, High Voltage Comparator with Transparent Latch

Equivalent Schematic



2018-11

Burn-In Circuit



2018-12

Pin numbers are for DIP packages.
All packages use the same schematic.

Clip!

EL2018D Die

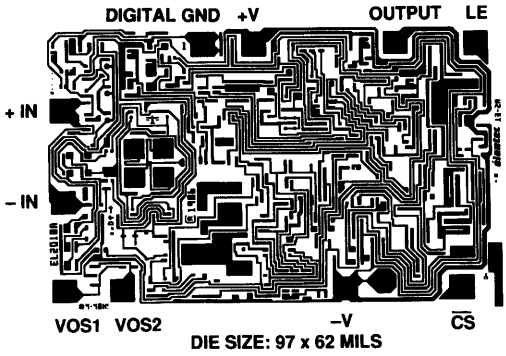
Fast, High Voltage Comparator with Transparent Latch

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V
V_{IN}	Input Voltage	$+V_S$ to $-V_S$
ΔV_{IN}	Differential Input Voltage	Limited Only by Power Supplies
I_{IN}	Input Current	±10 mA
I_{INS}	Input Current	±5 mA
T_J	Maximum Junction Temperature	175°C

Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.



DC Electrical Characteristics V_S = ±15V, T_A = 25°C

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage (Note 1) V_{CM} = 0V, V_{OS} = 1.4V		1	3	I	mV
I_B	Input Bias Current V_{CM} = 0V, pin 2 or 3		100	300	I	nA
I_{OS}	Input Offset Current V_{CM} = 0V		30	150	I	nA
CMRR	Common Mode Rejection Ratio (Note 2)	85	105		I	dB
PSRR	Power Supply Rejection Ratio (Note 3)	85	100		I	dB
V_{CM}	Common Mode Input Range	±12	±13		I	V
A_V	Voltage Gain V_{OUT} = 0.8V to 2.0V	15	40		I	V/mV
V_{OL}	Output Voltage Logic Low I_{OL} = 0 mA to 8 mA	−0.05	0.15	0.4	I	V
V_{OH}	Output Voltage Logic High V_S = ±15V	3.5	4	4.5	I	V
	V_S = ±5V	2.7	3	3.3	I	V

EL2019/EL2019C

Fast, High Voltage Comparator with Master Slave Flip-Flop

Features

- Comparator cannot oscillate
- Fast response—5 ns data to clock setup, 20 ns clock to output
- Wide input differential voltage range—24V on ±15V supplies
- Wide input common mode voltage range—±12V
- Precision input stage—V_{OS} = 1.5 mV
- Low input bias current—100 nA
- Low input offset current—30 nA
- ±4.5V to ±18V supplies
- 3 State TTL compatible output
- No supply current glitch during switching
- 103 dB voltage gain (Low input uncertainty ≈ 30 μV)
- 50% power reduction in shutdown mode
- Input and flip-flop remain active in shutdown mode

Applications

- Analog to digital converters
- ATE pin receiver
- Zero crossing detector
- Window detector
- "Go/no-go" detector

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2019CH	0°C to +75°C	TO-99	MDP0004
EL2019CJ	0°C to +75°C	CerDIP	MDP0010
EL2019CN	0°C to +75°C	P-DIP	MDP0006
EL2019H	−55°C to +125°C	TO-99	MDP0004
EL2019H/883B	−55°C to +125°C	TO-99	MDP0004
EL2019J	−55°C to +125°C	CerDIP	MDP0010
EL2019J/883B	−55°C to +125°C	CerDIP	MDP0010

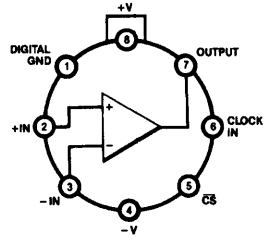
General Description

The EL2019 offers a new feature previously unavailable in a comparator before—a master/slave edge triggered flip-flop. The comparator output will only change output state after a positive going clock edge is applied. Thus the output can't feed back to the input and cause oscillation. Manufactured with Elantec's proprietary Complementary Bipolar process, this device uses fast PNP and NPN transistors in the signal path. A unique circuit design gives the inputs the ability to handle large common mode and differential mode signals, yet retain high speed and excellent accuracy. Careful design of the front end insures speed and accuracy when operating with a mix of small and large signals. The three-state output stage is designed to be TTL compatible for any power supply combination, yet it draws a constant current and does not generate current glitches. When the output is disabled, the supply current consumption drops by 50%, but the input stage and master slave flip-flop remain active.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's military processing, see *Elantec's Military Processing-Monolithic Products.*

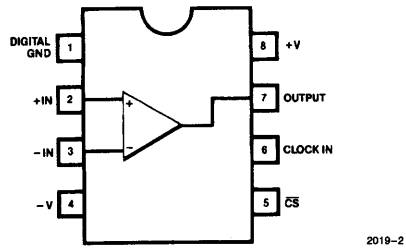
Connection Diagrams

TO-99 Metal Can



2019-1

8-Pin CerDIP
8-Pin Plastic DIP



2019-2

Top View

EL2019/EL2019C

Fast, High Voltage Comparator with Master Slave Flip-Flop

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V	I_O	Continuous Output Current	25 mA
V_{IN}	Input Voltage	$+V_S$ to $-V_S$	T_A	Operating Temperature Range	
ΔV_{IN}	Differential Input Voltage	Limited only by Power Supplies		EL2019	−55°C to +125°C
				EL2019C	0°C to +75°C
I_{IN}	Input Current (Pins 1, 2 or 3)	±10 mA	T_J	Operating Junction Temperature	
I_{INS}	Input Current (Pins 5 or 6)	±5 mA		Ceramic DIP Package,	
P_D	Maximum Power Dissipation (Note 3 - See Curves)			Metal Can Package	175°C
	CerDIP	1.5W		Plastic DIP Package	150°C
	Metal Can	1.0W	T_{ST}	Storage Temperature	−65°C to +150°C
	Plastic DIP	1.25W		Lead Temperature	
I_{OP}	Peak Output Current	50 mA		(Soldering, 5 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, unless otherwise specified

Parameter	Description	Temp	Limits			Test Level		Units
			Min	Typ	Max	EL2019	EL2019C	
V_{OS}	Input Offset Voltage V_{CM} = 0V, V_O Transition Point	25°C		1.5	5	I	I	mV
		T_{MIN}, T_{MAX}			7	I	III	mV
I_B	Input Bias Current V_{CM} = 0V, Pin 2 or 3	25°C		±100	±300	I	I	nA
		T_{MIN}, T_{MAX}			±500	I	III	nA
I_{OS}	Input Offset Current V_{CM} = 0V	25°C		30	150	I	I	nA
		T_{MIN}, T_{MAX}			250	I	III	nA
CMRR	Common Mode Rejection Ratio (Note 1)	25°C	75	90		I	I	dB
PSRR	Power Supply Rejection Ratio (Note 2)	25°C	75	95		I	I	dB
V_{CM}	Common Mode Input Range	25°C	±12	±13		I	I	V
		T_{MIN}, T_{MAX}	±12			I	III	V
V_{uncer}	Input Uncertainty Range			30		V	V	μV/RMS
V_{OL}	Output Voltage Logic Low I_{OL} = 8 mA and I_{OL} = 0 mA)	25°C	−0.05	0.15	0.4	I	I	V
		T_{MIN}, T_{MAX}	−0.1		0.4	I	III	V
V_{OH}	Output Voltage Logic High							
	V_S = ±15V	25°C	3.5	4.0	4.65	I	I	V
	V_S = ±15V	T_{MIN}, T_{MAX}	3.5		4.65	I	III	V
	V_S = ±5V	25°C	2.4			I	I	V
	V_S = ±5V	T_{MIN}	2.4			I	III	V
	V_S = ±5V	T_{MAX}	2.4			I	III	V

DC Electrical Characteristics $V_S = \pm 15V$, unless otherwise specified — Contd.

Parameter	Description	Temp	Limits			Test Level		Units
			Min	Typ	Max	EL2019	EL2019C	
V_{ODIS1}	V_{OUT} Range, Disabled, $I_{OL} = -1$ mA							
	$V_S = \pm 15V$	25°C	4.65			I	I	V
	$V_S = \pm 15V$	T_{MIN}, T_{MAX}	4.65			I	III	V
	$V_S = \pm 5V$	25°C		3.65		V	V	V
V_{ODIS2}	V_{OUT} Range, Disabled, $I_{OL} = +1$ mA $V_S = \pm 5V$ to $+15V$	All	-0.3	-1		I	II	V
V_{INH}	Clock or $\overline{CS}$ Inputs	25°C	2			I	I	V
	Logic High Input Voltage	T_{MIN}, T_{MAX}	2			I	III	V
I_{IN}	Clock or $\overline{CS}$ Inputs Logic Input Current $V_{IN} = 0V$ and $V_{IN} = 5V$	25°C			± 200	I	I	µA
		T_{MIN}, T_{MAX}			± 300	I	III	µA
V_{INL}	Clock or $\overline{CS}$ Inputs Logic Low Input Voltage	25°C			0.8	I	I	V
		T_{MIN}, T_{MAX}			0.8	I	III	V
I_{S+EN}	Positive Supply Current Enabled	25°C		8.8	11	I	I	mA
		T_{MIN}, T_{MAX}			12	I	II	mA
I_{S+DIS}	Positive Supply Current Disabled	25°C		4.9	6	I	I	mA
		T_{MIN}, T_{MAX}			7	I	II	mA
I_{S-EN}	Negative Supply Current Enabled	25°C		14.5	17	I	I	mA
		T_{MIN}, T_{MAX}			18	I	II	mA
I_{S-DIS}	Negative Supply Current Disabled	25°C		6.4	8.0	I	I	mA
		T_{MIN}, T_{MAX}			8.0	I	II	mA

AC Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$

Parameter	Description	Limits			Test Level		Units
		Min	Typ	Max	EL2019	EL2019C	
T_S	Setup Time 5 mV Overdrive		12	20	I	II	ns
T_H	Hold Time		-3	0	I	II	ns
T_{OPOUT}	Clock to Output Delay		20	25	I	II	ns
T_{OPMIN}	Minimum Clock Width		7		V	V	ns
T_{EN}	Output 3-State Enable Delay		40	70	I	II	ns
T_{DIS}	Output 3-State Disable Delay		150	300	I	II	ns

Note 1: $V_{CM} = +12V$ to $-12V$.

Note 2: $V_S = \pm 5V$ to $\pm 15V$.

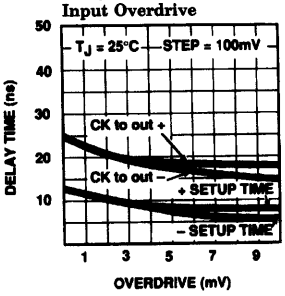
Note 3: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the Typical Performance curves for more details.

EL2019/EL2019C

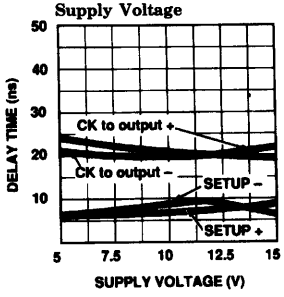
Fast, High Voltage Comparator with Master Slave Flip-Flop

Typical AC Performance Curves

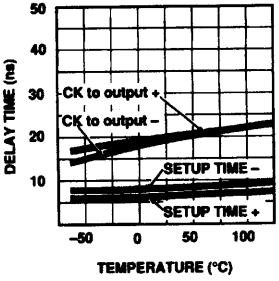
Delay Time vs Input Overdrive



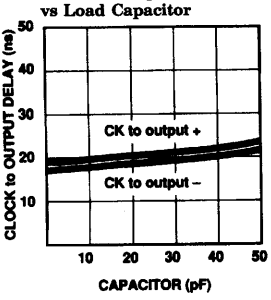
Delay Time vs Supply Voltage



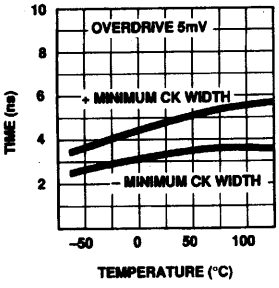
Delay Time vs Temperature



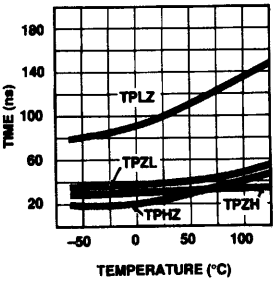
Clock to Output Delay vs Load Capacitor



Minimum Clock Width vs Temperature



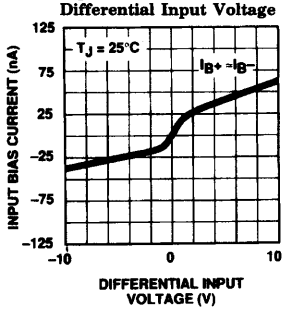
Enabled/Disabled Times vs Temperature



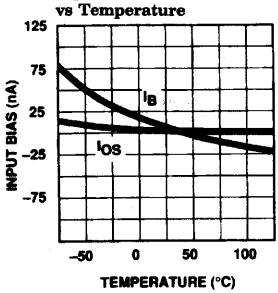
2019-3

Typical AC Performance Curves — Contd.

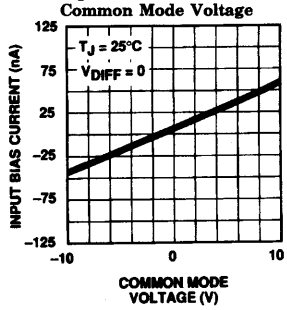
Input Bias Current vs Differential Input Voltage



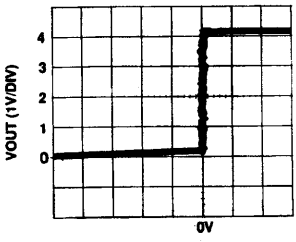
Input Bias Current vs Temperature



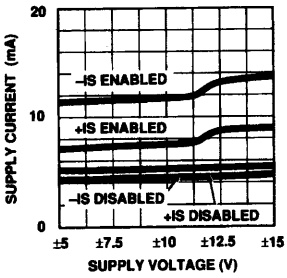
Input Bias Current vs Common Mode Voltage



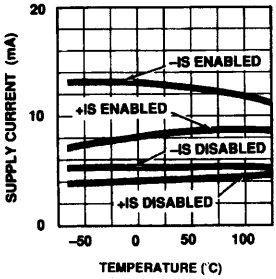
V_O/V_I Transfer Characteristics



Supply Current vs Supply Voltage



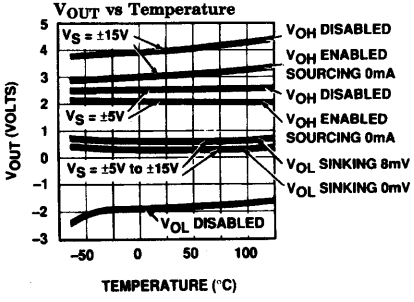
Supply Current vs Temperature



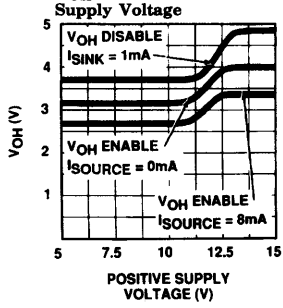
2019-4

Typical AC Performance Curves — Contd.

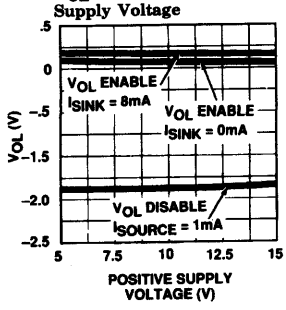
V_{OUT} vs Temperature



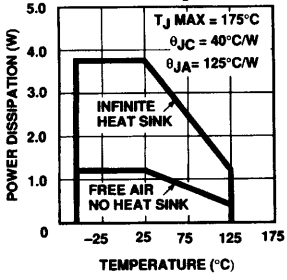
V_{OH} vs Positive Supply Voltage



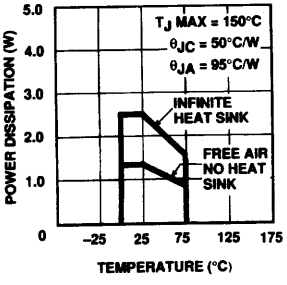
V_{OL} vs Positive Supply Voltage



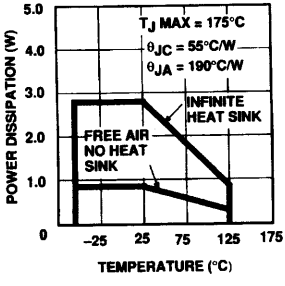
8-Lead CerDIP Maximum Power Dissipation vs Ambient Temperature



8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



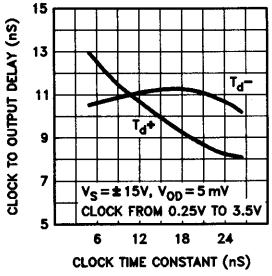
8-Lead TO-99 Metal Can Maximum Power Dissipation vs Ambient Temperature



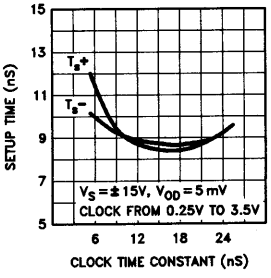
2019-5

Typical AC Performance Curves — Contd.

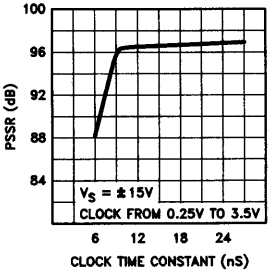
Clock to Output Delay vs Clock Time Constant



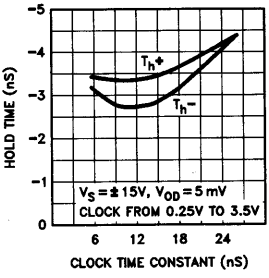
Set-up Time vs Clock Time Constant



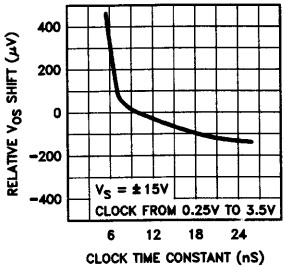
PSRR vs Clock Time Constant



Hold Time vs Clock Time Constant



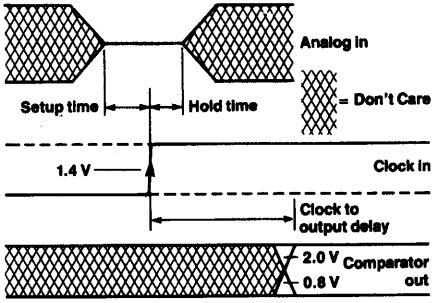
Relative V_{OS} Shift vs Clock Time Constant



2019-6

EL2019/EL2019C
Fast, High Voltage Comparator with Master Slave Flip-Flop

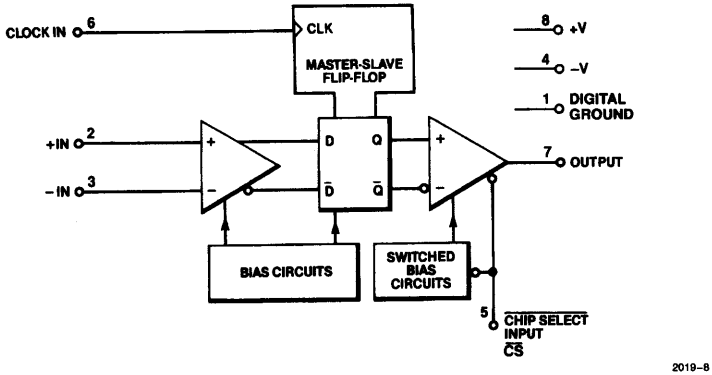
Timing Diagram



2019-7

Note: Since the hold time is negative the input is a don't care at the clock time. This ensures that clock noise will not affect the measurement.

Block Diagram



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Function Table

Inputs (Time n−1)				Internal Q (Time n)	Notes	Output (Time n)
+IN	−IN	$\overline{CS}$	CLK			
+	−	L	↓	H	Normal Comparator Operation	H
−	+	L	↓	L	With "D" Flip-Flop	L
+	−	H	↓	H	Normal Comparator Operation	High Z
−	+	H	↓	L	With "D" Flip-Flop; Power Down Mode	High Z
X	X	L	H	Qn−1	Data Retained in Flip-Flop	Qn−1
X	X	L	L	Qn−1	Data Retained in Flip-Flop	Qn−1
X	X	L	↓	Qn−1	Data Retained in Flip-Flop	Qn−1
X	X	H	H	Qn−1	Data Retained in Flip-Flop, Output Power Down Mode	High Z
X	X	H	L	Qn−1	Data Retained in Flip-Flop, Output Power Down Mode	High Z
X	X	H	↓	Qn−1	Data Retained in Flip-Flop, Output Power Down Mode	High Z

Application Hints

Device Overview

The EL2019 is the first comparator of its kind. It is capable of 24V differential signals, yet has excellent accuracy, linearity and voltage gain. The EL2019 has an internal master/slave flip-flop between the input and output. It even has a 3-state output feature that reduces the power supply currents 50% when the output is disabled, yet the input stage and latch remain active. This extremely fast and accurate device is built with the proprietary Elantec Complementary Bipolar Process, which is immune to power sequencing and latch up problems.

Power Supplies

The EL2019 will work with ±5V to ±18V supplies or any combination between (Example +12V and −5V). The supplies should be well bypassed with good high frequency capacitors (0.01 μF monolithic ceramic recommended) within ¼ inch of the power supply leads. Good ground plane construction techniques improve stability, and the lead from pin 1 to ground should be short.

Front End

The EL2019 uses schottky diodes to make a "bullet proof" front end with very low input bias currents, even if the two inputs are tied to very large differential voltages (±24V).

The large common mode range (±12V minimum) and differential voltage handling ability (±24V min.) of the device make it useful in ATE applications without the need for an input attenuator with its associated delay.

Recovery from Large Overdrives

Timing accuracy is excellent for all signals within the common mode range of the device (±12V with ±15V supply). When the common mode range is exceeded the input stage will saturate, input bias currents increase and it may take as much as 200 ns for the device to recover to normal operation after the inputs are returned to the common mode range. If signals greater than the common mode range of the device are anticipated, the inputs should be diode clamped to remain within the common mode range of the device, or the supply voltage be raised to encompass the input signal in the common mode range.

Input Slew Rate

All comparators have input slew rate limitations. The EL2019 operates normally with any input slew rate up to 300 V/μs. Input signal slew rates over 300 V/μs induce offset voltages of 5 mV to 20 mV. This induced offset voltage settles out in about 20 ns, 20 times faster than previous high voltage comparators. This shows up as an increased set-up time.

Master Slave Flip-Flop

The built-in Master/Slave Flip-Flop only allows the output to change when a positive edge is received on the clock input. This feature has some major benefits to the user. First, the device cannot oscillate due to feedback from the output to the inputs. Second, the device *must* make a decision when it receives a clock input, and the difference between deciding on a "0" or a "1" is limited only by the input circuit noise, both internal and external to the EL2019. With low impedance sources and a good layout this uncertainty can be less than 30 μV/RMS. Since a 30 μV change on the input can cause a 4V change on the output this works out to an effective gain of 103 dB, more than adequate for a 16-bit analog to digital converter.

The hold time of the EL2019 is worst case 0 ns, and typically −3 ns. This means that the analog signal is sampled typically 3 ns *before* the clock time and, worst case, concurrent with the clock.

The EL2019 is sensitive to a large clock edge rates. More than a 500 V/μs edge rate at the clock input will induce V_{OS} shifts, reduce PSRR, and cause the device to operate incorrectly at low temperatures and low supply voltages. A good method to control the clock edge rate is to place a resistor in series and a capacitor to ground in parallel with the clock input. Generally, any time constant 10 ns or greater will suffice.

Elantec tests the EL2019 with a nominal 20 ns time constant, using a series 330Ω resistor and 61 pF of capacitance to ground (including strays). All clocks are generated by Schottky TTL and have a 0.25V to 3.5V swing.

EL2019/EL2019C
Fast, High Voltage Comparator with Master Slave Flip-Flop

Application Hints — Contd.

Output Stage

The output stage of the EL2019 is a pair of complementary emitter followers operating as a linear amplifier. This makes the output stage of the EL2019 glitch free, and improves accuracy and stability when operating with small signals.

3-State Output, Power Saving Feature

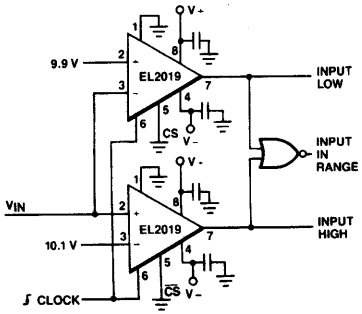
The EL2019 has an output stage which can be put into a high impedance "3-state" mode. When it is in this mode, the input stage and latch remain active, yet the device dissipates only 50% of the power used when the output is active. This has advantages in large ATE systems where there may be 1000 comparators, but only 10% are in use at any one time.

The EL2019 will work properly with the chip select input (pin 5) floating, however, good R.F. technique would be to ground this input if it is not used.

Due to the power saving feature and linear output stage, the EL2019 does not have a standard TTL 3-state output stage. As such one must be careful when using the 3-state feature with devices other than other EL2018's or EL2019's. When operating from ±15V supplies the 3-state feature is compatible with all TTL families, however CMOS families may conflict on high outputs. Since the output stage of the EL2019 turns on faster than it turns off, a 50Ω to 100Ω resistor in series with the output will limit fault currents between devices with minimum impact on logic drive capability.

Typical Applications

A Wide Input Range Window Comparator



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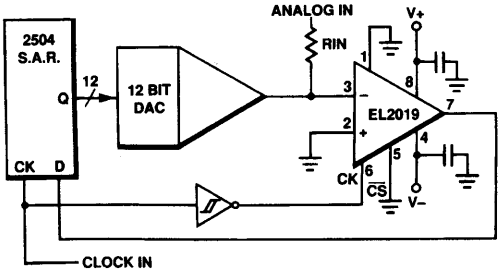
(V_{IN} Range +12V to −12V with V_S = ±15V)

The EL2019 makes an excellent comparator in most analog to digital converters, due to its high gain and fast response. Most 2504 based A to D designs can be modified to use the EL2019 simply by using an inverted clock to the EL2019 as shown below. This results in improved performance due to less jitter of the transition voltages.



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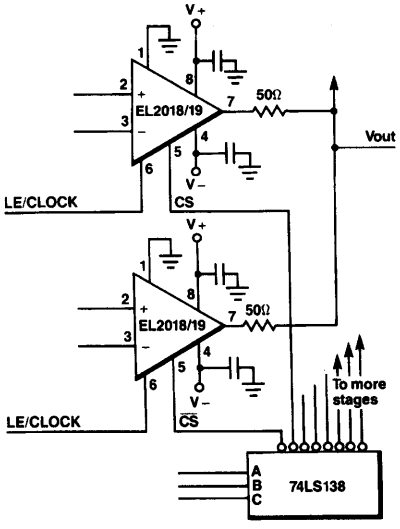
Using the Power Down/ 3-State Feature



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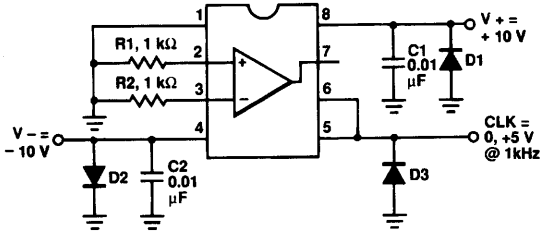
Burn-In Circuit



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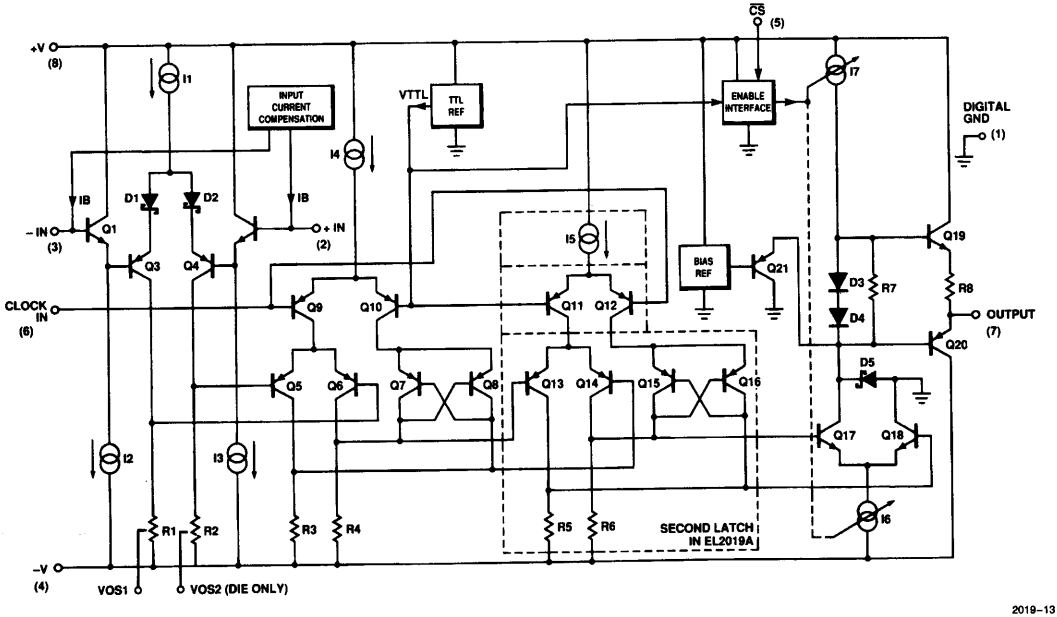
Pin numbers are for DIP packages. All packages use the same schematic.

Equivalent Schematic



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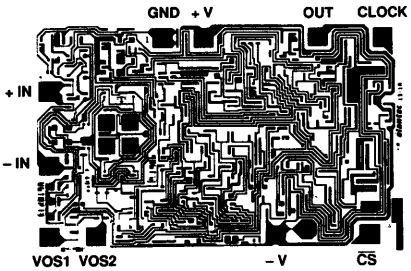
EL2019D Die

Fast, High Voltage Comparator with Master Slave Flip-Flop

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V
V_{IN}	Input Voltage	$+V_S$ to $-V_S$
ΔV_{IN}	Differential Input Voltage	Limited Only by Power Supplies
I_{IN}	Input Current	±10 mA
I_{INS}	Input Current	±5 mA
T_J	Maximum Junction Temperature	175°C



Important Note:
For AC electrical characteristics, refer to the typical electrical table and performance curves in the package data sheet. These characteristics are guaranteed but not tested in die form. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested in wafer form. See remarks under Electrical Testing in the General Die section.

DC Electrical Characteristics V_S = ±15V, T_A = 25°C, unless otherwise specified

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage (Note 1) V_{CM} = 0V, V_{OS} = 1.4V		1.5	5	I	mV
I_B	Input Bias Current V_{CM} = 0V, pin 2 or 3		100	300	I	nA
I_{OS}	Input Offset Current V_{CM} = 0V		30	150	I	nA
CMRR	Common Mode Rejection Ratio (Note 2)	75	105		I	dB
PSRR	Power Supply Rejection Ratio (Note 3)	75	100		I	dB
V_{CM}	Common Mode Input Range	±12	±13		I	V
V_{OL}	Output Voltage Logic Low I_{OL} = 0 mA to 8 mA	−0.05	0.15	0.4	I	V
V_{OH}	Output Voltage Logic High V_S = ±15V V_S = ±5V	 3.5 2.4	4	4.65	 I I	 V V