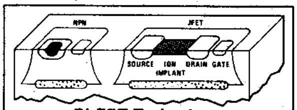
National Semiconductor

Instrumentation Amplifiers



BI-FET Technology

LF152/LF252/LF352 FET input instrumentation amplifier

general description

The LF152 series is the first monolithic JFET input instrumentation amplifier. The well-matched high voltage JFET input devices provide very high input impedance and extremely low bias currents, making the LF152 ideal in applications where high source impedances are encountered.

The LF152 very accurately amplifies a differential input signal and rejects common-mode signal and noise. It is not an op amp, but operates with an internal closed loop gain connection which allows good linearity with no external feedback. The LF152 eliminates the need for extremely precise resistor matching to obtain high common-mode rejection (CMR) and provides high input impedance as compared to the use of conventional op amps connected as a difference amplifier.

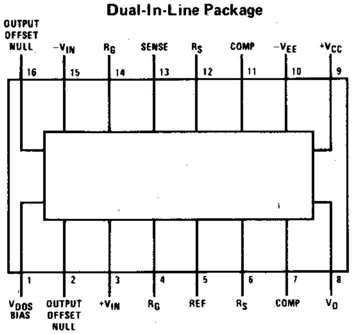
The LF152 utilizes internal differential current feedback eliminating the need for precision external feedback components. The amplifier gain can be easily adjusted from 1 to 1000 by changing the value of a single resistor. The transfer function for the LF152 is highly accurate because it has a very low initial gain error and non-linearity. The bandwidth and slew rate are externally controlled and the sense input and device output are pinned out separately for added versatility.

features

- JFET inputs
- High input impedance — $2 \times 10^{12}\Omega$
- Low bias currents — 3 pA
- Low noise currents — 0.01 pA rms
- Low gain nonlinearity — 0.02%
- High common-mode rejection ratio (G = 100) — 110 dB min
- Single resistor gain adjust
- External compensation for extended gain and frequency ranges
- Both input and output offset adjust capability to allow a change of gain without rezeroing
- Low supply current — 1 mA

connection diagram

Dual-In-Line Package



Order Number LF152D, LF252D or LF352D
See NS Package D16C

simplified schematic

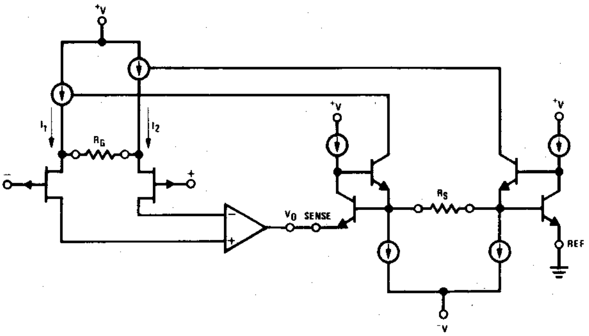


FIGURE 1

typical circuit

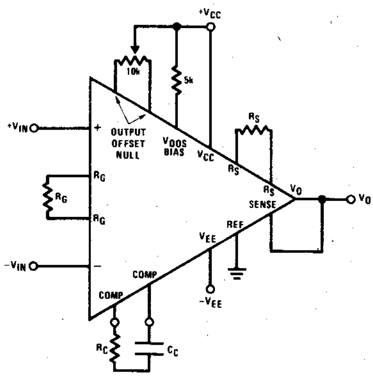


FIGURE 2

absolute maximum ratings

	LF152	LF252	LF352
Supply Voltage	±22V	±18V	±18V
Differential Input Voltage	±44V	±36V	±36V
Input Voltage Range	±22V	±18V	±18V
Output Short Circuit Duration	Continuous	Continuous	Continuous
Power Dissipation and Thermal Resistance (Note 1)			
Cavity DIP (D) P_D (25°C)	900 mW	900 mW	900 mW
θ_{jA}	100°C/W	100°C/W	100°C/W
Maximum Junction Temperature	+150°C	+110°C	+100°C
Operating Temperature Range	$-55°C \leq T_A \leq +125°C$	$-25°C \leq T_A \leq +85°C$	$0°C \leq T_A \leq +70°C$
Storage Temperature Range	$-65°C \leq T_A \leq +150°C$	$-65°C \leq T_A \leq +150°C$	$-65°C \leq T_A \leq +150°C$
Lead Temperature (Soldering, 60 seconds)	300°C	300°C	300°C

dc electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS	LF152			LF252/LF352			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
G_R	Gain Range	$R_C = 160\Omega$, $C_C = 0.002\mu F$	1		1000	1		1000	
G	Gain Equation	$G = R_S/R_G$							
G_E	Error From Gain Equation	$T_A = 25°C$, G = 1–100, R_L = 10k		0.05	0.1		0.05	0.2	%
G_{NL}	Gain Nonlinearity	$T_A = 25°C$, G = 1–100, R_L = 10k		0.02	0.05		0.02	0.1	%
$\Delta G/\Delta T$	Gain Temperature Coefficient			3			3		ppm/°C
V_O	Output Voltage Range	R_L = 2k	±9			±9			V
R_O	Output Resistance	$T_A = 25°C$, G = 1		1.2			1.5		Ω
V_{IN}	Input Voltage Range		±10	±12		±10	±12		V
I_B	Input Bias Current	$T_A = 25°C$		3	20		3	40	pA
				3	20		0.2	3	nA
I_{IO}	Input Offset Current	$T_A = 25°C$		0.5	10		0.5	20	pA
				0.3	2.0		0.05	0.6	nA
R_{IN}	Input Resistance	$T_A = 25°C$							
	Differential			2×10^{12}			2×10^{12}		Ω
	Common-Mode			2×10^{12}			2×10^{12}		Ω
C_{IN}	Input Capacitance	$T_A = 25°C$							
	Differential			2.5			2.5		pF
	Common-Mode			5.0			5.0		pF
CMRR	Common-Mode Rejection	G = 1	75	85		65	80		dB
	(RTI) (Note 4)	G = 10	95	105		85	100		dB
		G = 100	110	125		100	120		dB
		G = 1000	115	125		105	120		dB
V_{IOS}	Input Offset Voltage	$T_A = 25°C$		8	15		15	30	mV
$\Delta V_{IOS}/\Delta T$	Temperature Coefficient			10			10		μV/°C
$\Delta V_{IOS}/\Delta V_S$	Supply Sensitivity			100			200		μV/V
V_{OOS}	Output Offset Voltage	$T_A = 25°C$			200			400	mV
$\Delta V_{OOS}/\Delta T$	Temperature Coefficient			600			600		μV/°C
$\Delta V_{OOS}/\Delta V_S$	Supply Sensitivity			400			800		μV/V
I_{REF}	Reference Current			15			20		μA
R_{REF}	Reference Input Resistance			500			250		MΩ
I_S	Supply Current	$T_A = 25°C$		0.7	2.2		1.2	2.2	mA

ac electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS	LF152 MIN	LF152 TYP	LF152 MAX	LF252/LF352 MIN	LF252/LF352 TYP	LF252/LF352 MAX	UNITS
e_n	Noise Voltage (RTI) (Note 5)	$T_A = 25°C$							
		0.1 Hz – 10 Hz		1.3+670/G			1.3+670/G		μVp-p
		10 Hz – 10 kHz		8+450/G			8+450/G		μVrms
i_n	Noise Current (RTI) (Note 5)	$T_A = 25°C$, 10 Hz – 10 kHz		0.01			0.01		pArms
GBW	Small Signal Bandwidth	$T_A = 25°C$, ±3 dB							
		G = 1		140			140		kHz
		G = 10		50			50		kHz
		G = 100		30			30		kHz
		G = 1000		7			7		kHz
		$T_A = 25°C$, ±1% Flatness							
		G = 1		5			5		kHz
		G = 10		4			4		kHz
		G = 100		2			2		kHz
		G = 1000		1.5			1.5		kHz
PBW	Full-Power Bandwidth			25			25		kHz
SR	Slew Rate			1			1		V/μs
t_s	Settling Time 0.1%	$T_A = 25°C$							
		G = 1		15			15		μs
		G = 10		15			15		μs
		G = 100		40			40		μs
		G = 1000		200			200		μs

Note 1: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by $T_{j\,MAX}$, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_D = (T_{J\,MAX} - T_A)/\theta_{jA}$ or the 25°C $P_{D\,MAX}$, whichever is less.

Note 2: These specifications apply for $V_S = \pm15V$ and over the absolute maximum operating temperature range ($T_L \le T_A \le T_H$) unless otherwise noted. Parameters are specified for $R_C = 160\Omega$, $C_C = 0.002\mu F$, and a proper layout such as the PC board in *Figure 7*, which is laid out for *Figure 2 and Figure 4*.

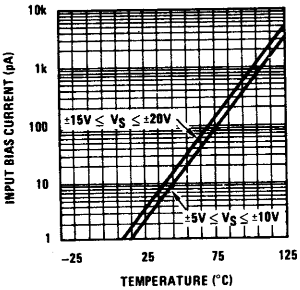
Note 3: If V_{OOS} adjust is not used, pins 1, 2 and 16 **MUST** be shorted to V_{CC}.

Note 4: Referred to input (RTI). May be referred to output by subtracting gain in dB.

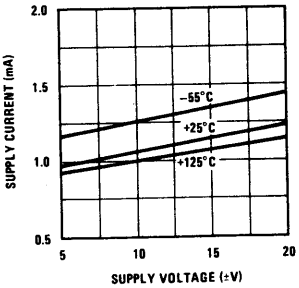
Note 5: Referred to input (RTI). May be referred to output by multiplying by gain G.

typical performance characteristics

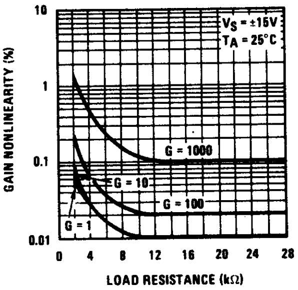
Input Bias Current



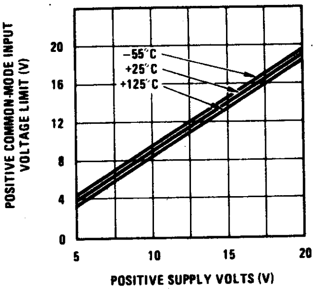
Supply Current



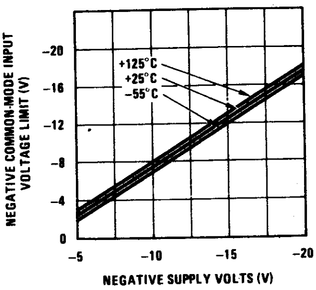
Gain Nonlinearity



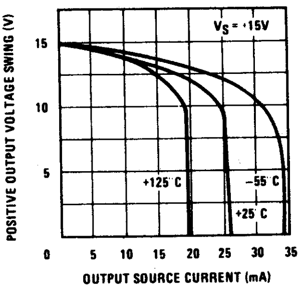
Positive Common-Mode Input Voltage Limit



Negative Common-Mode Input Voltage Limit

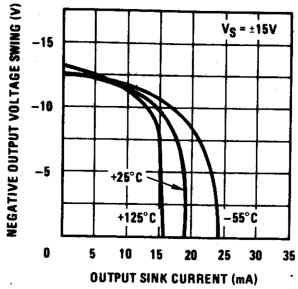


Positive Current Limit

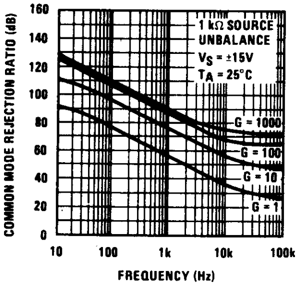


typical performance characteristics (con't)

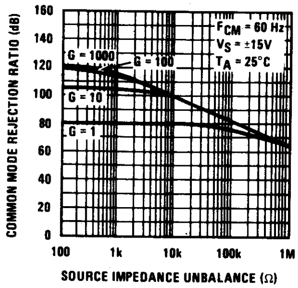
Negative Current Limit



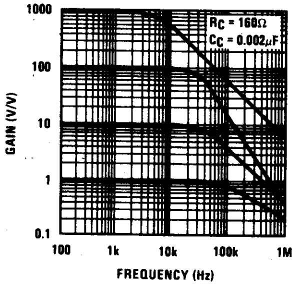
Common-Mode Rejection Ratio (RTI)



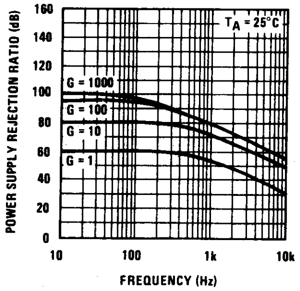
Common-Mode Rejection Ratio (RTI)



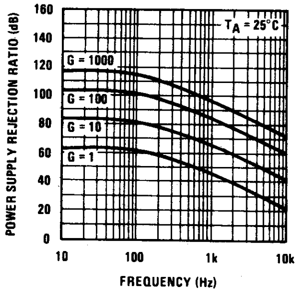
Frequency Response



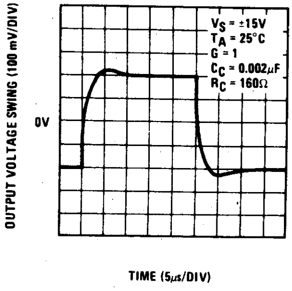
Positive Power Supply Rejection Ratio (RTI)



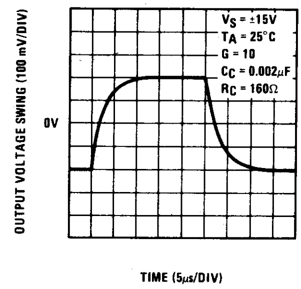
Negative Power Supply Rejection Ratio (RTI)



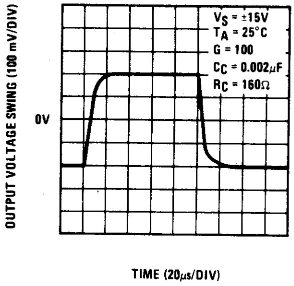
Small Signal Pulse Response (G = 1)



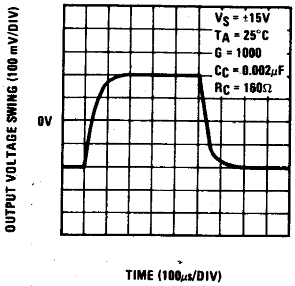
Small Signal Pulse Response (G = 10)



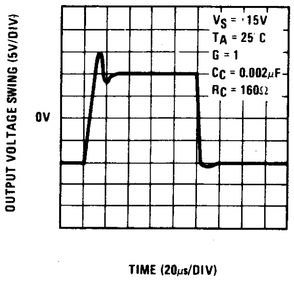
Small Signal Pulse Response (G = 100)



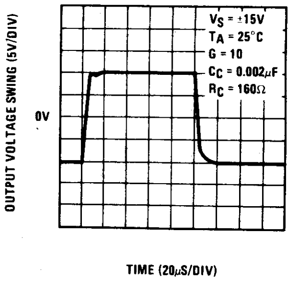
Small Signal Pulse Response (G = 1000)



Large Signal Pulse Response (G = 1)

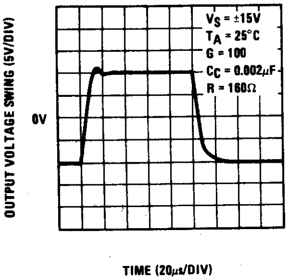


Large Signal Pulse Response (G = 10)

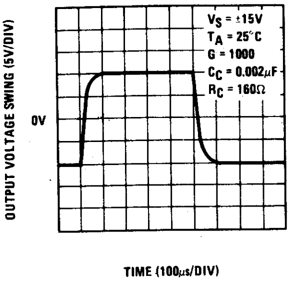


typical performance characteristics (con't)

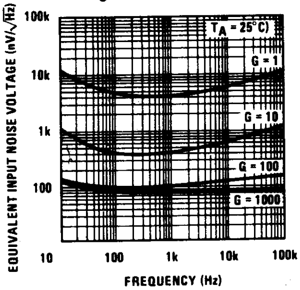
Large Signal Pulse Response (G = 100)



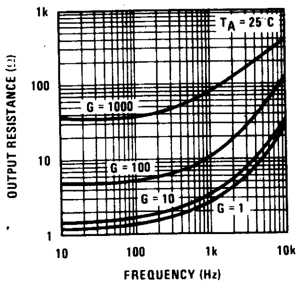
Large Signal Pulse Response (G = 1000)



Equivalent Input Noise Voltage



Output Resistance



application hints

BASIC OPERATION

The LF152 is a monolithic JFET input differential current feedback instrumentation amplifier. The BI-FET process used to fabricate the LF152 makes it possible to take advantage of JFETs throughout the design. In the simplified schematic of *Figure 1,* the differential input voltage is impressed across resistor R_G via the input JFETs, while the difference between the sense and reference voltages is impressed across the resistor R_S. The gain of the amplifier is determined by the ratio of resistor R_S to resistor R_G ($G = R_S/R_G$). (For clarity let's follow a signal through the amplifier:)

In *Figure 1,* let $R_G \doteq R_S$ = 1 MΩ, the (–) input be grounded, and the (+) input be 1V; the output should be 1V. The 1V signal applied developes 1μA through R_G from right to left and unbalances the current drive to the second stage amplifier. The additional current driven into the (+) input of the second stage amplifier causes the output to increase. As V_O increases, the sense input voltage increases and the left side of R_S also increases. When the sense input has risen 1V, 1μA will flow through R_S from left to right and, thus, subtract 1μA from I_1. An opposite action simultaneously occurs in I2 which brings the currents into the second stage and thus the system back into balance.

The LF152 series is designed to optimize key parameters in instrumentation amplifiers. The device has very high common-mode rejection, low gain non-linearity, extremely low bias currents and very high input impedance.

INPUTS

The P-channel JFET input devices of the LF152 series provide very low bias currents and very high input impedances.

The maximum differential input voltage is independent of the supply voltages, however, neither of the input voltages should be allowed to exceed the negative supply, as this will cause large currents to flow, which can result in a destroyed unit.

Exceeding the negative voltage range on either input will cause a reversal of phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative input voltage range on both inputs will force the amplifier output to a high state. Exceeding the positive input voltage range on a single input will not change the phase of the output; however, gain linearity will degrade. If both inputs exceed the positive input voltage range, the output of the amplifier will be forced to a high state.

The common-mode slew rate of the inputs should be limited to 5V/μs to insure low input bias currents.

application hints (con't)

USING THE SENSE, REFERENCE, AND OUTPUT PINS

The sense input and the output of the device are pinned out separately to allow increased flexibility in system designs (see applications). The reference input allows biasing of the output voltage, from +10V to −10V. The ac input resistance of both the sense and reference inputs is unusually high because their input currents are forced to be constant with voltage (typically 20μA).

The maximum linear output swing is determined by the magnitude of resistor R_S:

$$|V_{O\,MAX}| = 10\mu A\,(R_S)$$

If the output of the amplifier is to be abruptly changed more than 6V, a PNP transistor should be connected, as shown in *Figure 3*, to prevent the slew rate of the output from exceeding the slew rate of the sense stage. If this precaution is not taken, the base-emitter junction of the input transistor in the sense stage will transiently break down and its β will degrade, resulting in a permanent negative shift in output offset voltage.

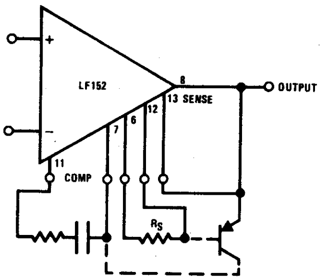


FIGURE 3. Large Signal Transient Suppression

OFFSET VOLTAGE

Because of the two stage design of the instrumentation amplifier, there are two independent contributors to offset voltage (V_{OS}). The output offset (V_{OOS}) is independent of gain while the input offset (V_{IOS}) is multiplied by the gain of the amplifier to the output.

$$V_{OS} = V_{IOS}\,(G) + V_{OOS}$$

The output offset of the LF152 can be adjusted as shown in *Figure 2*. In addition, the LF152 features input offset adjust which is not common to monolithic instrumentation amplifiers and is normally available only on expensive modules. The simple adjust scheme shown in *Figure 5* has only a slight increase in non-linearity compared to that of *Figure 4* and is recommended for most applications. Nulling both input and output offset makes the overall offset zero, independent of gain.

The output offset is affected by adjustment of the input offset. For every mV of input offset adjust, the output offset will change by approximately 32 mV. Adjustment of the output offset has no effect on the input offset, so it should always be done last.

Offset adjustment changes the temperature coefficient of the V_{OS} drift. The typical input offset drift of the unadjusted device is −10μV/°C. If the input offset is adjusted, the V_{IOS} drift increases by approximately

$$V_{IOS}\text{ drift} \approx -10\mu V/°C + 2\mu V/°C/(\text{mV of adjustment})$$

The V_{OOS} drift will be improved by output offset adjust because the magnitudes of the current sources adjusted become less sensitive to V_{BE} variations. If V_{OOS} adjust is not used, pins 1, 2 and 16 must be shorted to the positive supply for circuit operation.

OFFSET VOLTAGE ADJUSTMENT PROCEDURE

For gains less than 100, only output offset adjustment is needed. For gains greater than 100, input offset adjust is usually necessary since the input offset voltage amplified to the output may be out of the range of the output offset adjust. Input offset adjust is also needed if zero overall offset is desired while varying the amplifier gain.

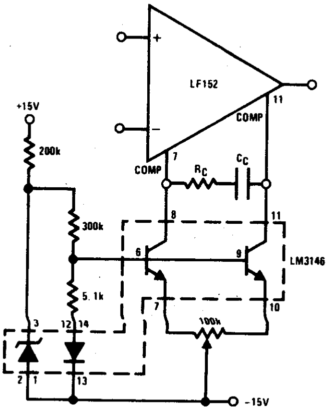


FIGURE 4. Input Offset Adjust

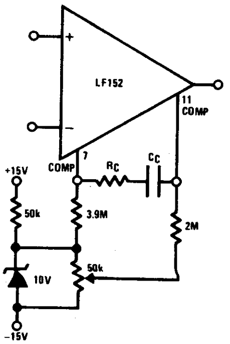


FIGURE 5. Simple Input Offset Adjust

application hints (con't)

To adjust the input offset, the following procedure should be used:

The effective input offset voltage appears directly across R_G when both inputs are connected to ground, and can be measured by a voltmeter referenced to ground. This offset error across R_G can be zeroed by the input offset adjustment circuit shown in *Figure 4 or 5.* The remaining error at the output is strictly due to the output offset voltage which can then be nulled out with the circuit shown in *Figure 2.* The amplifier is now offset nulled independent of gain.

COMPENSATION

The variable bandwidth and slew rate of the LF152 are controlled by an RC network between the compensation pins of the amplifier as shown in *Figure 2.* R_C and C_C may be varied for optimum operating characteristics in a particular application.

Layout of accompanying circuitry may influence the value of this RC network. The lead lengths to resistors R_S and R_G should be minimized and the capacitance from these nodes should also be minimized for optimum frequency response. If $R_C = 160\Omega$ and $C_C = 0.002\mu F$ in the printed circuit board of *Figure 7*, the amplifier will be compensated for all gains from 1 to 1000. Gains from 0.1 to 10,000 may be obtained with different compensation.

GAIN ERROR AND NONLINEARITY

Gain error of the LF152 is the error between the average slope of the transfer function compared to the slope of R_S/R_G. In the LF152, the small gain error is essentially constant with gain and may be nulled out by trimming R_S.

Of the existing monolithic instrumentation amplifiers, the LF152 is among the lowest in gain nonlinearity error. Gain nonlinearity is the curvature of the transfer function from the theoretically perfect function as shown in *Figure 6.*

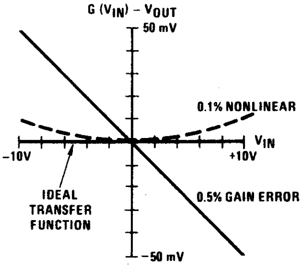


FIGURE 6. Gain Error and Nonlinearity

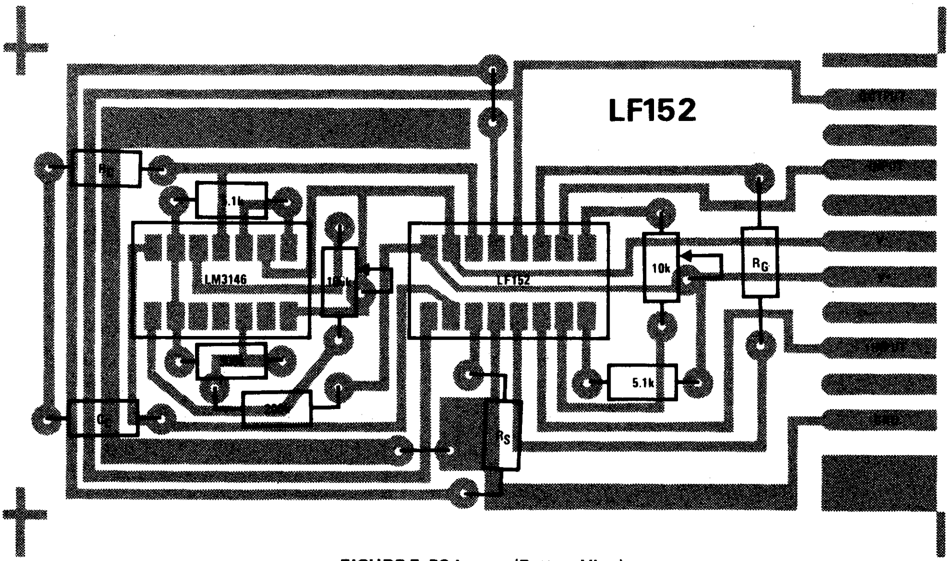
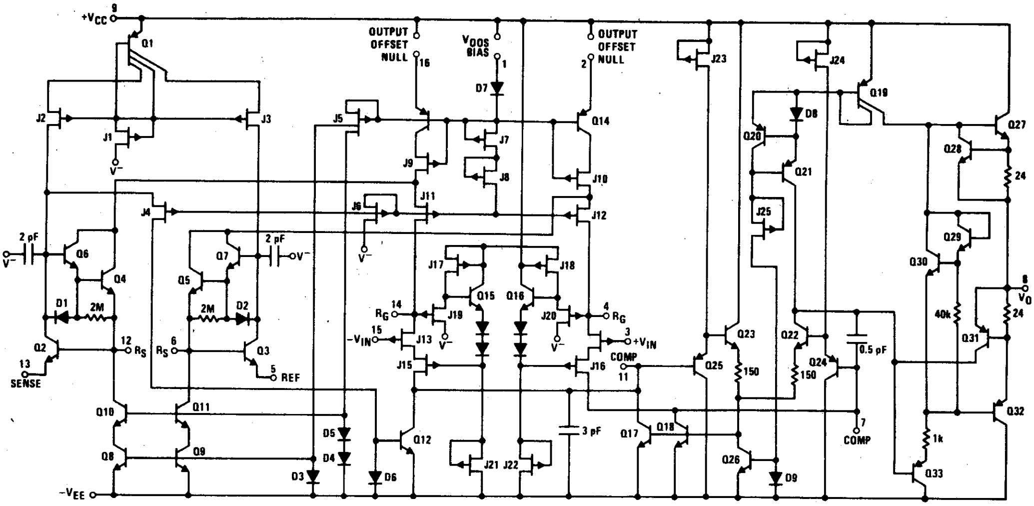


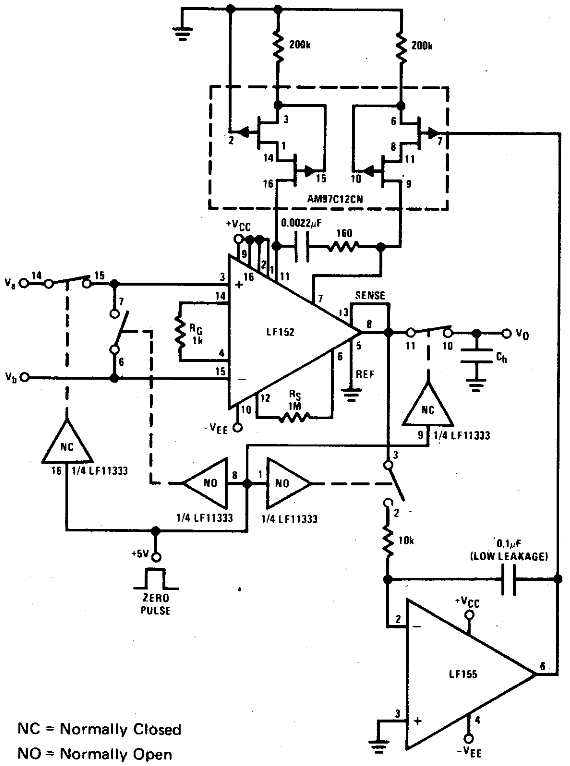
FIGURE 7. PC Layout (Bottom View)

detailed schematic



typical applications

Automatic V_{IOS} Adjust ($G \geq 100$)

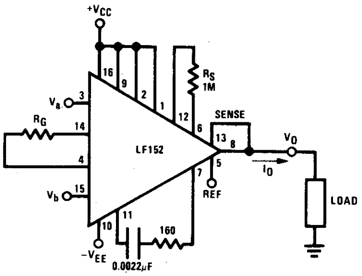


NC = Normally Closed

NO = Normally Open

Minimum pulse width to drive V_O to zero is 400µs.

General Purpose Instrumentation Amplifier



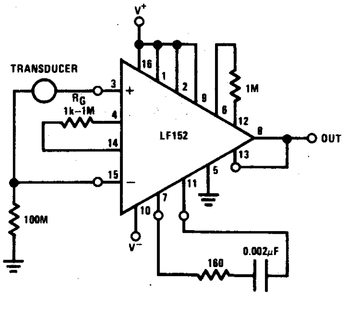
$$V_O = (V_a - V_b)\frac{R_S}{R_G} + V_{REF}$$

For $\frac{R_S}{R_G} = 1$

$V_O = V_a + V_{REF} - V_b$

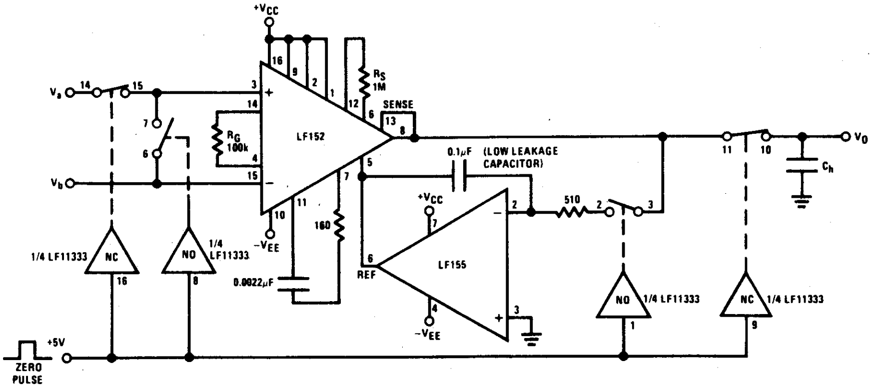
I_O SOURCE OR SINK $\leq$ 5 mA

Isolated Sensor



typical applications (con't)

Automatic V_{OOS} Adjust (For G ≤ 100)

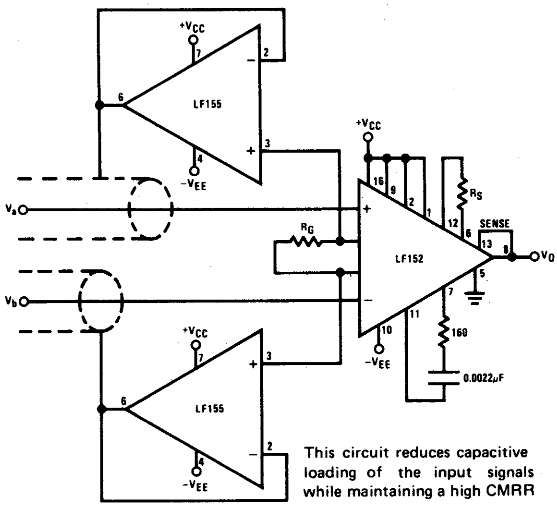


Minimum pulse width to drive V_O to zero is 450µs

NC = Normally Closed

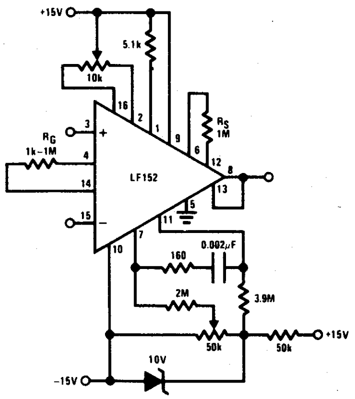
NO = Normally Open

AC Active Guard Drive

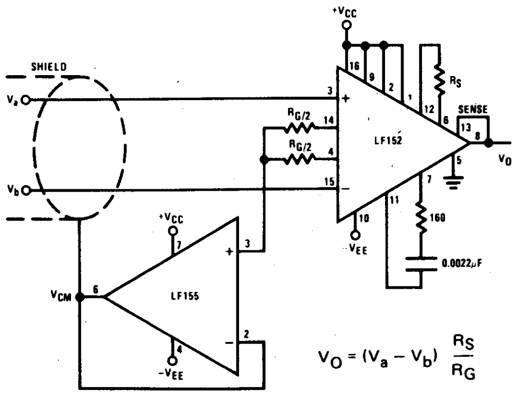


This circuit reduces capacitive loading of the input signals while maintaining a high CMRR

Typical Circuit with Full Offset Adjust



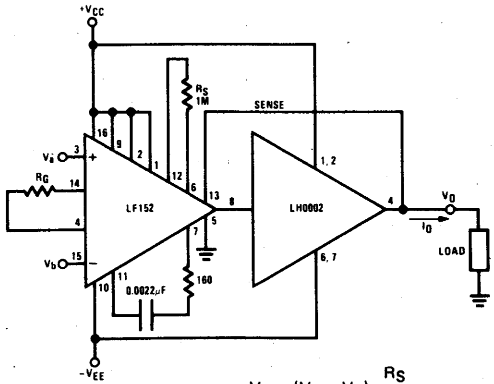
Active Guard Drive



$$V_O = (V_a - V_b)\ \frac{R_S}{R_G}$$

(This circuit reduces the degradation of CMRR caused by the capacitance of shielded cable.)

Output Current Boost

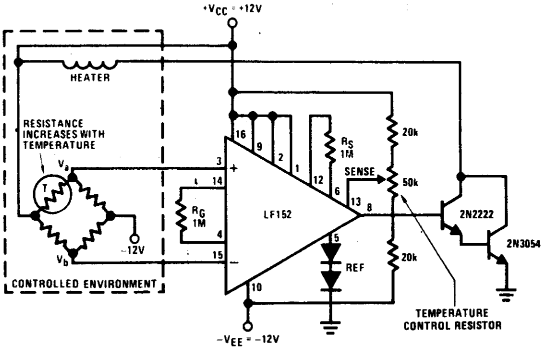


$$V_O = (V_a - V_b)\ \frac{R_S}{R_G}$$

I_O SOURCE OR SINK ≤ 95 mA

typical applications (con't)

Temperature Control Circuit

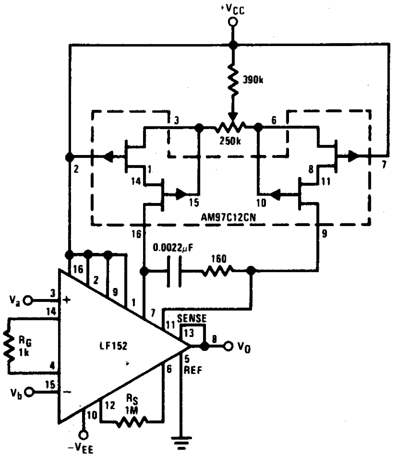


Under balanced conditions, $V_{SENSE} - V_{REF}$ appears across R_S, $V_a - V_b$ appears across R_G and $I_{RG} = I_{RS}$.

$$\frac{V_a - V_b}{R_G} = \frac{V_{SENSE}}{R_S} \text{ or } V_a - V_b = V_{SENSE} \frac{R_G}{R_S}$$

V_{SENSE} is fixed by the temperature control resistor and R_G/R_S is constant. The LF152 is used as a comparator with a feedback loop closed through the heater and the temperature dependent resistor. If $V_a - V_b > V_{SENSE}\ R_G/R_S$. The output goes high turning "ON" the heater. If $V_a - V_b < V_{SENSE}\ R_G/R_S$. The output goes low turning "OFF" the heater.

Alternate Input Offset (V_{IOS}) Adjust Scheme



definition of terms

G **Closed loop gain.** $G = R_S/R_G$

G_E **Gain error.** A rotational error of the transfer function about the origin.

G_{NL} **Gain nonlinearity.** Curvature of the transfer function.

V_{OS} **Offset voltage.** Voltage offset of the transfer function at the origin $V_{OS} = V_{IOS}(G) + V_{OOS}$