Operational Amplifiers

LH0023/LH0023C, LH0043/LH0043C
sample and hold circuits
general description

The LH0023/LH0023C and LH0043/LH0043C are complete sample and hold circuits including input buffer amplifier, FET output amplifier, analog signal sampling gate, TTL compatible logic circuitry and level shifting. They are designed to operate from standard ±15V DC supplies, but provision is made on the LH0023/LH0023C for connection of a separate +5V logic supply in minimum noise applications. The principal difference between the LH0023/LH0023C and the LH0043/LH0043C is a 10:1 trade-off in performance on sample accuracy vs sample acquisition time. Devices are pin compatible except that TTL logic is inverted between the two types.

The LH0023/LH0023C and LH0043/LH0043C are ideally suited for a wide variety of sample and

hold applications including data acquisition, analog to digital conversion, synchronous demodulation, and automatic test setup. They offer significant cost and size reduction over equivalent module or discrete designs. Each device is available in a hermetic TO-8 package and are completely specified over both full military and instrument temperature ranges.

The LH0023 and LH0043 are specified for operation over the –55°C to +125°C military temperature range. The LH0023C and LH0043C are specified for operation over the –25°C to +85°C temperature range.
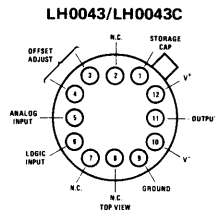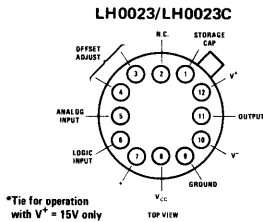
features
LH0023/LH0023C
- Sample accuracy–0.01% max
- Hold drift rate–0.5 mV/sec typ
- Sample acquisition time–100 μs max for 20V
- Aperture time–150 ns typ
- Wide analog range–±10V min
- Logic input–TTL/DTL
- Offset adjustable to zero with single 10k pot
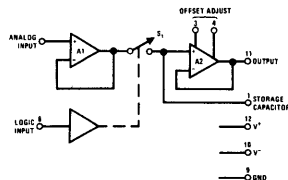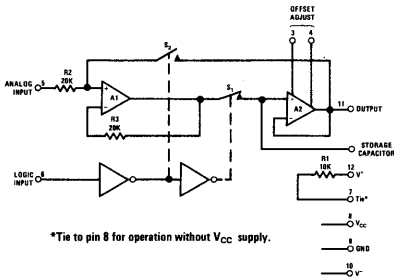- Output short circuit proof

features
LH0043/LH0043C
- Sample acquisition time–15 μs max for 20V
  4 μs typ for 5V
- Aperture time–20 nS typ
- Hold drift rate–1 mV/sec typ
- Sample accuracy–0.1% max
- Wide analog range–±10V min
- Logic input–TTL/DTL
- Offset adjustable to zero with single 10k pot
- Output short circuit proof

block and connection diagrams

LH0023/LH0023C

LH0043/LH0043C

Order Number LH0023G or
LH0023CG or LH0043G or
LH0043CG
See Package 6

*Tie for operation
with V⁺ = 15V only   TOP VIEW

*Tie to pin 8 for operation without V_CC supply.

absolute maximum ratings

Supply Voltage (V$^+$ and V$^-$)	±20V
Logic Supply Voltage (V$_{CC}$) LH0023, LH0023C	+7.0V
Logic Input Voltage (V$_6$)	+5.5V
Analog Input Voltage (V$_5$)	±15V
Power Dissipation	See graph
Output Short Circuit Duration	Continuous
Operating Temperature Range LH0023, LH0043	−55°C to +125°C
LH0023C, LH0043C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Soldering (10 sec)	300°C

electrical characteristics LH0023/LH0023C (Note 1)

PARAMETER	CONDITIONS	LH0023 MIN	LH0023 TYP	LH0023 MAX	LH0023C MIN	LH0023C TYP	LH0023C MAX	UNITS
Sample (Logic "1") Input Voltage	V$_{CC}$ = 4.5V	2.0			2.0			V
Sample (Logic "1") Input Current	V$_6$ = 2.4V, V$_{CC}$ = 5.5V			5.0			5.0	μA
Hold (Logic "0") Input Voltage	V$_{CC}$ = 4.5V			0.8			0.8	V
Hold (Logic "0") Input Current	V$_6$ = 0.4V, V$_{CC}$ = 5.5V			0.5			0.5	mA
Analog Input Voltage Range		±10	±11		±10	±11		V
Supply Current – I$_{10}$	V$_5$ = 0V, V$_6$ = 2V, V$_{11}$ = 0V		4.5	6		4.5	6	mA
Supply Current – I$_{12}$	V$_5$ = 0V, V$_6$ = 0.4V, V$_{11}$ = 0V		4.5	6		4.5	6	mA
Supply Current – I$_8$	V$_8$ = 5.0V, V$_5$ = 0		1.0	1.6		1.0	1.6	mA
Sample Accuracy	V$_{OUT}$ = ±10V (Full Scale)		0.002	0.01		0.002	0.02	%
DC Input Resistance	Sample Mode	500	1000		300	1000		kΩ
	Hold Mode	20	25		20	25		kΩ
Input Current – I$_5$	Sample Mode		0.2	1.0		0.3	1.5	μA
Input Capacitance			3.0			3.0		pF
Leakage Current – pin 1	V$_5$ = ±10V; V$_{11}$ = ±10V, T$_A$ = 25°C		100	200		200	500	pA
	V$_5$ = ±10V; V$_{11}$ = ±10V		0.6	1.0		1.0	2	nA
Drift Rate	V$_{OUT}$ = ±5V, C$_S$ = 0.01 μF, T$_A$ = 25°C		0.5			0.5		mV/s
Drift Rate	V$_{OUT}$ = ±10V, C$_S$ = 0.01 μF, T$_A$ = 25°C		10	20		20	50	mV/s
Drift Rate	V$_{OUT}$ = ±10V, C$_S$ = 0.01 μF			0.1			0.2	mV/ms
Aperture Time			150			150		ns
Sample Acquisition Time	ΔV$_{OUT}$ = 20V, C$_S$ = 0.01 μF		50	100		50	100	μs
Output Amplifier Slew Rate		1.5	3.0		1.5	3.0		V/μs
Output Offset Voltage (without null)	R$_S$ ≤ 10k, V$_5$ = 0V, V$_6$ = 0V			±20			±20	mV
Analog Voltage Output Range	R$_L$ ≥ 1k, T$_A$ = 25°C	±10	±11		±10	±11		V
	R$_L$ ≥ 2k	±10	±12		±10	±12		V

Note 1: Unless otherwise noted, these specifications apply for V$^+$ = +15V, V$_{CC}$ = +5V, V$^-$ = −15V, pin 9 grounded, a 0.01μF capacitor connected between pin 1 and ground over the temperature range −55°C to +125°C for the LH0023, and −25°C to +85°C for the LH0023C. All typical values are for T$_A$ = 25°C.

electrical characteristics LH0043/LH0043C: (Note 2)

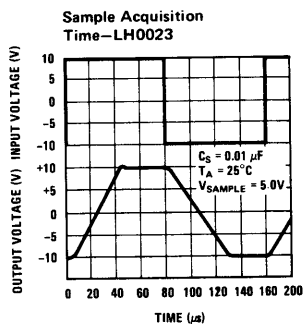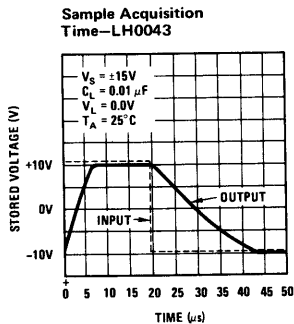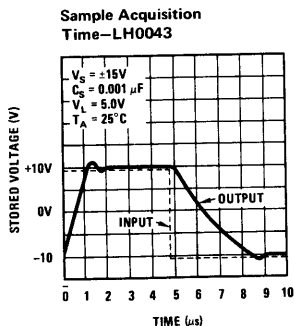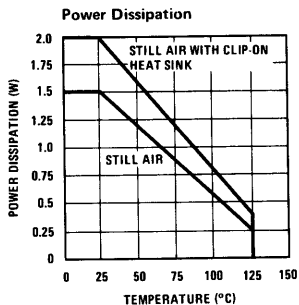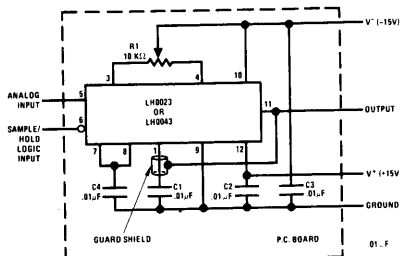| PARAMETER	CONDITIONS	LH0043			LH0043C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Hold (Logic "1") Input Voltage		2.0			2.0			V
Hold (Logic "1") Input Current	$V_6 = 2.4V$			5.0			5.0	μA
Sample (Logic "0") Input Voltage				0.8			0.8	V
Sample (Logic "0") Input Current	$V_6 = 0.4V$			1.5			1.5	mA
Analog Input Voltage Range		±10	±11		±10	±11		V
Supply Current	$V_5 = 0V, V_6 = 2V, V_{11} = 0V$ $V_5 = 0V, V_6 = 0.4V,$ $V_{11} = 0V$		20 14	22 18		20 14	22 18	mA mA
Sample Accuracy	$V_{OUT} = ±10V$ (Full Scale)		0.02	0.1		0.02	0.3	%
DC Input Resistance	$T_C = 25°C$	10^{10}	10^{12}		10^{10}	10^{12}		Ω
Input Current − I_5			1.0	5.0		2.0	10.0	nA
Input Capacitance			1.5			1.5		pF
Leakage Current− pin 1	$V_5 = ±10V; V_{11} = ±10,$ $T_C = 25°C$ $V_5 = ±10V; V_{11} = ±10V$		10 10	25 25		20 2	50 5	pA nA
Drift Rate	$V_{OUT} = ±10V, C_S = 0.001 \mu F,$ $T_A = 25°C$		10	25		20	50	mV/s
Drift Rate	$V_{OUT} = ±10V, C_S = 0.001 \mu F$		10	25		2	5	mV/ms
Drift Rate	$V_{OUT} = ±10V, C_S = 0.01 \mu F,$ $T_A = 25°C$		1	2.5		2	5	mV/s
Drift Rate	$V_{OUT} = ±10V, C_S = 0.01 \mu F$		1	2.5		0.2	0.5	mV/ms
Aperture Time			20	60		20	60	ns
Sample Acquisition Time	$\Delta V_{OUT} = 20V, C_S = 0.001 \mu F$ $\Delta V_{OUT} = 20V, C_S = 0.01 \mu F$ $\Delta V_{OUT} = 5V, C_S = 0.001 \mu F$		10 30 4	15 50		10 30 4	15 50	μs μs μs
Output Amplifier Slew Rate	$V_{OUT} = 5V, C_S = 0.001 \mu F$	1.5	3.0		1.5	3.0		V/μs
Output Offset Voltage (without null)	$R_S \leq 10k, V_5 = 0V, V_6 = 0V$			±40			±40	mV
Analog Voltage Output Range	$R_L \geq 1k, T_A = 25°C$ $R_L \geq 2k$	±10 ±10	±11 ±12		±10 ±10	±11 ±12		V V

Note 2: Unless otherwise noted, these specifications apply for $V^+ = +15V$, $V^- = -15V$, pin 9 grounded, a 5000 pF capacitor connected between pin 1 and ground over the temperature range −55°C to +125°C for the LH0043, and −25°C to +85°C for the LH0043C. All typical values are for $T_C = 25°C$.

typical performance characteristics

Power Dissipation

STILL AIR WITH CLIP-ON HEAT SINK

STILL AIR

POWER DISSIPATION (W) — TEMPERATURE (°C)

Sample Acquisition Time—LH0043

$V_S = \pm 15V$
$C_S = 0.001\ \mu F$
$V_L = 5.0V$
$T_A = 25°C$

STORED VOLTAGE (V) — TIME (μs)

OUTPUT
INPUT

Sample Acquisition Time—LH0043

$V_S = \pm 15V$
$C_L = 0.01\ \mu F$
$V_L = 0.0V$
$T_A = 25°C$

STORED VOLTAGE (V) — TIME (μs)

OUTPUT
INPUT

Sample Acquisition Time—LH0023

$C_S = 0.01\ \mu F$
$T_A = 25°C$
$V_{SAMPLE} = 5.0V$

OUTPUT VOLTAGE (V)   INPUT VOLTAGE (V) — TIME (μs)

Pin 1 Leakage Current vs Output Voltage

$V_S = \pm 15V$
$T_A = 25°C$

PIN 1 LEAKAGE (pA) — OUTPUT VOLTAGE (V)

Pin 1 Leakage Current vs Temperature

$V_{OUT} = -10$
$V_{OUT} = 0$
$V_{OUT} = +10$

PIN 1 LEAKAGE CURRENT (nA) — TEMPERATURE (°C)

Output Current Limiting

$V_S = \pm 15V$

$T_A = 125°C$ $T_A = 25°C$

OUTPUT SWING ($\pm V$) — OUTPUT CURRENT ($\pm mA$)

Drift Rate vs Capacitance

$V_{OUT} = \pm 10V$
$T_A = 125°C$
$V_{OUT} = \pm 10V$
$T_A = 25°C$
$V_{OUT} = \pm -5V$
$T_A = 25°C$

DRIFT RATE (mV/sec) — C_S – CAPACITANCE (μF)

Drift vs Capacitance (LH0043)

$V_S = \pm 15$
$V_{OUT} = \pm 10$

$T_C = +125°C$

$T_C = 25°C$

DRIFT RATE (mV/s) — CAPACITANCE (μF)

typical applications

R1
10 KΩ

ANALOG INPUT

SAMPLE/ HOLD LOGIC INPUT

LH0023 OR LH0043

V⁻ (-15V)

OUTPUT

V⁺ (+15V)

GROUND

C4 .01 μF   C1 .01 μF   C2 .01 μF   C3 .01 μF

GUARD SHIELD   P.C. BOARD

.01 μF
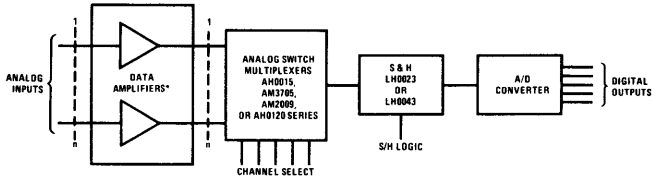
Note 1: C1 is polystyrene.
Note 2: C2, C3, C4 are cermic disc.
Note 3: Jumper 7—8 and C4 not required for LH0043.
Note 4: R1 optional if zero trim is required.

How to Build a Sample and Hold Module

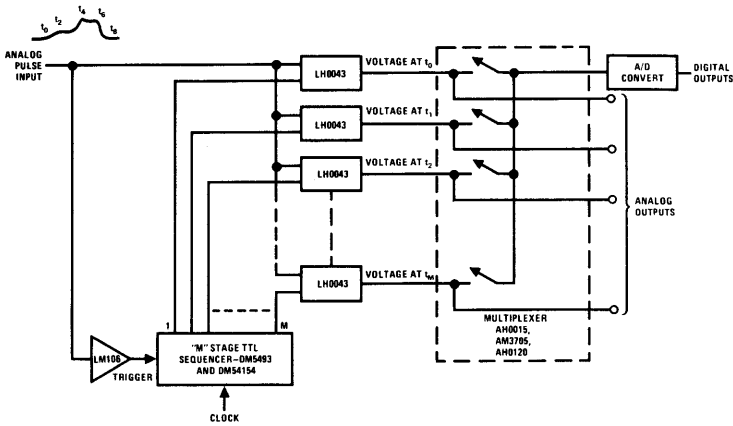# typical applications (con't)
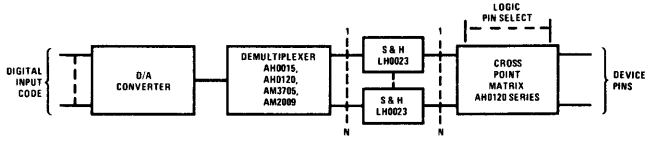
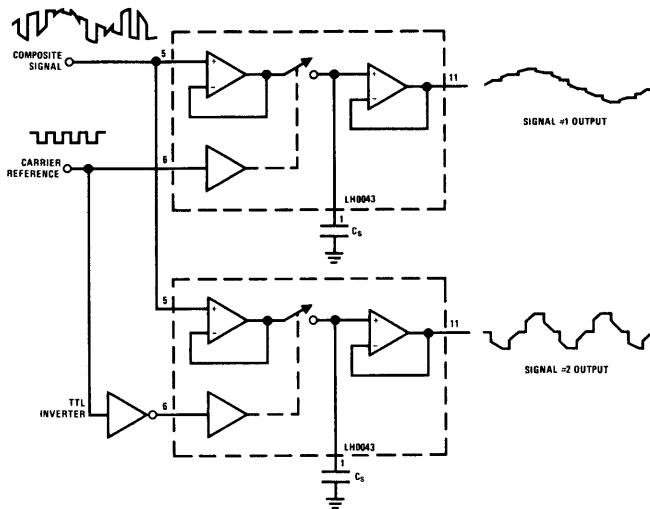**Forcing Function Setup for Automatic Test Gear**

*See op amp selection guide for details. Most popular types include LH0052, LH175, LM108, LM112 and LM116.
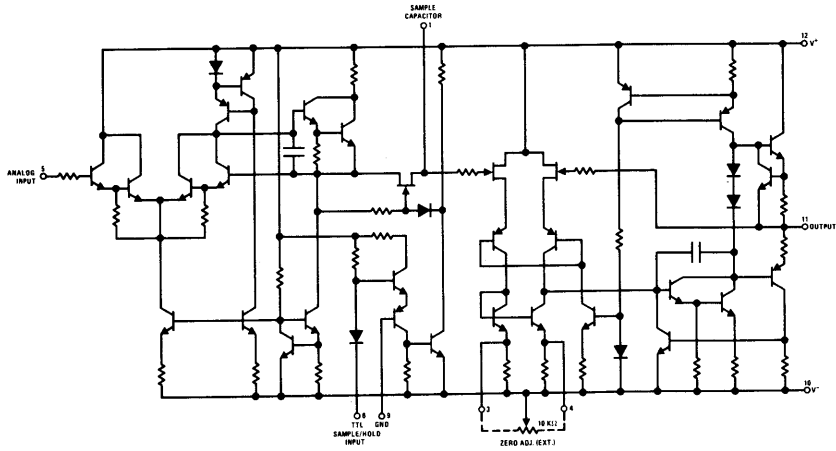
Data Acquisition System
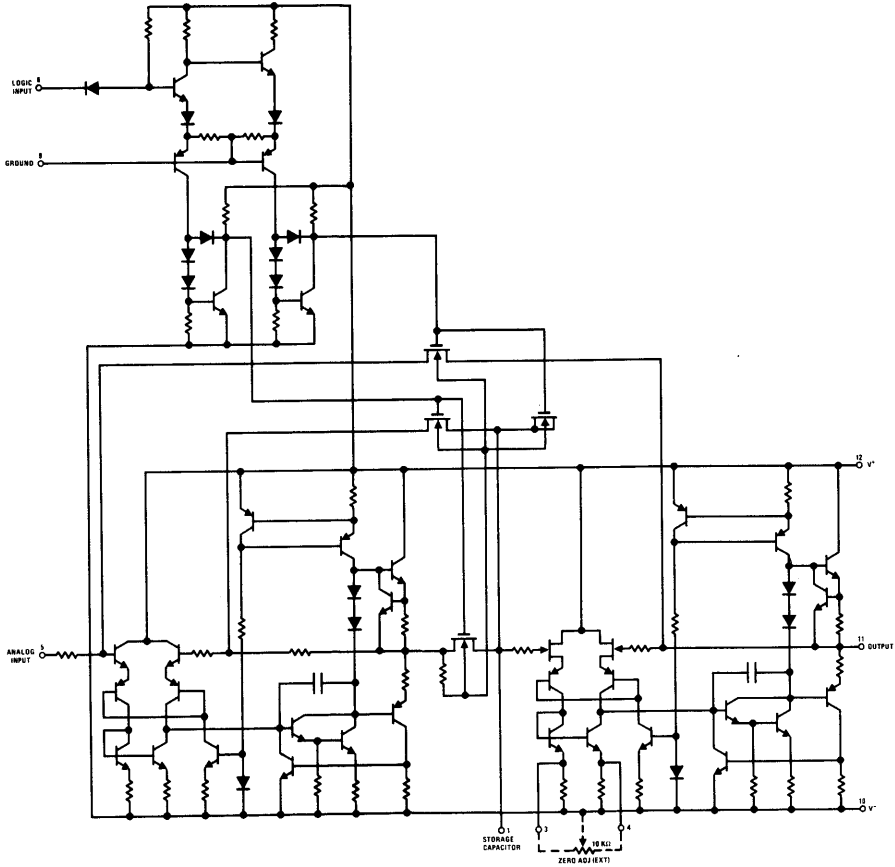

Single Pulse Sampler

Two Channel Double Sideband Demodulator

schematic diagrams

LH0043/LH0043C

LH0023/LH0023C

2

applications information

1.0 Drift Error Minimization

In order to minimize drift error, care in selection of C_S and layout of the printed circuit board is required. The capacitor should be of high quality Teflon, polycarbonate, or polystyrene construction. Board cleanliness and layout are critical particularly at elevated temperatures. See AN-63 for detailed recommendations. A guard conductor connected to the output surrounding the storage node (pin 1) will be helpful in meeting severe environmental conditions which would otherwise cause leakage across the printed circuit board.

2.0 Capacitor Selection

The size of the capacitor is dictated by the required drift rate and acquisition time. The drift is determined by the leakage current at pin 1 and may be calculated by $\dfrac{dV}{dt} = \dfrac{I_L}{C_S}$, where I_L is the total leakage current at pin 1 of the device, and C_S is the value of the storage capacitor.

2.1 Capacitor Selection — LH0023

At room temperature leakage current for the LH0023 is approximately 100 pA. A drift rate of 10 mV/sec would require a 0.01 μF capacitor.

For values of C_S up to 0.01 μF the acquisition time is limited by the slew rate of the input buffer amplifier, A1, typically 0.5 V/μs. Beyond this point, current availability to charge C_S also enters the picture. The acquisition time is given by:

$$t_A \cong \sqrt{\frac{2\Delta e_O\,RC_S}{0.5 \times 10^6}} = 2 \times 10^{-3}\sqrt{\Delta e_O\,RC_S}$$

where: R = the internal resistance in series with C_S

Δe_O = change in voltage sampled

An average value for R is approximately 600 ohms. The expression for t_A reduces to:

$$t_A \cong \frac{\sqrt{\Delta e_O\,C_S}}{20}$$

For a −10V to +10V change and C_S = .05 μF, acquisition time is typically 50 μs.

2.2 Capacitor Selection—LH0043

At 25°C case temperature, the leakage current for the LH0043G is approximately 10 pA, so a drift rate of 5 mV/s would require a capacitor of $C_S = 10 \cdot 10^{-12}/5 \cdot 10^{-3} = 2000$ pF or larger.

For values of C_S below about 5000 pF, the acquisition time of the LH0043G will be limited by the slew rate of the output amplifier (the signal will be acquired, in the sense that the voltage will be stored on the capacitor, in much less time as dictated by the slew rate and current capacity of the input amplifier, but it will not be available at the output). For larger values of storage capacitance, the limitation is the current sinking capability of the input amplifier, typically 10 mA. With C_S = 0.01 μF, the slew rate can be estimated by $\dfrac{dV}{dt} = \dfrac{10 \cdot 10^{-3}}{0.01 \cdot 10^{-6}} = 1V/\mu s$ or a slewing time for a 5 volt signal change of 5μs.

3.0 Offset Null

Provision is made to null both the LH0023 and LH0043 by use of a 10k pot between pins 3 and 4. Offset null should be accomplished in the sample mode at one half the input voltage range for minimum average error.

4.0 Switching Spike Minimization—LH0043

A capacitive divider is formed by the storage capacitor and the capacitance of the internal FET switch which causes a small error current to be injected into the storage capacitor at the termination of the sample interval. This can be considered a negative DC offset and nulled out as described in (3.0), or the transient may be nulled by coupling an equal but opposite signal to the storage capacitor. This may be accomplished by connecting a capacitor of about 30 pF (or a trimmer) between the logic input (pin 6) and the storage capacitor (pin 1). Note that this capacitor must be chosen as carefully as the storage capacitor itself with respect to leakage. The LH0023 has switch spike minimization circuitry built into the device.

5.0 Elimination of the 5V Logic Supply—LH0023

The 5V logic supply may be eliminated by shorting pin 7 to pin 8 which connects a 10k dropping resistor between the +15V and V_C. Decoupling pin 8 to ground through 0.1 μF disc· capacitor is recommended in order to minimize transients in the output.

6.0 Heat Sinking

The LH0023 and LH0043G may be operated without damage throughout the military temperature range of −55 to +125°C (−25 to +85°C for the LH0023CG and LH0043CG) with no explicit heat sink, however power dissipation will cause the internal temperature to rise above ambient. A simple clip-on heat sink such as Wakefield #215–1.9 or equivalent will reduce the internal temperature about 20°C thereby cutting the leakage current and drift rate by one fourth at max. ambient. There is no internal electrical connection to the case, so it may be mounted directly to a grounded heat sink.

7.0 Theory of Operation—LH0023

The LH0023/LH0023C is comprised of input buffer amplifier, A1, analog switches, S1 and S2, a

applications information (con't)

TTL to MOS level translator, and output buffer amplifier, A2. In the "sample" mode, the logic input is raised to logic "1" ($V_6 \leq 2.0V$) which closes S1 and opens S2. Storage capacitor, C_S, is charged to the input voltage through S1 and the output slews to the input voltage. In the "hold" mode, the logic input is lowered to logic "0" ($V_6 \leq 0.8V$) opening S1 and closing S2. C_S retains the sample voltage which is applied to the output via A2. Since S1 is open, the input signal is overridden, and leakage across the MOS switch is therefore minimized. With S1 open, drift is primarily determined by input bias current of A2, typically 100 pA at $25°C$.

7.1 Theory of Operation—LH0043

The LH0043/LH0043C is comprised of input buffer amplifier A1, FET switch S1 operated by a TTL compatible level translator, and output buffer amplifier A2. To enter the "sample" mode, the logic input is taken to the TTL logic "0" state ($V_6 = 0.8V$) which commands the switch S1
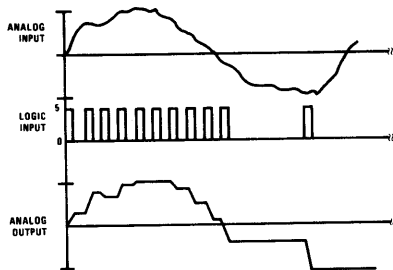
closed and allows A1 to make the storage capacitor voltage equal to the analog input voltage. In the "hold" mode ($V_6 = 2.0V$), S1 is opened isolating the storage capacitor from the input and leaving it charged to a voltage equal to the last analog input voltage before entering the hold mode. The storage capacitor voltage is brought to the output by low leakage amplifier A2.

8.0 Definitions

V_5:　The voltage at pin 5, e.g., the analog input voltage.

V_6:　The voltage at pin 6, e.g., the logic control input signal.

V_{11}:　The voltage at pin 11, e.g., the output signal.

T_A:　The temperature of the ambient air.

T_C:　The temperature of the device case at the center of the bottom of the header.

Acquisition Time:
The time required for the output (pin 11) to settle within the rated accuracy after a specified input change is applied to the input (pin 5) with the logic input (pin 6) in the low state.

Aperture Time:
The time indeterminacy when switching from sample mode to hold including the delay from the time the mode control signal (pin 6) passes through its threshold (1.4 volts) to the time the circuit actually enters the hold mode.

Output Offset Voltage:
The voltage at the output terminal (pin 11) with the analog input (pin 5) at ground and logic input (pin 6) in the "sample" mode. This will always be adjustable to zero using a 10k pot between pins 3 and 4 with the wiper arm returned to V^-.

2