LM1861, LM1862 Linear Frequency Synthesizers

General Description

The LM1861 and LM1862 are linear integrated circuits designed to complement available digital phase locked loop circuits to produce complete frequency synthesizer systems for Class D Citizens Band transceivers. Both circuits include a wide range voltage controlled oscillator with receive or transmit frequency shift, buffers and mixers, and feature output suppression during acquisition of lock. The LM1862 is designed primarily for dual conversion IF amplifier receivers, while the LM1861 is designed for single conversion receivers. The voltage-controlled oscillator, VCO, uses no varactor but relies on external phase shift networks. This results in a predictable, linear frequency control characteristic dependent only on components external to the integrated circuit. Balanced mixers are employed to minimize spurious outputs.

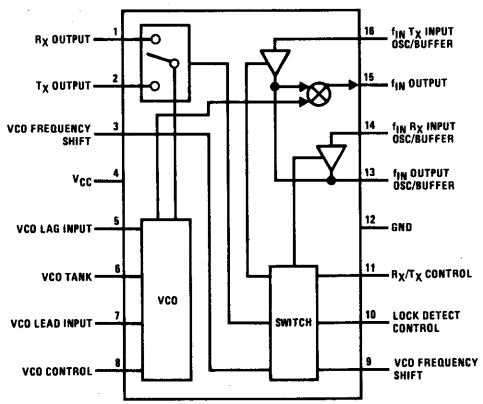
The buffers can be used as crystal oscillators if a multiple crystal system is desired. The receive and transmit outputs are suppressed if an "out of lock" (low) input is received from the phase detector of the PLL circuit. The receive-transmit control pin retunes the VCO to allow fast receive-transmit transfer time as well as suppressing the undesired output. Although designed to complement the MM55108, MM55109, MM55110, MM55111, MM55124 or the MM55126, the LM1861 or LM1862 can be used with any similar digital PLL circuit.

Features

- 1, 2 or 3 crystal system operation
- VCO with no varactor
- Very linear VCO
- Double balanced modulators
- Low VCO input bias current (50 nA typ)
- Lock detect input provided
- Fast receive-transmit transfer time (10 ms typ)

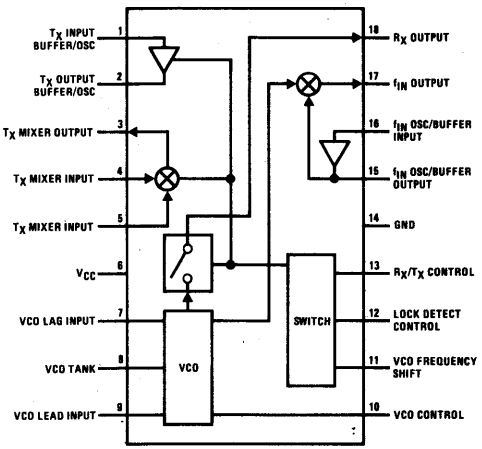
Block and Connection Diagrams

Dual-In-Line Package



Order Number LM1861N
See NS Package N16A

Dual-In-Line Package



Order Number LM1862N
See NS Package N18A

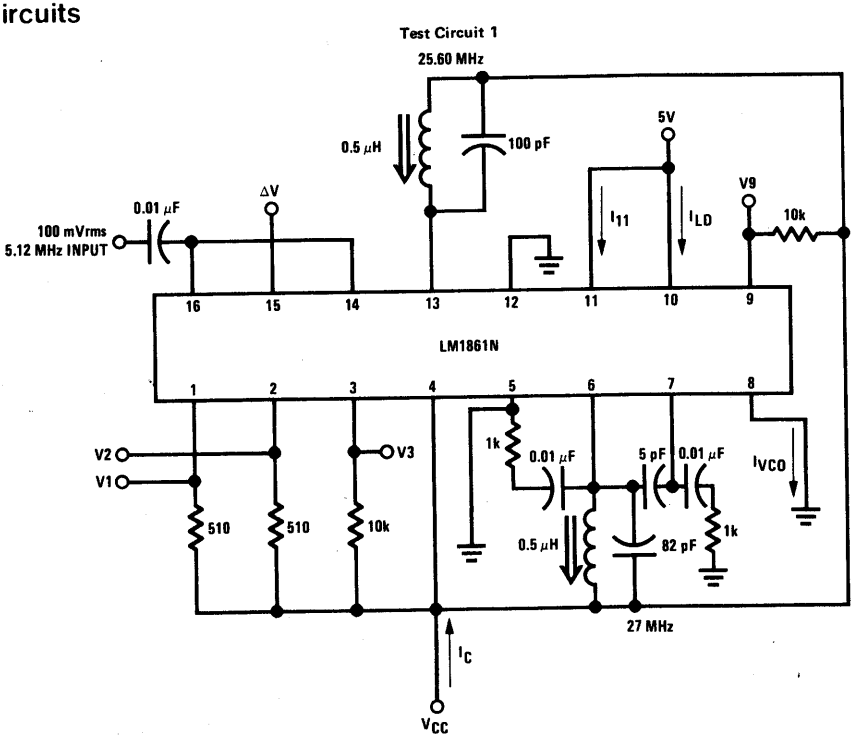
Absolute Maximum Ratings

Supply Voltage	16V
Package Dissipation (Note 1)	1390 mW
Junction Temperature	150°C
Operating Temperature Range	0°C to 85°C
Storage Temperature Range	−65°C to +150°C
Input Voltage	
LM1861, Pins 5, 7, 14, 16	1 Vrms
LM1862, Pins 7, 9, 1, 4, 5, 16	1 Vrms
Input Current	
LM1861, Pins 3, 9	20 mA_{DC}
LM1862, Pin 11	20 mA_{DC}
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics LM1861 $T_A = 25°C$, $V_{CC} = 10V$

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage	Test Circuit 1	8	10	12	V_{DC}
I_C	Supply Current	Test Circuit 1	20		40	mA_{DC}
I_{VCO}	VCO Bias Current	Test Circuit 1		0.05	1	μA_{DC}
I_{11}	I_{IN} Pin 11	Test Circuit 1		0.5	1	mA_{DC}
I_{LD}	I_{IN} Pin 10	Test Circuit 1		0.5	1	mA_{DC}
V3	Saturation Voltage Pin 3	Test Circuit 1, Pin 11 Grounded			0.4	V_{DC}
V9	Saturation Voltage Pin 9	Test Circuit 1			0.4	V_{DC}
V1	Receive Output	Test Circuit 1	0.1			Vp-p
V2	Transmit Output	Test Circuit 1, Pin 11 Grounded	0.1			Vp-p
ΔV	Difference Output	Test Circuit 1	100			mVrms

Test Circuits



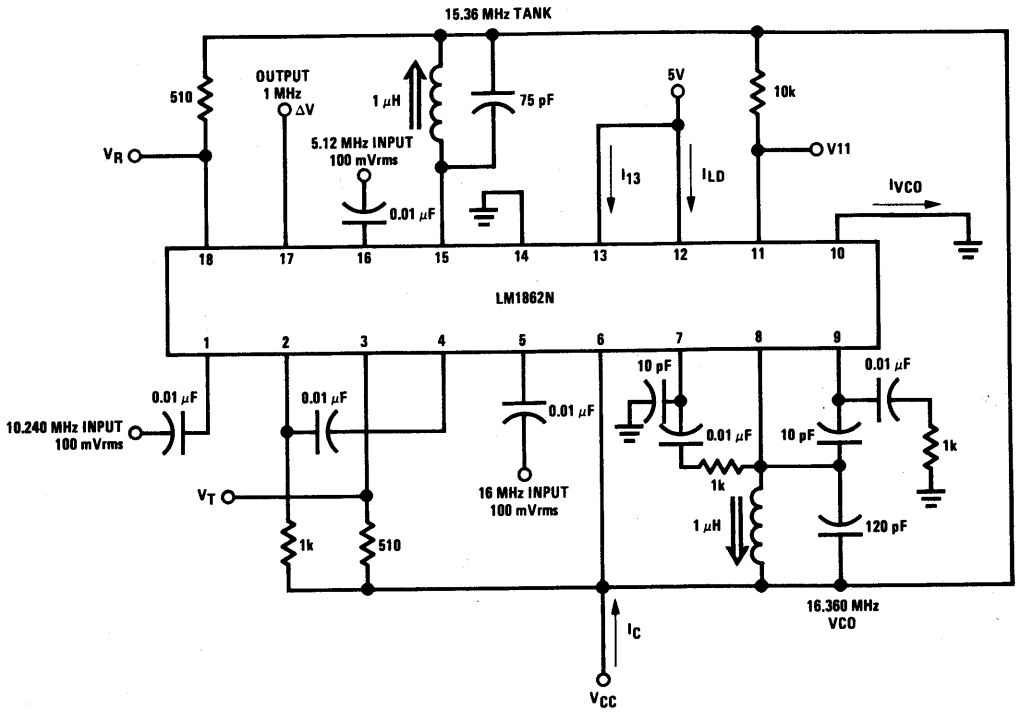
Electrical Characteristics LM1862 $T_A = 25°C$, $V_{CC} = 10V$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage	Test Circuit 2	8	10	12	V_{DC}
I_C	Supply Current	Test Circuit 2	25		45	mA_{DC}
I_{VCO}	VCO Bias Current	Test Circuit 2		0.05	1	μA
I_{LD}	I_{IN} Pin 12	Test Circuit 2		0.5	1	mA
I_{13}	I_{IN} Pin 13	Test Circuit 2		0.5	1	mA
V11	Saturation Voltage Pin 11	Test Circuit 2			0.4	V_{DC}
V_R	Receive Output	Test Circuit 2	0.1			Vp-p
V_T	Transmit Output	Test Circuit 2, Pin 13 Grounded	0.1			Vp-p
ΔV	Difference Output	Test Circuit 2	100			mVrms

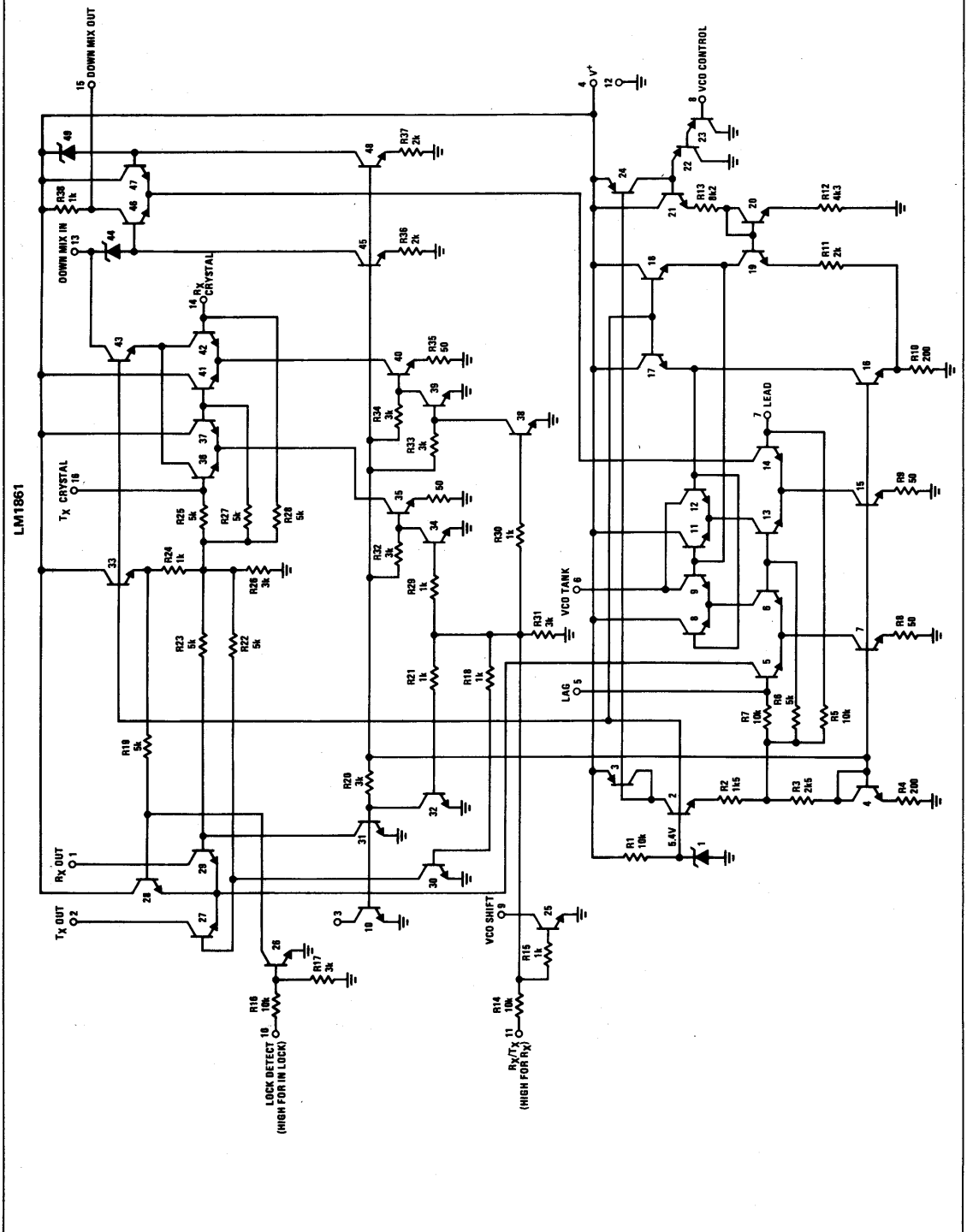
Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 90°C/W junction to ambient.

Test Circuits (Continued)

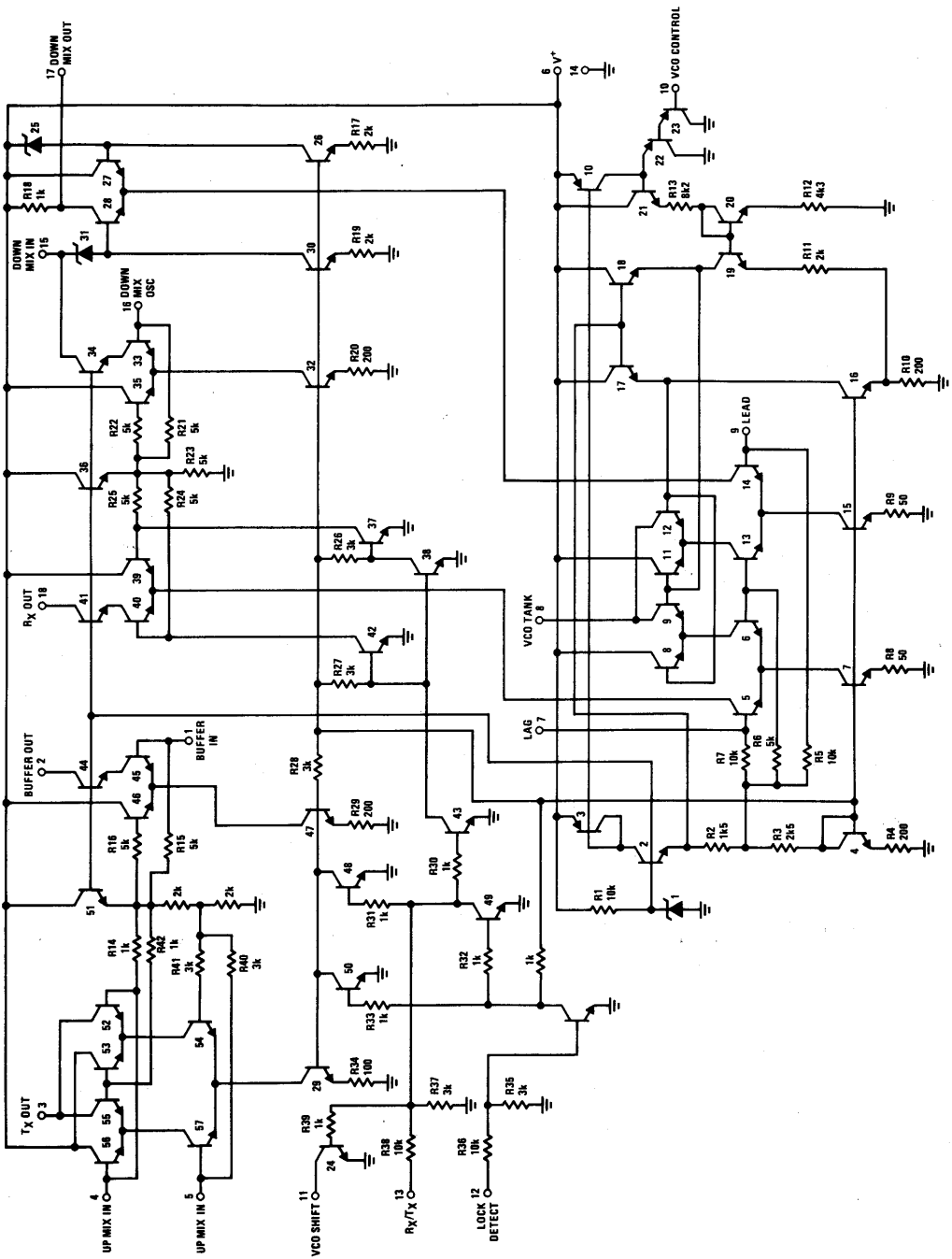
Test Circuit 2



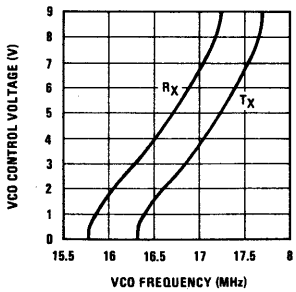
Simplified Schematics

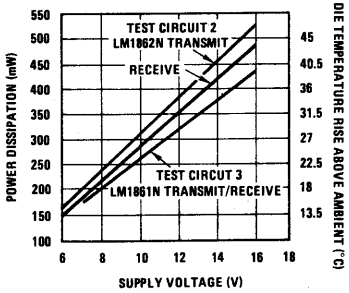


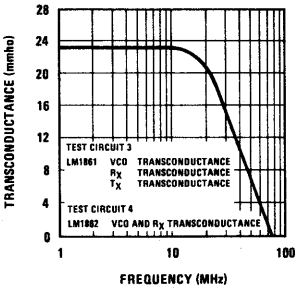
Simplified Schematics (Continued)



Typical Performance Characteristics

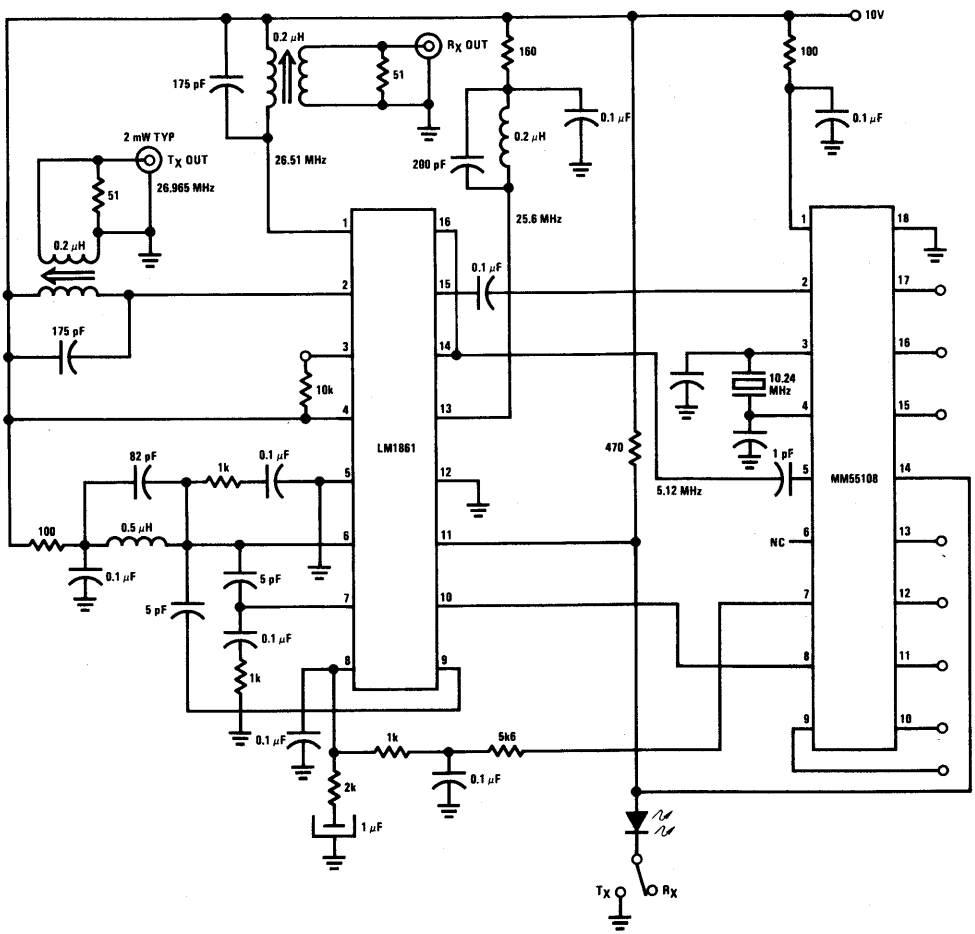






Typical Applications

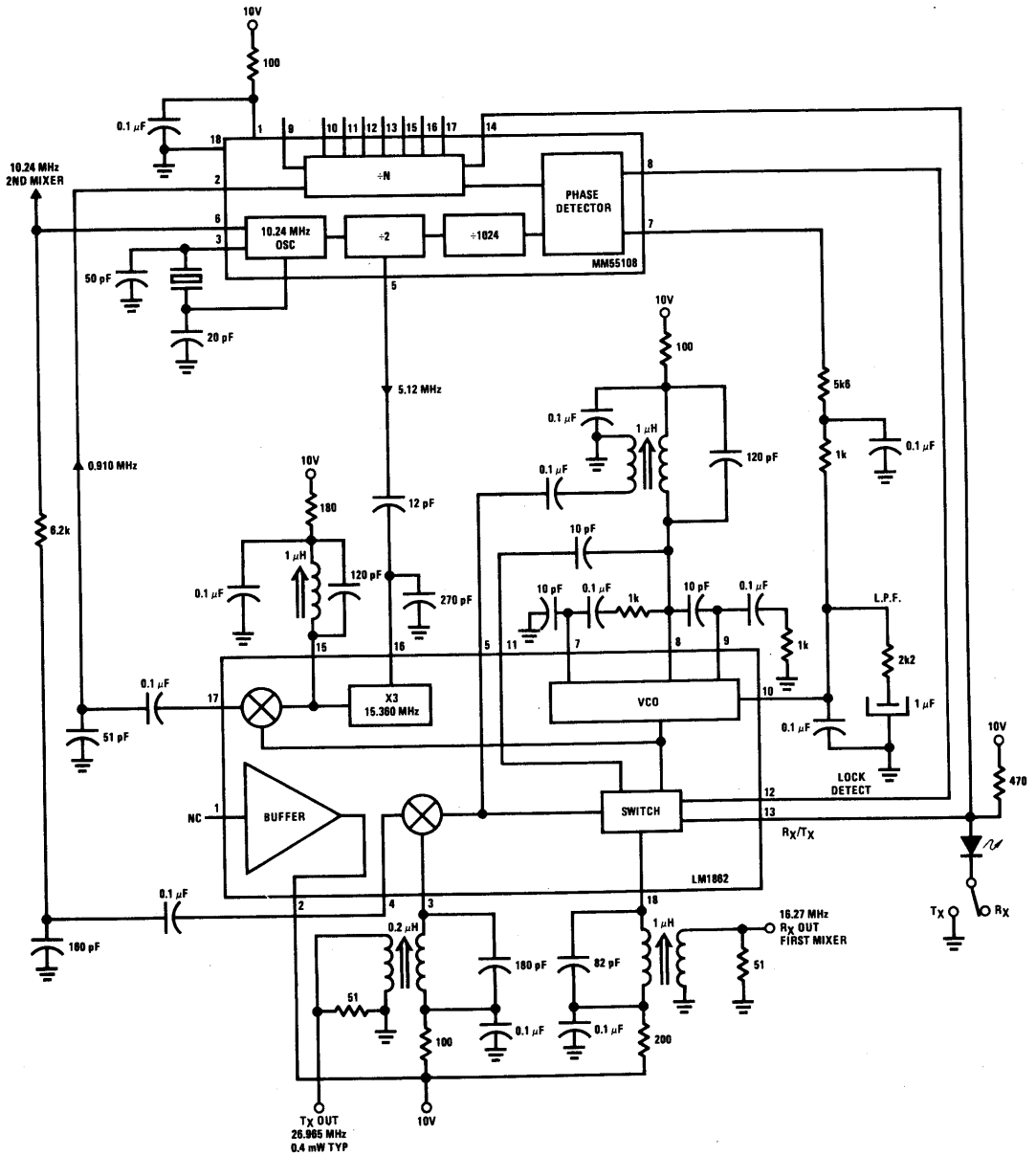
LM1861 Single Conversion Synthesizer



Channel 1 frequencies shown.

Typical Applications (Continued)

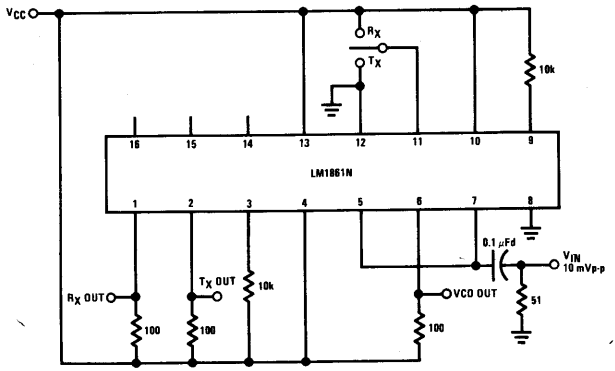
LM1862 Dual Conversion Synthesizer



Channel 1 frequencies shown.

Test Circuits (Continued)

Test Circuit 3



Test Circuit 4