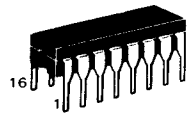
TWO-MODULUS PRESCALER

MC12013
MC12513

Advance Information

The MC12013/MC12513 is a two-modulus prescaler which will divide by 10 and 11. A MECL-to-MTTL translator is provided to interface directly with the MC12014 Counter Control Logic. In addition, the MC12013/MC12513 provides a buffered clock input and MECL bias voltage source. Details of operation are on the MC12012 data sheet.



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

- 600 MHz (typ) Toggle Frequency
- ÷10/11
- MECL to MTTL Translator on Chip
- MECL and MTTL Enable Inputs
- +5.0 or -5.2 V Operation*
- Buffered Clock Input
- V_{BB} Reference Voltage
- 310 Milliwatts (typ)

*When using +5.0 V supply, apply +5.0 V to pin 1 (V_{CCO}), pin 6 (MTTL V_{CC}), pin 16 (V_{CC}), and ground pin 8 (V_{EE}). When using -5.2 V supply, ground pin 1 (V_{CCO}), pin 6 (MTTL V_{CC}), and pin 16 (V_{CC}) and apply -5.2 V to pin 8 (V_{EE}). If the translator is not required, pin 6 may be left open to conserve dc power drain.

PIN ASSIGNMENT

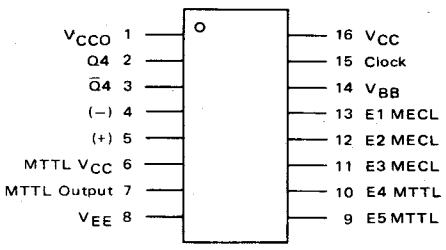


FIGURE 1 – LOGIC DIAGRAM

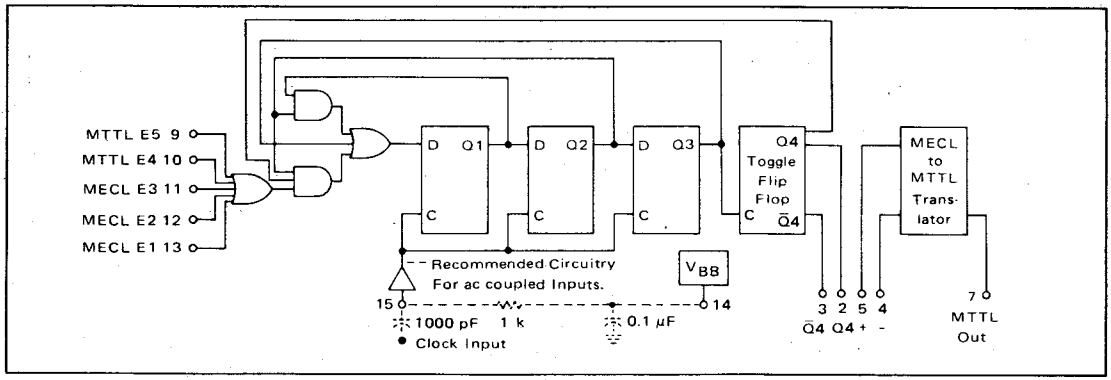
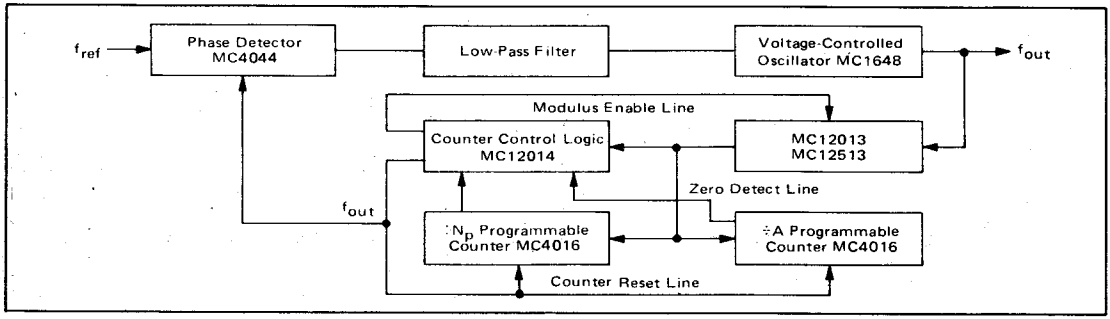


FIGURE 2 – TYPICAL FREQUENCY SYNTHESIZER APPLICATION



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Ratings above which device life may be impaired:			
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8.0	Vdc
Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{ILmin}	Vdc
Output Source Current Continuous Surge	I_O	 <50 <100	mAdc
Storage Temperature Range	T_{stg}	-65 to +175	°C
Recommended maximum ratings above which performance may be degraded:			
Operating Temperature Range	T_A	-30 to +85	°C
DC Fan-Out* (Gates and Flip-Flops)	n	70	–

*AC fan-out is limited by desired system performance.

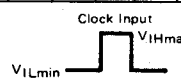
ELECTRICAL CHARACTERISTICS
Supply Voltage -5.2 V

The MC12013 has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50-ohm resistor to -2.0 Vdc.

@Test Temperature	TEST VOLTAGE/CURRENT VALUES: Volts V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{EE}	mA I_L	I_{OL}	I_{OH}
-30°C	-0.890	-1.990	-1.205	-1.500	-2.8	-4.7	-3.2	-4.4	-5.2	-0.25	16	-0.40
+25°C	-0.810	-1.950	-1.105	-1.475	-2.8	-4.7	-3.2	-4.4	-5.2	-0.25	16	-0.40
+85°C	-0.700	-1.925	-1.035	-1.440	-2.8	-4.7	-3.2	-4.4	-5.2	-0.25	16	-0.40

Characteristic	Symbol	Pin Under Test	MC12013 -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OH}	Gnd
Power Supply Drain Current	I_{CC1}	8	–	–	-80	-62	–	–	–	mAdc	–	–	–	–	–	–	–	–	8	–	–	–	1,16
	I_{CC2}	6	–	–	–	–	5.2	–	–	mAdc	4	5	–	–	–	–	–	–	8	–	–	–	6
Input Current	I_{INH1}	15	–	–	–	–	250	–	–	µAdc	15	–	–	–	–	–	–	–	8	–	–	–	1,16
		11	–	–	–	–	↓	–	–	↓	11	–	–	–	–	–	–	–	↓	–	–	–	↓
		12	–	–	–	–		–	–		12	–	–	–	–	–	–	–		–	–	–	
		13	–	–	–	–		–	–		13	–	–	–	–	–	–	–		–	–	–	
	I_{INH2}	4	–	–	2.0	–	5.0	–	–	mAdc	5	4	–	–	–	–	–	–	8	–	–	–	6
		5	–	–	2.0	–	5.0	–	–	mAdc	5	4	–	–	–	–	–	–	8	–	–	–	6
	I_{INH3}	5	–	–	1.0	–	2.5	–	–	mAdc	4	5	–	–	–	–	–	–	8	–	–	–	6
	I_{INH4}	9	–	–	–	–	100	–	–	µAdc	–	–	–	–	9	–	–	–	8	–	–	–	1,16
		10	–	–	–	–	100	–	–	µAdc	–	–	–	–	10	–	–	–	8	–	–	–	1,16
Leakage Current	I_{INL1}	15	–	–	-10	–	–	–	–	µAdc	–	–	–	–	–	–	–	–	8,15	–	–	–	1,16
		11	–	–	↓	–	–	–	–		–	–	–	–	–	–	–	–	8,11	–	–	–	↓
		12	–	–		–	–	–	–		–	–	–	–	–	–	–	–	8,12	–	–	–	
		13	–	–		–	–	–	–		–	–	–	–	–	–	–	–	8,13	–	–	–	
	I_{INL2}	9	-1.6	–	-1.6	–	–	-1.6	–	mAdc	–	–	–	–	–	9	–	–	8	–	–	–	1,16
		10	-1.6	–	-1.6	–	–	-1.6	–	mAdc	–	–	–	–	–	10	–	–	8	–	–	–	1,16
Reference Voltage	V_{BB}	14	–	–	-1.360	–	-1.160	–	–	Vdc	–	–	–	–	–	–	–	–	8	14	–	–	1,16
Logic "1" Output Voltage	V_{OH1} ①	2	-1.100	-0.890	-1.000	–	-0.810	-0.930	-0.700	Vdc	–	11,12,13	–	–	–	9,10	–	–	8	–	–	–	1,16
		3	-1.100	-0.890	-1.000	–	-0.810	-0.930	-0.700	Vdc	–	11,12,13	–	–	–	9,10	–	–	8	–	–	–	1,16
	V_{OH2}	7	-2.8	–	-2.6	–	–	-2.4	–	Vdc	5	4	–	–	–	–	–	–	8	–	–	7	6
Logic "0" Output Voltage	V_{OL1} ①	2	-1.990	-1.675	-1.950	–	-1.650	-1.925	-1.615	Vdc	–	11,12,13	–	–	–	9,10	–	–	8	–	–	–	1,16
		3	-1.990	-1.675	-1.950	–	-1.650	-1.925	-1.615	Vdc	–	11,12,13	–	–	–	9,10	–	–	8	–	–	–	1,16
	V_{OL2}	7	–	-4.26	–	–	-4.40	–	-4.48	Vdc	4	5	–	–	–	–	–	–	8	–	7	–	6
Logic "1" Threshold Voltage	V_{OHA} ②	2	-1.120	–	-1.020	–	–	-0.950	–	Vdc	–	–	11,12,13	–	–	–	9,10	–	8	–	–	–	1,16
		3	-1.120	–	-1.020	–	–	-0.950	–	Vdc	–	–	11,12,13	–	–	–	9,10	–	8	–	–	–	1,16
Logic "0" Threshold Voltage	V_{OLA} ③	2	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	11,12,13	–	–	–	9,10	8	–	–	–	1,16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	–	–	–	11,12,13	–	–	–	9,10	8	–	–	–	1,16
Short Circuit Current	I_{OS}	7	-65	-20	-65	–	-20	-65	-20	mAdc	5	4	–	–	–	7	–	–	8	–	–	–	6

① Test outputs of the device must be tested by sequencing through the truth table. All input, power supplya nd ground voltages must be maintained between tests. The clock input is the waveform shown.
② In addition to meeting the output levels specified, the device must divide by 10 during this test. The clock input is the waveform shown.
③ In addition to meeting the output levels specified, the device must divide by 11 during this test. The clock input is the waveform shown.



ELECTRICAL CHARACTERISTICS

Supply Voltage +5.0 V

The MC12513 has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 100-ohm resistor to +3.0 Vdc.

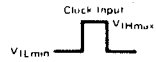
@ Test Temperature	TEST VOLTAGE/CURRENT VALUES											
	Volts									mA		
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}
-55°C	+4.120	+3.040	+3.745	+3.500	+2.4	+0.5	+2.0	+0.8	+5.0	-0.25	16	-0.40
+25°C	+4.220	+3.110	+3.895	+3.525	+2.4	+0.5	+2.0	+0.8	+5.0	-0.25	16	-0.40
+125°C	+4.370	+3.140	+4.000	+3.560	+2.4	+0.5	+2.0	+0.8	+5.0	-0.25	16	-0.40

Characteristic	Symbol	Pin Under Test	MC12513 -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}	(V_{EE}) Gnd
Power Supply Drain Current	I_{CC1}	8	--	--	-80	-62	--	--	--	mAdc									1,16				8
	I_{CC2}	6	--	--	--	--	5.2	--	--	mAdc	4	5	--						6				8
Input Current	I_{INH1}	15	--	--	--	--	250	--	--	µAdc	15	--	--						1,16				8
		11	--	--	--	--	↓	--	--	↓	11	--	--						↓				↓
		12	--	--	--	--		--	--		12	--	--										
		13	--	--	--	--		--	--		13	--	--										
	I_{INH2}	4	--	--	2.0	--	5.0	--	--	mAdc	4,5	--	--						6				8
		5	--	--	2.0	--	5.0	--	--	mAdc	4,5	--	--						6				8
	I_{INH3}	5	--	--	1.0	--	2.5	--	--	mAdc	4	5	--						6	--	--		8
	I_{INH4}	9	--	--	--	--	100	--	--	µAdc					9	--	--	--	1,16	--	--	--	8
		10	--	--	--	--	100	--	--	µAdc					10	--	--	--	1,16	--	--	--	8
Leakage Current	I_{INL1}	15	--	--	-10	--		--	--	µAdc	--	--							1,16	--			8,15
		11	--	--	↓	--	--	--	--	↓	--	--							↓	--			8,11
		12	--	--		--	--	--	--		--	--	--							--			8,12
		13	--	--		--	--	--	--		--	--	--	--						--	--	--	8,13
	I_{INL2}	9	-1.6	--	-1.6	--	--	-1.6	--	mAdc	--	--	--	--	--	9	--	--	1,16	--	--	--	8
		10	-1.6	--	-1.6	--	--	-1.6	--	mAdc	--	--	--	--	--	10	--	--	1,16	--	--	--	8
Reference Voltage	V_{BB}	14	--	--	3.67	--	3.87	--	--	Vdc	--	--	--	--	--	--	--	--	1,16	14	--	--	8
Logic "1" Output Voltage	V_{OH1} ①	2	3.880	4.120	4.030	--	4.220	4.135	4.370	Vdc	--	11,12,13	--	--	--	9,10	--	--	1,16	--	--	--	8
		3	3.880	4.120	4.030	--	4.220	4.135	4.370	Vdc	--	11,12,13	--	--	--	9,10	--	--	1,16	--	--	--	8
	V_{OH2}	7	2.4	--	2.7	--	--	3.0	--	Vdc	5	4	--	--	--	--	--	--	6	--	--	7	8
Logic "0" Output Voltage	V_{OL1} ①	2	3.040	3.405	3.110	--	3.440	3.140	3.515	Vdc	--	11,12,13	--	--	--	9,10	--	--	1,16	--	--	--	8
		3	3.040	3.405	3.110	--	3.440	3.140	3.515	Vdc	--	11,12,13	--	--	--	9,10	--	--	1,16	--	--	--	8
	V_{OL2}	7	--	1.00	--	--	0.80	--	0.66	Vdc	4	5	--	--	--	--	--	--	6	--	7	--	8
Logic "1" Threshold Voltage	V_{OHA} ②	2	3.860	--	4.010	--	--	4.115	--	Vdc	--		11,12,13	--	--	--	9,10	--	1,16	--	--	--	8
		3	3.860	--	4.010	--	--	4.115	--	Vdc	--	--	11,12,13	--	--	--	9,10	--	1,16	--	--	--	8
Logic "0" Threshold Voltage	V_{OLA} ③	2	--	3.425	--	--	3.460	--	3.535	Vdc	--	--	--	11,12,13	--	--	--	9,10	1,16	--	--	--	8
		3	--	3.425	--	--	3.460	--	3.535	Vdc	--	--	--	11,12,13	--	--	--	9,10	1,16	--	--	--	8
Short Circuit Current	I_{OS}	7	-65	-20	-65	--	-20	-65	-20	mAdc	5	4				7		--	6			--	8

① Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.

② In addition to meeting the output levels specified, the device must divide by 10 during this test. The clock input is the waveform shown.

③ In addition to meeting the output levels specified, the device must divide by 11 during this test. The clock input is the waveform shown.



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Ratings above which device life may be impaired:			
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8.0	Vdc
Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{ILmin}	Vdc
Output Source Current Continuous Surge	I_O	 <50 <100	mAdc
Storage Temperature Range	T_{stg}	-65 to +175	°C
Recommended maximum ratings above which performance may be degraded:			
Operating Temperature Range	T_A	-55 to +125	°C
DC Fan-Out* (Gates and Flip-Flops)	n	70	–

*AC fan-out is limited by desired system performance.

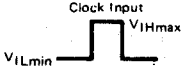
ELECTRICAL CHARACTERISTICS
Supply Voltage -5.2 V

The MC12513 has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 100-ohm resistor to -2.0 Vdc.

@Test Temperature	TEST VOLTAGE/CURRENT VALUES: Volts V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{EE}	mA I_L	I_{OL}	I_{OH}
-55°C	-0.880	-2.020	-1.255	-1.500	-2.8	-4.7	-3.2	-4.4	-5.2	-0.25	16	-0.40
+25°C	-0.780	-1.950	-1.105	-1.475	-2.8	-4.7	-3.2	-4.4	-5.2	-0.25	16	-0.40
+125°C	-0.630	-1.920	-1.000	-1.400	-2.8	-4.7	-3.2	-4.4	-5.2	-0.25	16	-0.40

Characteristic	Symbol	Pin Under Test	MC12513 -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OH}	Gnd
Power Supply Drain Current	I_{CC1}	8	–	–	-80	-62	–	–	–	mAdc	–	–	–	–	–	–	–	–	8	–	–	–	1,16
	I_{CC2}	6	–	–	–	–	5.2	–	–	mAdc	4	5	–	–	–	–	–	–	8	–	–	–	6
Input Current	I_{INH1}	15	–	–	–	–	250	–	–	μAdc	15	–	–	–	–	–	–	–	8	–	–	–	1,16
		11	–	–	–	–	↓	–	–	↓	11	–	–	–	–	–	–	–	↓	–	–	–	↓
		12	–	–	–	–		–	–		12	–	–	–	–	–	–	–		–	–	–	
		13	–	–	–	–		–	–		13	–	–	–	–	–	–	–		–	–	–	
	I_{INH2}	4	–	–	2.0	–	5.0	–	–	mAdc	5	4	–	–	–	–	–	–	8	–	–	–	6
		5	–	–	2.0	–	5.0	–	–	mAdc	5	4	–	–	–	–	–	–	8	–	–	–	6
	I_{INH3}	5	–	–	1.0	–	2.5	–	–	mAdc	4	5	–	–	–	–	–	–	8	–	–	–	6
	I_{INH4}	9	–	–	–	–	100	–	–	μAdc	–	–	–	–	9	–	–	–	8	–	–	–	1,16
		10	–	–	–	–	100	–	–	μAdc	–	–	–	–	10	–	–	–	8	–	–	–	1,16
Leakage Current	I_{INL1}	15	–	–	-10	–	–	–	–	μAdc	–	–	–	–	–	–	–	–	8,15	–	–	–	1,16
		11	–	–	↓	–	–	–	–	↓	–	–	–	–	–	–	–	–	8,11	–	–	–	↓
		12	–	–		–	–	–	–		–	–	–	–	–	–	–	–	8,12	–	–	–	
		13	–	–		–	–	–	–		–	–	–	–	–	–	–	–	8,13	–	–	–	
	I_{INL2}	9	-1.6	–	-1.6	–	–	-1.6	–	mAdc	–	–	–	–	–	9	–	–	8	–	–	–	1,16
		10	-1.6	–	-1.6	–	–	-1.6	–	mAdc	–	–	–	–	–	10	–	–	8	–	–	–	1,16
Reference Voltage	V_{BB}	14	–	–	-1.360	–	-1.160	–	–	Vdc	–	–	–	–	–	–	–	–	8	14	–	–	1,16
Logic "1" Output Voltage	V_{OH1} ①	2	-1.120	-0.880	-0.970	–	-0.780	-0.865	-0.630	Vdc	–	11,12,13	–	–	–	9,10	–	–	8	–	–	–	1,16
		3	-1.120	-0.880	-0.970	–	-0.780	-0.865	-0.630	Vdc	–	11,12,13	–	–	–	9,10	–	–	8	–	–	–	1,16
	V_{OH2}	7	-2.8	–	-2.5	–	–	-2.2	–	Vdc	5	4	–	–	–	–	–	–	8	–	–	7	6
Logic "0" Output Voltage	V_{OL1} ①	2	-2.020	-1.655	-1.950	–	-1.620	-1.920	-1.545	Vdc	–	11,12,13	–	–	–	9,10	–	–	8	–	–	–	1,16
		3	-2.020	-1.655	-1.950	–	-1.620	-1.920	-1.545	Vdc	–	11,12,13	–	–	–	9,10	–	–	8	–	–	–	1,16
	V_{OL2}	7	–	-4.20	–	–	-4.40	–	-4.54	Vdc	4	5	–	–	–	–	–	–	8	–	7	–	6
Logic "1" Threshold Voltage	V_{OHA} ②	2	-1.140	–	-0.990	–	–	-0.885	–	Vdc	–	–	11,12,13	–	–	–	9,10	–	8	–	–	–	1,16
		3	-1.140	–	-0.990	–	–	-0.885	–	Vdc	–	–	11,12,13	–	–	–	9,10	–	8	–	–	–	1,16
Logic "0" Threshold Voltage	V_{OLA} ③	2	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	–	11,12,13	–	–	–	9,10	8	–	–	–	1,16
		3	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	–	11,12,13	–	–	–	9,10	8	–	–	–	1,16
Short Circuit Current	I_{OS}	7	-65	-20	-65	–	-20	-65	-20	mAdc	5	4	–	–	–	7	–	–	8	–	–	–	6

① Test outputs of the device must be tested by sequencing through the truth table. All input, power supplya nd ground voltages must be maintained between tests. The clock input is the waveform shown.
② In addition to meeting the output levels specified, the device must divide by 10 during this test. The clock input is the waveform shown.
③ In addition to meeting the output levels specified, the device must divide by 11 during this test. The clock input is the waveform shown.



ELECTRICAL CHARACTERISTICS

Supply Voltage +5.0 V

The MC12013 has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50-ohm resistor to +3.0 Vdc.

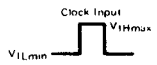
@ Test Temperature	TEST VOLTAGE/CURRENT VALUES											
	Volts									mA		
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}
-30°C	+4.110	+3.070	+3.795	+3.500	+2.4	+0.5	+2.0	+0.8	+5.0	-0.25	16	-0.40
+25°C	+4.190	+3.110	+3.895	+3.525	+2.4	+0.5	+2.0	+0.8	+5.0	-0.25	16	-0.40
+85°C	+4.300	+3.135	+3.965	+3.560	+2.4	+0.5	+2.0	+0.8	+5.0	-0.25	16	-0.40

Characteristic	Symbol	Pin Under Test	MC12013 -30°C Min	MC12013 -30°C Max	MC12013 +25°C Min	MC12013 +25°C Typ	MC12013 +25°C Max	MC12013 +85°C Min	MC12013 +85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}	(V_{EE}) Gnd
Power Supply Drain Current	I_{CC1}	8			-80	-62				mAdc									1,16				8
	I_{CC2}	6					5.2			mAdc	4	5							6				8
Input Current	I_{INH1}	15					250			µAdc	15								1,16				8
		11									11												
		12									12												
		13									13												
	I_{INH2}	4			2.0		5.0			mAdc	4.5								6				8
		5			2.0		5.0			mAdc	4.5								6				8
	I_{INH3}	5			1.0		2.5			mAdc	4	5							6				8
	I_{INH4}	9					100			µAdc					9				1,16				8
		10					100			µAdc					10				1,16				8
Leakage Current	I_{INL1}	15			-10					µAdc									1,16				8,15
		11																					8,11
		12																					8,12
		13																					8,13
	I_{INL2}	9	-1.6		-1.6			-1.6		mAdc						9			1,16				8
		10	-1.6		-1.6			-1.6		mAdc						10			1,16				8
Reference Voltage	V_{BB}	14			3.67		3.87			Vdc									1,16	14			8
Logic "1" Output Voltage	V_{OH1} ①	2	3.900	4.110	4.000		4.190	4.070	4.300	Vdc		11,12,13				9,10			1,16				8
		3	3.900	4.110	4.000		4.190	4.070	4.300	Vdc		11,12,13				9,10			1,16				8
	V_{OH2}	7	2.4		2.6			2.8		Vdc	5	4							6			7	8
Logic "0" Output Voltage	V_{OL1} ①	2	3.070	3.385	3.110		3.410	3.135	3.445	Vdc		11,12,13				9,10			1,16				8
		3	3.070	3.385	3.110		3.410	3.135	3.445	Vdc		11,12,13				9,10			1,16				8
	V_{OL2}	7		0.94			0.80		0.72	Vdc	4	5							6		7		8
Logic "1" Threshold Voltage	V_{OHA} ②	2	3.880		3.980			4.050		Vdc			11,12,13				9,10		1,16				8
		3	3.880		3.980			4.050		Vdc			11,12,13				9,10		1,16				8
Logic "0" Threshold Voltage	V_{OLA} ③	2		3.405			3.430		3.465	Vdc				11,12,13				9,10	1,16				8
		3		3.405			3.430		3.465	Vdc				11,12,13				9,10	1,16				8
Short Circuit Current	I_{OS}	7	-65	-20	-65		-20	-65	-20	mAdc	5	4				7			6				8

① Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.

② In addition to meeting the output levels specified, the device must divide by 10 during this test. The clock input is the waveform shown.

③ In addition to meeting the output levels specified, the device must divide by 11 during this test. The clock input is the waveform shown.



SWITCHING CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC12013 -30°C Min	-30°C Typ	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Typ	+85°C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Pulse Gen. 1	Pulse Gen. 2	Pulse Gen. 3	V_{IHmin} †	V_{ILmin} †	V_F -3.0 V	V_{EE} -3.0 V	V_{CC} +2.0
Propagation Delay (See Figures 3 and 5)	t_{15+2+}	2	–	–	–	–	5.3	8.1	–	–	–	ns	15	–	–	–	11,12,13	9,10	8	1,6,16
	t_{15+2-}	2	–	–	–	–	5.0	7.5	–	–	–		15	–	–	–	11,12,13	9,10	8	1,6,16
	t_{5+7+}	7	–	–	–	–	5.7	8.1	–	–	–		A	–	–	–	–	–	8	1,6,16
	t_{5-7-}	7	–	–	–	–	4.1	6.5	–	–	–		A	–	–	–	–	–	8	1,6,16
Setup Time (See Figures 4 and 5)	t_{setup1}	11	–	–	–	5.0	1.5	–	–	–	–	ns	15	*	–	–	*	9,10	8	1,6,16
	t_{setup2}	9	–	–	–	5.0	2.0	–	–	–	–	ns	15	–	*	–	11,12,13	*	8	1,6,16
Release Time (See Figures 4 and 5)	t_{rel1}	11	–	–	–	5.0	1.5	–	–	–	–	ns	15	*	–	–	*	9,10	8	1,6,16
	t_{rel2}	9	–	–	–	5.0	2.0	–	–	–	–	ns	15	–	*	–	11,12,13	*	8	1,6,16
Toggle Frequency (Figure 6 ÷ 11)	f_{max}	2	–	600	–	550	600	–	–	550	–	MHz	–	–	–	11	–	–	8	16

*Test inputs sequentially, with Pulse Generator 2 or 3 as indicated connected to input under test, and the voltage indicated applied to the other input(s) of the same type (i.e., MECL or MTTL).

†	-30°C	+25°C	+85°C	
V_{IHmin}	+1.03	+1.115	+1.20	Vdc
†V_{ILmin}	+0.175	+0.200	+0.235	Vdc

SWITCHING CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC12513 -55°C Min	-55°C Typ	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Typ	+125°C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Pulse Gen. 1	Pulse Gen. 2	Pulse Gen. 3	V_{IHmin} †	V_{ILmin} †	V_F -3.0 V	V_{EE} -3.0 V	V_{CC} +2.0
Propagation Delay (See Figures 3 and 5)	t_{15+2+}	2	–	–	–	–	5.3	8.1	–	–	–	ns	15	–	–	–	11,12,13	9,10	8	1,6,16
	t_{15+2-}	2	–	–	–	–	5.0	7.5	–	–	–		15	–	–	–	11,12,13	9,10	8	1,6,16
	t_{5+7+}	7	–	–	–	–	5.7	8.1	–	–	–		A	–	–	–	–	–	8	1,6,16
	t_{5-7-}	7	–	–	–	–	4.1	6.5	–	–	–		A	–	–	–	–	–	8	1,6,16
Setup Time (See Figures 4 and 5)	t_{setup1}	11	–	–	–	5.0	1.5	–	–	–	–	ns	15	*	–	–	*	9,10	8	1,6,16
	t_{setup2}	9	–	–	–	5.0	2.0	–	–	–	–	ns	15	–	*	–	11,12,13	*	8	1,6,16
Release Time (See Figures 4 and 5)	t_{rel1}	11	–	–	–	5.0	1.5	–	–	–	–	ns	15	*	–	–	*	9,10	8	1,6,16
	t_{rel2}	9	–	–	–	5.0	2.0	–	–	–	–	ns	15	–	*	–	11,12,13	*	8	1,6,16
Toggle Frequency (Figure 6 ÷ 11)	f_{max}	2	–	600	–	550	600	–	–	550	–	MHz	–	–	–	11	–	–	8	16

*Test inputs sequentially, with Pulse Generator 2 or 3 as indicated connected to input under test, and the voltage indicated applied to the other input(s) of the same type (i.e., MECL or MTTL).

†	-55°C	+25°C	+125°C	
V_{IHmin}	+1.02	+1.15	+1.27	Vdc
†V_{ILmin}	+0.165	+0.215	+0.260	Vdc

FIGURE 3 – AC VOLTAGE WAVEFORMS

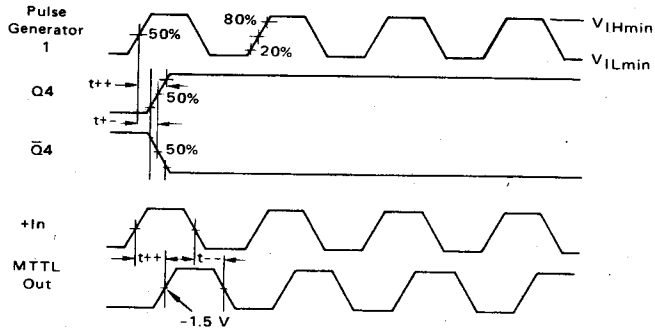


FIGURE 4 – SETUP AND RELEASE TIME WAVEFORMS

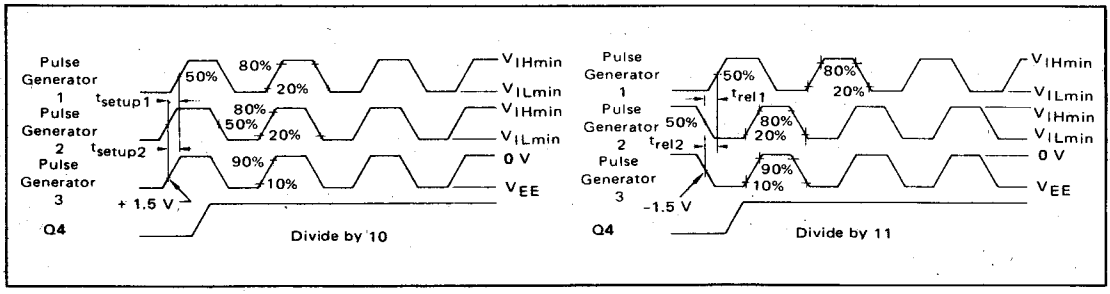


FIGURE 5 – AC TEST CIRCUIT

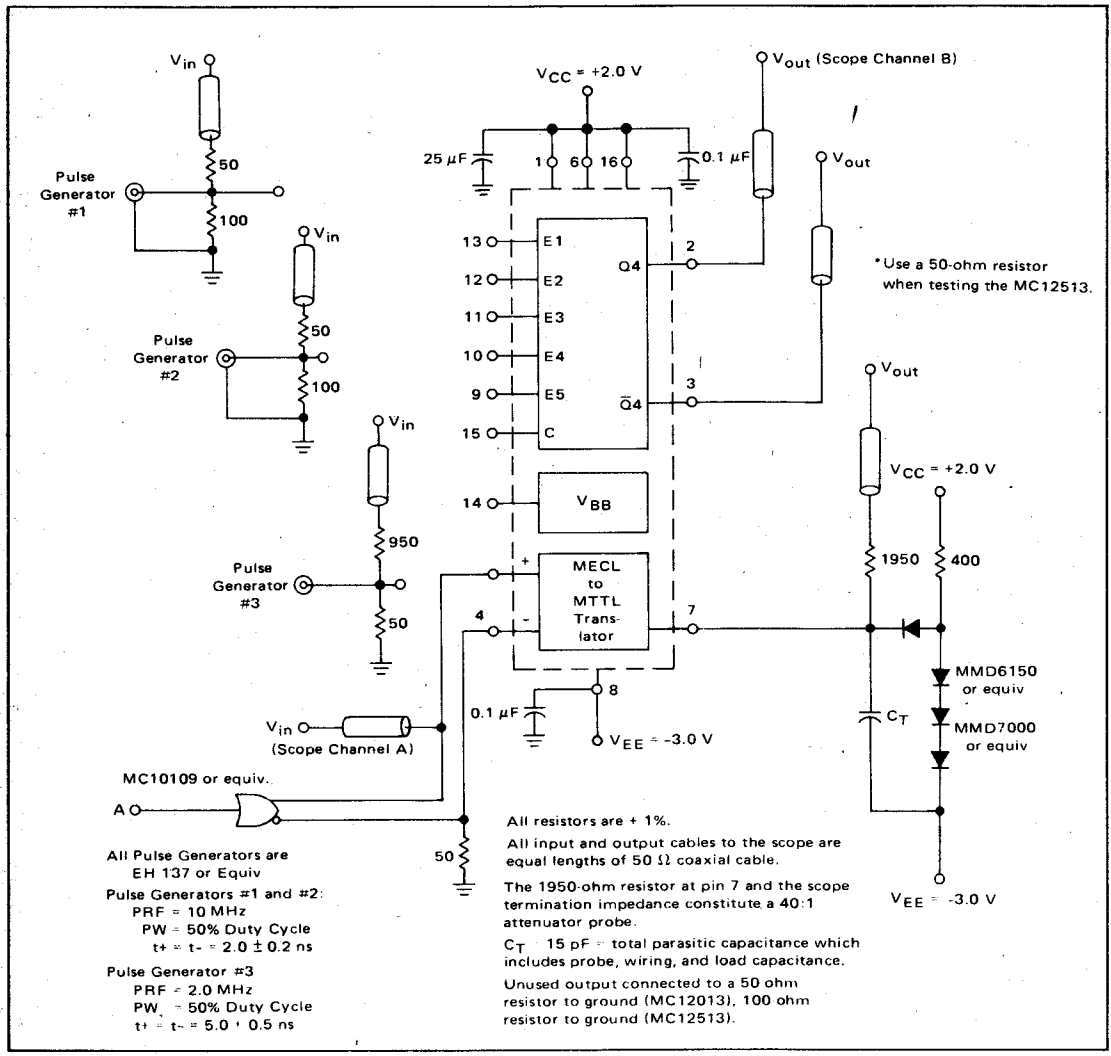


FIGURE 6 – MAXIMUM FREQUENCY TEST CIRCUIT (÷ 11)

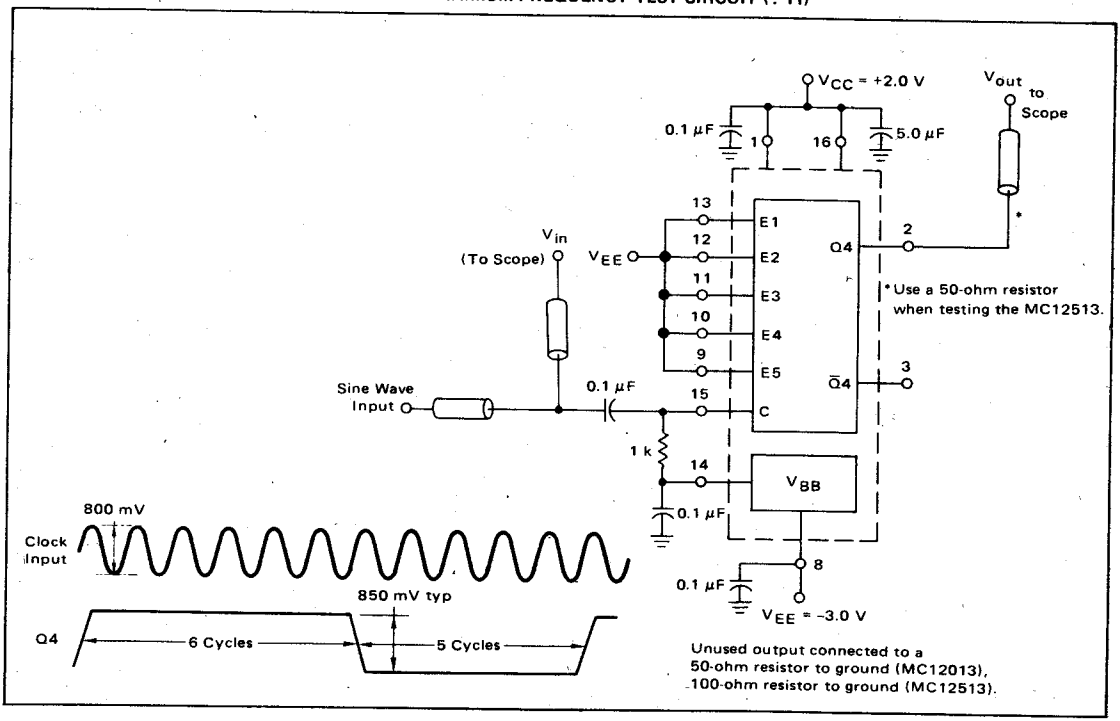
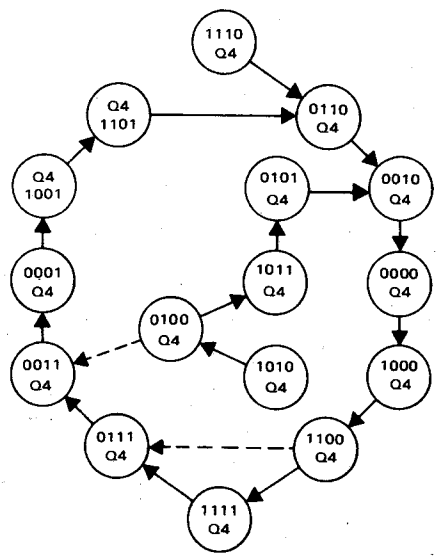


FIGURE 7 – STATE DIAGRAM

Q1	Q2	Q3	Q4
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
1	0	0	1
1	1	0	1
0	1	1	0
0	0	1	0
0	0	0	0
1	0	0	0
1	1	0	0

Enable = 0

Enable = 1



NOTES:

– – – Enable = 1.

The State of the Enable is important only for the positive Clock Transition when the counter is in state 1100.

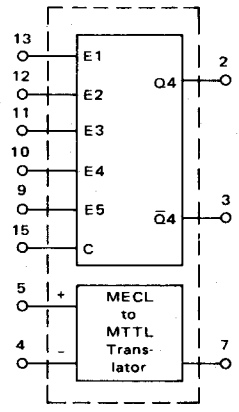
APPLICATIONS INFORMATION

The primary application of the MC12013/MC12513 is as a high speed variable modulus prescaler in the divide by N section of a phase locked loop synthesizer used as the local oscillator of two way radios. The theory and advantages of variable modulus prescaling, along with typical applications, are covered in detail on the data sheet for the MC12012.

Proper VHF termination techniques should be followed when the clock is separated from the prescaler by any appreciable distance.

In its basic form, the MC12013/MC12513 will divide by 10 or 11. Division by 10 occurs when anyone or all of the five gate inputs E1 through E5 are high. Division by 11 occurs when all inputs E1 through E5 are low. (Unconnected MTTL inputs are normally high, unconnected MECL inputs are normally low.) With the addition of extra parts, many different division configurations may be obtained (20/21, 40/41, 50/51, 100/101, etc.). A few of the many configurations are shown below.

FIGURE 8 – ÷10/11

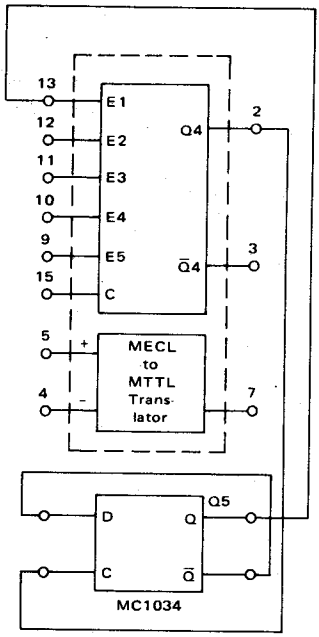


Q1	Q2	Q3	Q4
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
1	0	0	1
1	1	0	1
0	1	1	0
0	0	1	0
0	0	0	0
1	0	0	0
1	1	0	0

Enable = 0

Enable = 1

FIGURE 9 – ÷ 20/21



COUNT	Q1	Q2	Q3	Q4	Q4
31	1	1	1	1	1
30	0	1	1	1	1
28	0	0	1	1	1
24	0	0	0	1	1
25	1	0	0	1	1
27	1	1	0	1	1
22	0	1	1	0	1
20	0	0	1	0	1
16	0	0	0	0	1
17	1	0	0	0	1
19	1	1	0	0	1
14	0	1	1	1	0
12	0	0	1	1	0
8	0	0	0	1	0
9	1	0	0	1	0
11	1	1	0	1	0
6	0	1	1	0	0
4	0	0	1	0	0
0	0	0	0	0	0
1	1	0	0	0	0
3	1	1	0	0	0

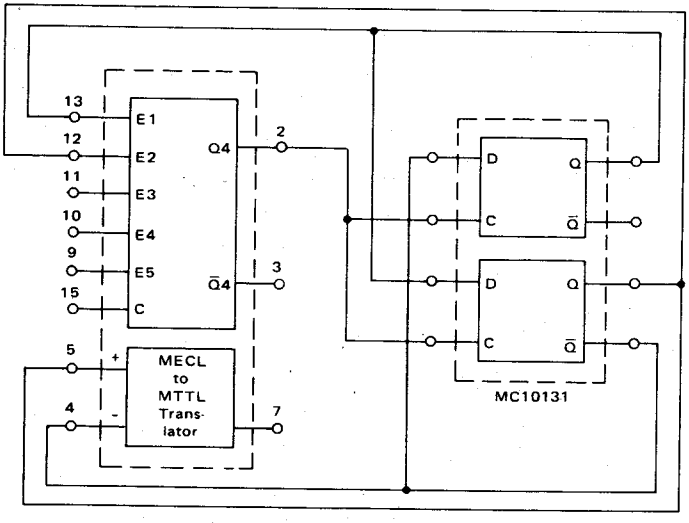
E2 + E3 + E4 + E5 = 0

E2 + E3 + E4 + E5 = 1

To obtain an MTTL output, connect pins 5 and 4 to pins 2 and 3 respectively. Termination resistors for the MECL outputs are not shown, but are required except for the flip-flop driving the translator section.

The ÷ 20/21 counter may also be built using an MTTL flip-flop by connecting pins 5 and 4 to pins 2 and 3 respectively, and driving the MTTL flip-flop with pin 7. MC12013 inputs E4 and E5 are used rather than E1 With E1 + E2 + E3 = 0, operation remains as shown.

FIGURE 10 – ÷ 40/41



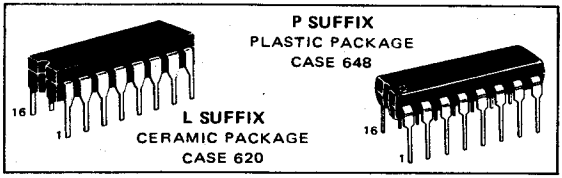
For ÷ 40: E4 + E5 = 1
For ÷ 41: E4 + E5 = 0

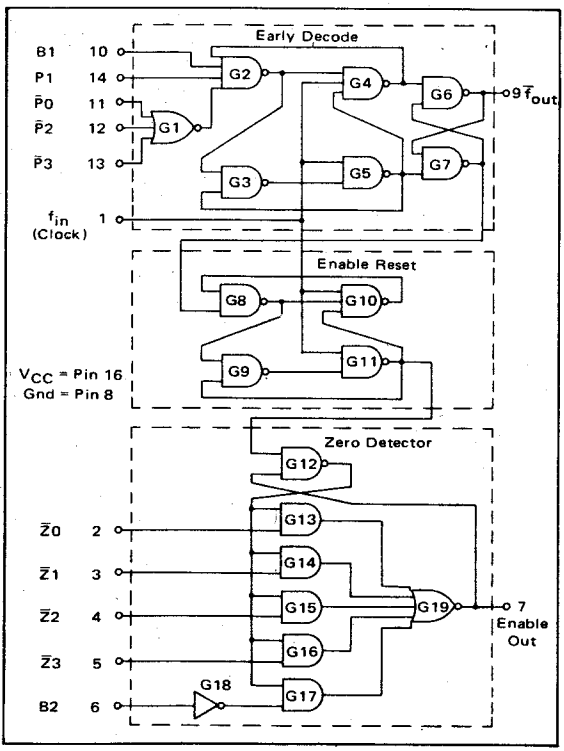
Termination resistors for MECL outputs are not shown, but are required except for the flip-flop driving the translator section.

COUNTER CONTROL LOGIC

MC12014
MC12514

The MC12014/MC12514 monolithic counter control logic unit is designed for use with the MC12012 Two-Modulus Prescaler and the MC4016 Programmable Counter to accomplish direct high-frequency programming. The MC12014/MC12514 consists of a zero detector which controls the modulus of the MC12012, and an early decode function which controls the MC4016. The early decode feature also increases the useful frequency range of the MC4016 from 8.0 MHz to 25 MHz.

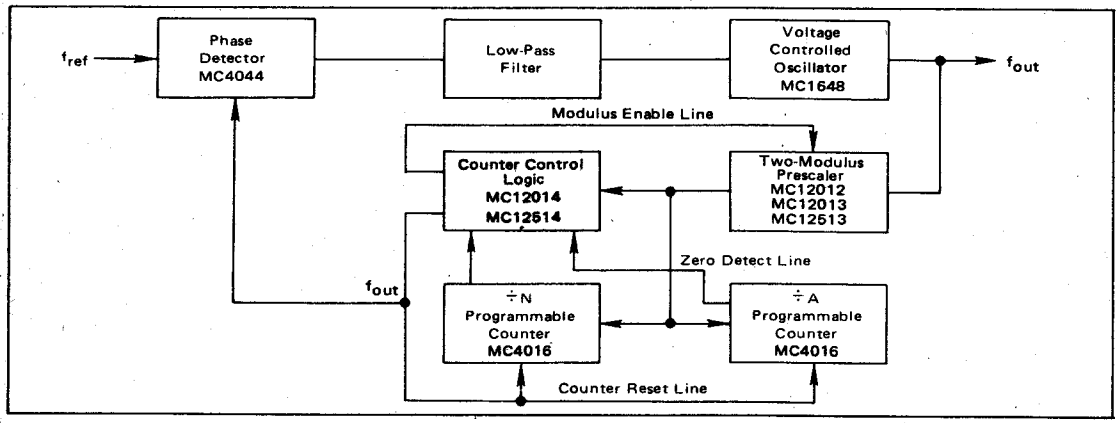




MAXIMUM RATINGS

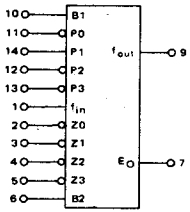
Rating	Symbol	Unit
Supply Operating Voltage Range	4.75 to 5.25	Vdc
Supply Voltage	+7.0	Vdc
Input Voltage	+5.5	Vdc
Output Voltage	+5.5	Vdc
Operating Temperature Range	0 to +75	°C
Storage Temperature Range	-65 to +150	°C
Maximum Junction Temperature	+150	°C
Thermal Resistance - Junction to Case (θ_{JC})	0.05	°C/mW
Thermal Resistance - Junction to Ambient (θ_{JA})	0.15	°C/mW

FIGURE 1 – TYPICAL FREQUENCY SYNTHESIZER APPLICATION



ELECTRICAL CHARACTERISTICS

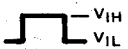
Test procedures are shown for the f_{in}, $\overline{Z0}$, B1 and P1 inputs. All other inputs are tested in the same manner as the $\overline{Z0}$ input.



	TEST CURRENT/VOLTAGE VALUES (All Temperatures)									
	mA			Volts						
	I_{OL}	I_{OH}	I_{IC}	V_{IL}	V_{IH}	V_{IHH}	V_{RH}	V_{CC}	V_{CCL}	V_{CCH}
MC12514	16	-0.4	-10	0.5	2.4	5.5	4.5	5.0	4.5	5.5
MC12014	16	-0.4	-10	0.5	2.4	5.5	4.5	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC12514 Test Limits -55 to +125°C			MC12014 Test Limits 0 to +75°C			TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW									Gnd
			Min	Max	Unit	Min	Max	Unit	I_{OL}	I_{OH}	I_{IC}	V_{IL}	V_{IH}	V_{IHH}	V_{RH}	V_{CC}	V_{CCL}	V_{CCH}	
Input																		
Forward Current	I_{IL}	1	-6.4	–	mAdc	-6.4	–	mAdc	–	–	–	1	–	–	–	–	–	16	8,10
		2	-1.6	–	↓	-1.6	–	↓	–	–	–	2	–	–	–	–	–	↓	8
		10	-1.6	–	↓	-1.6	–	↓	–	–	–	10	–	–	–	–	–	↓	1,8,11,12,13
		14	-1.6	–	↓	-1.6	–	↓	–	–	–	14	–	–	–	–	–	↓	1,8,11,12,13
Leakage Current	I_{IH}	1	–	160	µAdc	–	160	µAdc	–	–	–	–	1	–	–	–	–	16	8,10
		2	–	40	↓	–	40	↓	–	–	–	–	2	–	–	–	–	↓	8
		10	–	↓	↓	–	↓	↓	–	–	–	–	10	–	–	–	–	↓	1,8,11,12,13
		14	–	↓	↓	–	↓	↓	–	–	–	–	14	–	–	–	–	↓	1,8,11,12,13
	I_{IHH}	1	–	1.0	mAdc	–	1.0	mAdc	–	–	–	–	–	1	–	–	–	16	8
		2	–	↓	↓	–	↓	↓	–	–	–	–	–	2	–	–	–	↓	8
		10	–	↓	↓	–	↓	↓	–	–	–	–	–	10	–	–	–	↓	1,8,11,12,13
		14	–	↓	↓	–	↓	↓	–	–	–	–	–	14	–	–	–	↓	1,8,11,12,13
Clamp Voltage	V_{IC}	1	–	-1.2	Vdc	–	-1.2	Vdc	–	–	1	–	–	–	–	–	16	–	8
		2	–	↓	↓	–	↓	↓	–	–	2	–	–	–	–	–	↓	–	↓
		10	–	↓	↓	–	↓	↓	–	–	10	–	–	–	–	–	↓	–	
		14	–	↓	↓	–	↓	↓	–	–	14	–	–	–	–	–	↓	–	
Output																		
Output Voltage	V_{OL}*	7	–	0.5	Vdc	–	0.5	Vdc	7	–	–	11,12,13	–	–	2,3,4,5,10	–	16	–	8
		9	–	0.5	Vdc	–	0.5	Vdc	9	–	–	11,12,13	–	–	10,14	–	16	–	8
	V_{OH}	7	2.4	–	Vdc	2.4	–	Vdc	–	7	–	2,3,4,5	–	–	6	–	16	–	8
		9**	2.4	–	Vdc	2.4	–	Vdc	–	9	–	–	–	–	11,12,13	–	16	–	8
Short-Circuit Current	I_{OS}	7	-65	-20	Vdc	-65	-20	Vdc	–	–	–	2,3,4,5	–	–	6	16	–	–	7,8
		9**	-65	-20	Vdc	-65	-20	Vdc	–	–	–	–	–	–	11,12,13	16	–	–	8,9
Power Requirements																		
Power Supply Drain	I_{CC}	16†	–	35	mAdc	–	35	mAdc	–	–	–	–	–	–	–	16	–	–	6,8,10

*Output level to be measured after waveform 1 is applied to f_{in}, pin 1.
**Output level to be measured after waveform 2 is applied to f_{in}, pin 1.
†Current to be measured after waveform 1 is applied to f_{in}, pin 1.

Waveform 1: 

Waveform 2: 

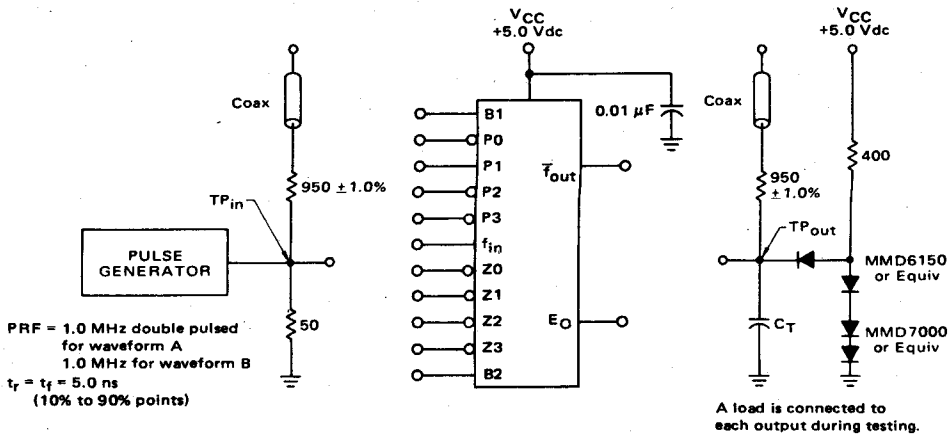
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, waveform letters refer to waveforms on next page.)

Characteristic	Symbol	Pin Under Test		MC12514 Test Limits (ns)							Pulse Gen. 1		Pulse Gen. 2		Pulse Out		Voltage Applied to Pins Listed Below	
				−55°C		+25°C			+125°C									
		In	Out	Min	Max	Min	Typ	Max	Min	Max	Wave-form	Pin	Wave-form	Pin	Wave-form	Pin	V_{IL} = 0.5 V	V_{IH} = 2.4 V
Propagation Delay	t_{PLH1}	1	9	–	16	–	10	15	–	19	A	1	J	10	K	9	11,12,13	14
	t_{PHL1}	1	9	–	17	–	11	16	–	18	A	1	J	10	K	9	11,12,13	14
	t_{PLH2}	2	7	–	12	–	8.5	12	–	17	A	1	H	2	L	7	3,4,5,11,12,13	6,10,14
		3	↓	–	↓	–	↓	↓	–	↓	↓	↓	↓	3	↓	↓	2,4,5,11,12,13	↓
		4		–		–			–					4			2,3,5,11,12,13	
		5		–		–			–					5			2,3,4,11,12,13	
	t_{PHL2}	1	7	–	17	–	11	16	–	19	A	1	H	2	L	7	3,4,5,11,12,13	6,10,14
	t_{PLH3}	6	7	–	17	–	11	16	–	20	A	1	J	6	L	7	2,3,4,5,11,12,13	10,14
Setup Time	t_{setup}"1"	10	–	–	–	–	1.0	2.0	–	–	A	1	B	10	G	9	11,12,13	14
		11	–	–	–	–	7.0	12	–	–	↓	↓	↓	11	F	↓	12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12			11,13	↓
		13	→	–	–	–			–	–				13			11,12	
		14	–	–	–	–	1.0	2.0	–	–				14	G		11,12,13	10
	t_{setup}"0"	10	–	–	–	–	4.5	8.0	–	–	A	1	C	10	F	9	11,12,13	14
		11	–	–	–	–	5.0	9.0	–	–	↓	↓	↓	11	G	↓	12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12			11,13	↓
		13	–	–	–	–			–	–				13			11,12	
		14	–	–	–	–	4.5	8.0	–	–				14	F		11,12,13	10
Hold Time	t_{hold}"1"	10	–	–	–	–	4.0	8.0	–	–	A	1	D	10	G	9	11,12,13	14
		11	–	–	–	–	5.0	10	–	–	↓	↓	↓	11	F	↓	12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12			11,13	↓
		13	–	–	–	–			–	–				13			11,12	
		14	–	–	–	–	4.0	8.0	–	–				14	G		11,12,13	10
	t_{hold}"0"	10	–	–	–	–	1.0	2.0	–	–	A	1	E	10	F	9	11,12,13	14
		11	–	–	–	–	7.5	14	–	–	↓	↓	↓	11	G	↓	12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12			11,13	↓
		13	–	–	–	–			–	–				13			11,12	
		14	–	–	–	–	1.0	2.0	–	–				14	F		11,12,13	10

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, waveform letters refer to waveforms on next page.)

Characteristic	Symbol	Pin Under Test		MC12014 Test Limits (ns)							Pulse Gen. 1		Pulse Gen. 2		Pulse Out		Voltage Applied to Pins Listed Below	
				0°C		+25°C			+75°C									
		In	Out	Min	Max	Min	Typ	Max	Min	Max	Wave-form	Pin	Wave-form	Pin	Wave-form	Pin	V_{IL} = 0.5 V	V_{IH} = 2.4 V
Propagation Delay	t_{PLH1}	1	9	–	15	–	10	15	–	17	A	1	J	10	K	9	11,12,13	14
	t_{PHL1}	1	9	–	16	–	11	16	–	18	A	1	J	10	K	9	11,12,13	14
	t_{PLH2}	2	7	–	12	–	8.5	12	–	14	A	1	H	2	L	7	3,4,5,11,12,13	6,10,14
		3	↓	–	↓	–	↓	↓	–	↓	↓	↓	↓	3	↓	↓	2,4,5,11,12,13	↓
		4		–		–			–					4			2,3,5,11,12,13	
		5		–		–			–					5			2,3,4,11,12,13	
	t_{PHL2}	1	7	–	16	–	11	16	–	18	A	1	H	2	L	7	3,4,5,11,12,13	6,10,14
	t_{PLH3}	6	7	–	16	–	11	16	–	18	A	1	J	6	L	7	2,3,4,5,11,12,13	10,14
Setup Time	t_{setup}"1"	10	–	–	–	–	1.0	2.0	–	–	A	1	B	10	G	9	11,12,13	14
		11	–	–	–	–	7.0	12	–	–	↓	↓	↓	11	F	↓	12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12			11,13	↓
		13	–	–	–	–			–	–				13			11,12	
		14	–	–	–	–	1.0	2.0	–	–				14	G		11,12,13	10
	t_{setup}"0"	10	–	–	–	–	4.5	8.0	–	–	A	1	C	10	F	9	11,12,13	14
		11	–	–	–	–	5.0	9.0	–	–	↓	↓	↓	11	G	↓	12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12			11,13	↓
		13	–	–	–	–			–	–				13			11,12	
		14	–	–	–	–	4.5	8.0	–	–				14	F		11,12,13	10
Hold Time	t_{hold}"1"	10	–	–	–	–	4.0	8.0	–	–	A	1	D	10	G	9	11,12,13	14
		11	–	–	–	–	5.0	10	–	–	↓	↓	↓	11	F	↓	12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12			11,13	↓
		13	–	–	–	–			–	–				13			11,12	
		14	–	–	–	–	4.0	8.0	–	–				14	G		11,12,13	10
	t_{hold}"0"	10	–	–	–	–	1.0	2.0	–	–	A	1	E	10	F	9	11,12,13	14
		11	–	–	–	–	7.5	14	–	–	↓	↓	↓	11	G	↓	12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12			11,13	↓
		13	–	–	–	–			–	–				13			11,12	
		14	–	–	–	–	1.0	2.0	–	–				14	F		11,12,13	10

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

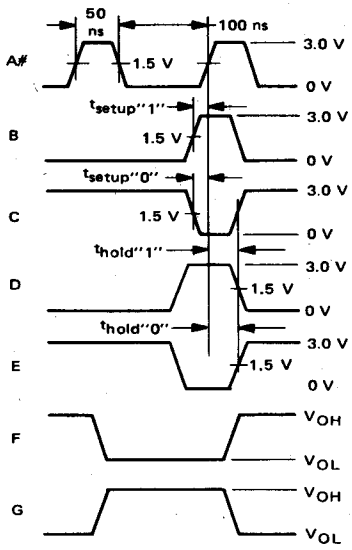


Two pulse generators are required and must be slaved together to provide the waveforms shown.

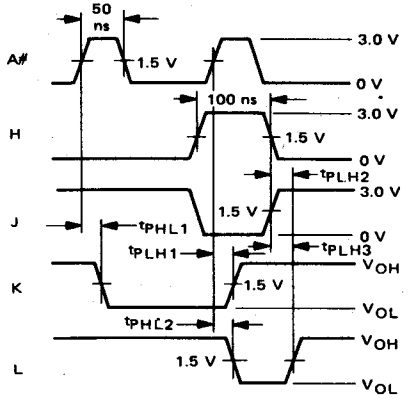
C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

SETUP AND HOLD TIMES



PROPAGATION DELAY TIMES

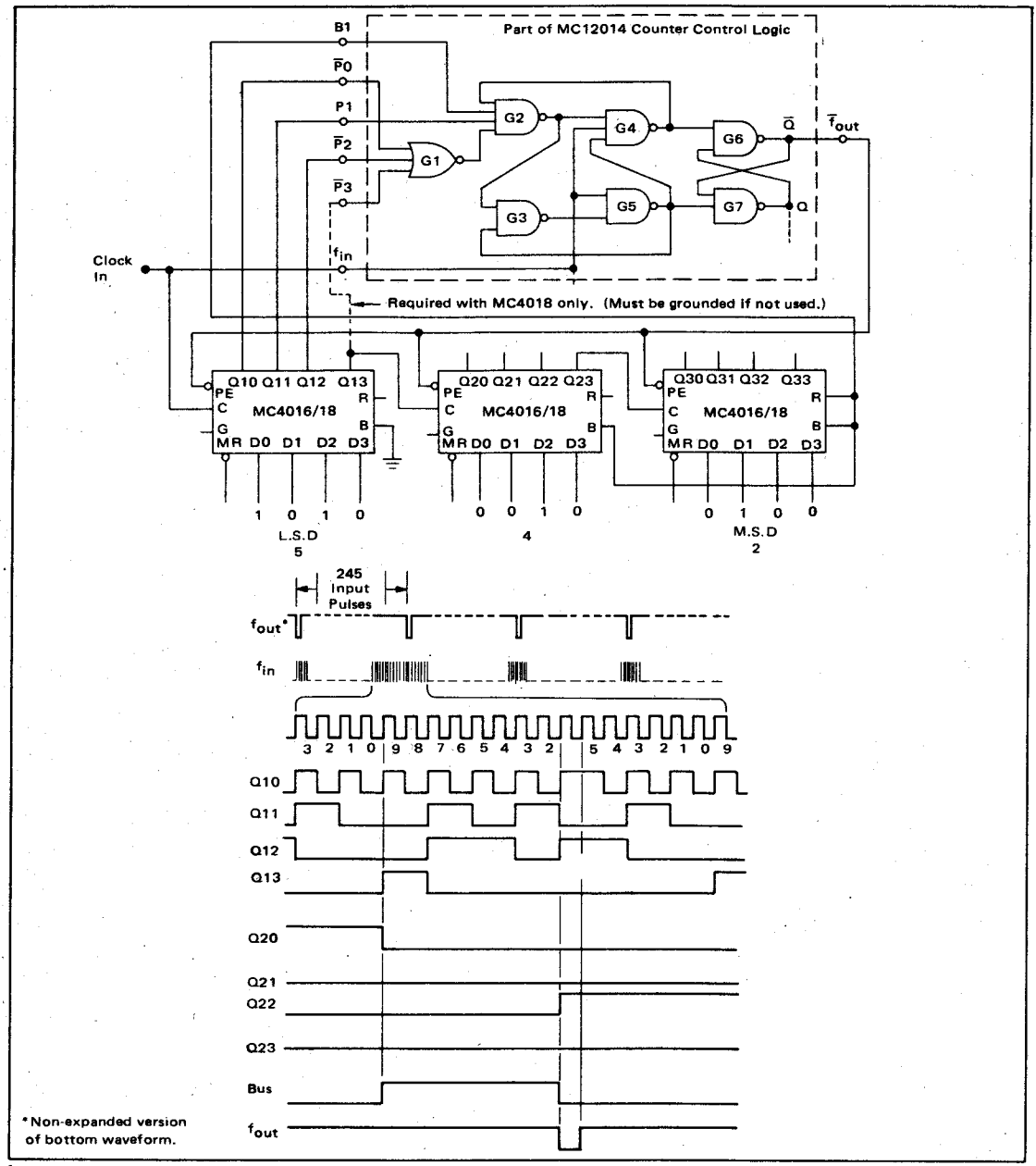


#Pulse A (f_{in}) used with all tests.

APPLICATIONS INFORMATION

The MC12014/MC12514 Counter Control Logic incorporates two features for enhancing operation of the MC4016/MC4018 Programmable Counters.[1] Maximum operating frequency of the counters is limited by the time required for re-programming at the end of each count-down cycle. Operation can be extended to approximately 25 MHz by using the "early decode" feature included in the MC12014. The appropriate connections are shown in

FIGURE 2 – INCREASING THE OPERATING RANGE OF MC4016/MC4018 PROGRAMMABLE COUNTERS USING MC12014/MC12514



[1] See the MC4016/4018 data sheet for additional information.

Figure 2. Only three counter stages are shown; however, up to eight stages can be satisfactorily cascaded. Note the following differences between this and the non-extended method: the counter gate inputs are not connected to the input clock; all parallel enables are connected to the $\overline{Q}$ output (f_{out}) of a type-D flip-flop formed by gates G2 through G7 in the MC12014 package; the bus terminal of the least significant stage is grounded; all other bus terminals and one internal resistor, R, are connected together and serve as a data input, B1, to the flip-flop. Four additional data inputs, $\overline{P0}$ through $\overline{P3}$, serve to decode the "two" state of the least significant counter stage. Circuit operation is illustrated in waveforms of Figure 2, where the timing for the end of a count-down cycle is shown in expanded form. The counter parallel inputs are assumed to have N = 245 programmed. Timing is not shown for the third stage since it has already been counted down to the all zero state. As the next-to-least significant stage reaches zero, the common bus line goes high. Count down of the least significant stage continues until the "two" state is reached, causing the remaining data inputs to the flip-flop to go high. The next-to-last clock pulse of the cycle then triggers the flip-flop $\overline{Q}$ output low. This takes the parallel enables of all three counter stages low, resetting the programmed data to the outputs. The next input pulse clocks $\overline{Q}$ back to the high state since the data inputs to the flip-flop are no longer all high. The resulting negative output pulse at f_{out} is one input clock period in duration. Note that division by N equal to 001 or 002 is not available using this method.

The frequency synthesizer shown in Figure 8 requires that the programmable counters be quickly stopped after reaching their terminal (zero) count. This can be simply accomplished by taking the master reset of all stages low at the appropriate time. The bus output of the counters could be used for this function since a transition there signals the end of a count-down sequence. However, due to the relatively long delay between the last positive clock transition and the bus transition a faster method is required in this application.

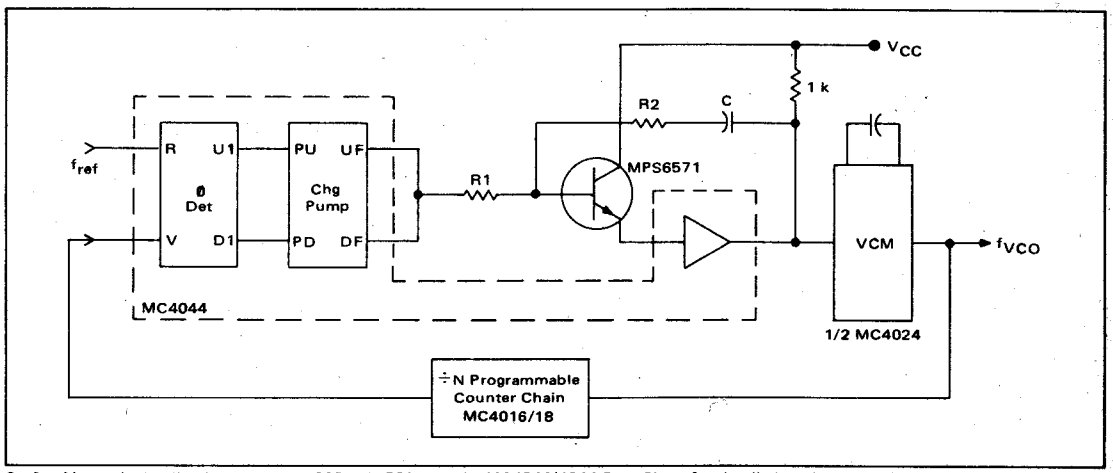
The "zero detection" feature of the MC12014 provides a convenient means of implementing a faster method. Gates G12 through G19 form a latch whose output goes high if B2 is high and low logic levels are applied to the Z0 thru Z3 inputs. When once set to a one by appropriate input conditions, the output of G19 remains high until it is reset by the circuit comprised of gates G8 through G11. Note that since the required information is stored, the counter can be allowed to continue cycling.

The G8-G11 circuit monitors the G7 output of the "early decode" type D flip-flop. When the counter stage connected to the $\overline{P0}$ thru $\overline{P3}$ inputs has counted down to its two state the output of G7 goes high; this enables the G8-G11 circuitry and the next positive clock transition causes the output of G11 to go high, resetting the output of G19 to zero.

Operation of the Counter Control Logic can be further clarified by considering a typical system application for programmable counters illustrated in the frequency synthesizer shown in Figure 3. There the counter provides a means of digitally selecting some integral multiple of a stable reference frequency. The circuit phase locks the output, f_{VCO}, of a voltage controlled oscillator to a reference frequency, f_{ref}.[2] Circuit operation is such that $f_{VCO} = Nf_{ref}$, where N is the divider ratio of the feedback counter, permitting frequency selection by means of thumbwheel switches.

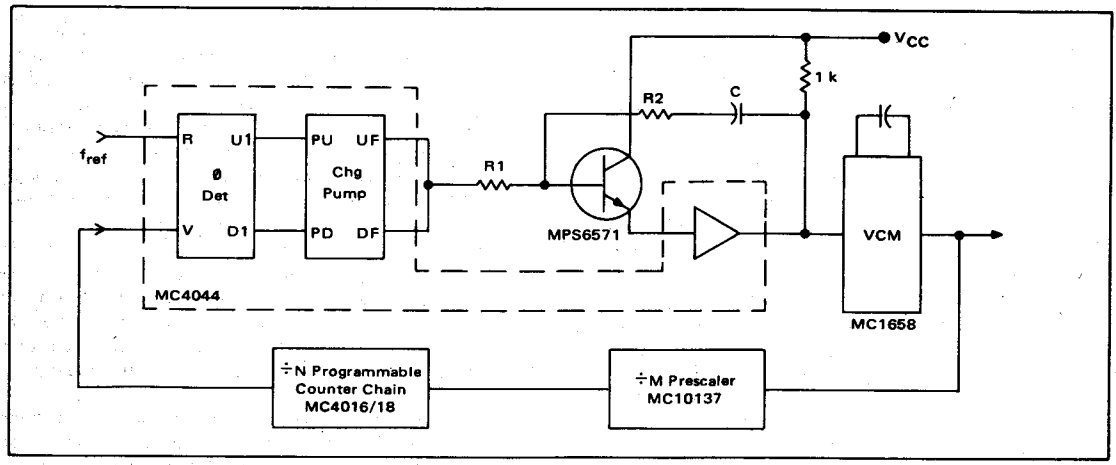
In many synthesizer applications the VCO is operated at VHF frequencies too high for direct division by TTL counters. In these cases the VCO output is usually prescaled by using a suitable fixed divide-by-M ECL circuit as shown in Figure 4. For this configuration, $f_{VCO} = NMf_{ref}$, where N is variable (programmable) and M is fixed. Design of the optimum loop filter requires that the input reference frequency be as high as possible where the upper limit is established by the required channel

FIGURE 3 – MTTL PHASE-LOCKED LOOP



2 See Motorola Application Notes AN-535, AN-532, and the MC4344/4044 Data Sheet for detailed explanation of over-all circuit operation.

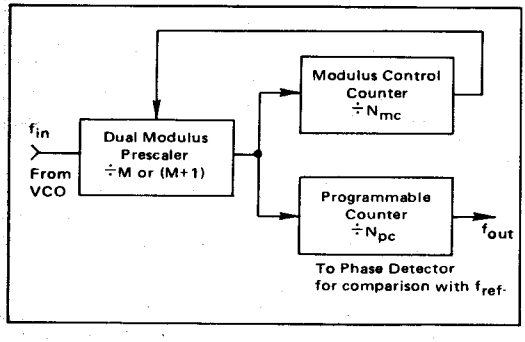
FIGURE 4 – MTTL-MECL PHASE-LOCKED LOOP



spacing. Since $f_{VCO} = Nf_{ref}$ in the non-prescaled case, if N is changed by one, the VCO output changes by f_{ref}, or the synthesizer channel spacing is just equal to f_{ref}. When the prescaler is used as in Figure 4, $f_{VCO} = NMf_{ref}$, and a change of one in N results in the VCO changing by Mf_{ref}, i.e., if f_{ref} is set equal to the minimum permissible channel spacing as is desirable, then only every M channels in a given band can be selected. One solution is to set f_{ref} = channel spacing/M but this leads to more stringent loop filter requirements.

An alternate approach that avoids this problem is provided by the counter configuration shown in Figure 5. It too uses a prescaler ahead of a programmable counter, however the modulus of the prescaler is now controlled by a third counter, causing it to alternate between M and M + 1. Operation is best explained by assuming that all three counters have been set for the beginning of a cycle: the prescaler for division by (M + 1), the modulus control counter for division by N_{mc}, and the programmable counter for division by N_{pc}. The prescaler will divide by (M +1) until the modulus control counter has counted down to zero; at this time, the all zero state is detected and causes the prescaler to divide by M until the programmable counter has also counted down to zero. When this occurs, a cycle is complete and each counter is reset to its original modulus in readiness for the next cycle.

FIGURE 5 – FEEDBACK COUNTERS WITH DUAL MODULUS PRESCALER



To determine the relationship between f_{out} and f_{in}, let T_1 be the time required for the modulus control counter to reach its terminal count and let T_2 be the remainder of one cycle. That is, T_2 is the time between terminal count in the modulus control counter and terminal count in the programmable counter. When the modulus control counter reaches zero, N_{mc} pulses will have entered it at a rate given by $f_{in}/(M + 1)$ pulses/second or T_1 is:

$$T_1 = \frac{(M + 1)}{f_{in}} \bullet N_{mc} \qquad (1)$$

At this time, N_{mc} pulses have also entered the programmable counter and it will reach its terminal counter after $(N_{pc} - N_{mc})$ more pulses have entered. The rate of entry is now f_{in}/M pulses/second since the prescaler is now dividing by M. From this T_2 is given by:

$$T_2 = \frac{M}{f_{in}} \bullet (N_{pc} - N_{mc}) \qquad (2)$$

Since $f = \frac{1}{T}$:

$$f_{out} = \frac{1}{T_{total}} = \frac{1}{T_1 + T_2} = \frac{1}{\frac{(M + 1)N_{mc}}{f_{in}} + \frac{M(N_{pc} - N_{mc})}{f_{in}}} \qquad (3)$$

$$f_{out} = \frac{f_{in}}{(M+1)N_{mc} + M(N_{pc}-N_{mc})}$$

$$= \frac{f_{in}}{MN_{mc}+N_{mc}+MN_{pc}-MN_{mc}}$$

$$= \frac{f_{in}}{MN_{pc}+N_{mc}}$$

In terms of the synthesizer application, $f_{VCO} = (MN_{pc} + N_{mc})\, f_{ref}$ and channels can be selected every f_{ref} by letting N_{pc} and N_{mc} take on suitable integer values, including zero.

A simplified example of this technique is shown in Figure 6. The MC12012 Dual Modulus Prescaler divides by either 10 or 11 when connected as shown in Figure 6. If the E3 and E4 Enable inputs are high at the start of a prescaler cycle, division by 10 results; if the Enable inputs are low at the beginning of the cycle, division by 11 results. The zero detection circuitry of the MC12014 Counter Control Logic is connected to monitor the outputs of the modulus control counter; this provides a suitable enable signal at E0 as the modulus control counter reaches its terminal (zero) count. The remainder of the MC12014 is connected to extend the operating frequency of the programmable counter chain. Appropriate waveforms for division by 43 are shown in Figure 7a.

The beginning of the timing diagram indicates circuit status just prior to the end of a countdown cycle, i.e., the modulus control counter has been counted down to one and the programmable counter is in the two state. The next positive transition from the prescaler (f1 in the timing diagram) then initiates the following sequence of events. Since the two state of the programmable counter enables the early decode circuitry in the MC12014, the positive f1 transition causes f_{out} to go low. Since f_{out} is connected to the Parallel Enables of all the MC4016 counters this low signal will re-program the counters in readiness for another cycle. However, due to the propagation time through the decode circuitry, the programmable and modulus control counters are briefly decremented to one and zero, respectively, before re-programming occurs. The momentary zero state of the modulus control counter is detected, setting E_O of the MC12014 high, enabling the MC12012 for division by ten during its next cycle. After eleven more f_{in} pulses (E_O went high after the beginning of the prescaler cycle and so doesn't change the modulus until the next prescaler cycle), f1 again goes high, causing f_{out} to return to the one state. This releases the Parallel Enables and simultaneously resets E_O to zero. However, since E_O was high when the current prescaler cycle began, the next positive f1 transition occurs only ten f_{in} pulses later. Subsequent f1 transitions now decrement the MC4016 counters down through another cycle with the prescaler dividing by eleven. From the waveforms, 11 + 10 + 11 + 11 = 43 input pulses occur for each output pulse.

Division by 42 is shown in Figure 7b. Operation is similar except that the modulus control counter reaches its terminal count one f1 cycle earlier than before. Since

FIGURE 6 – FREQUENCY DIVISION: $f_O = f_{in}/(MN_{pc} + N_{mc})$

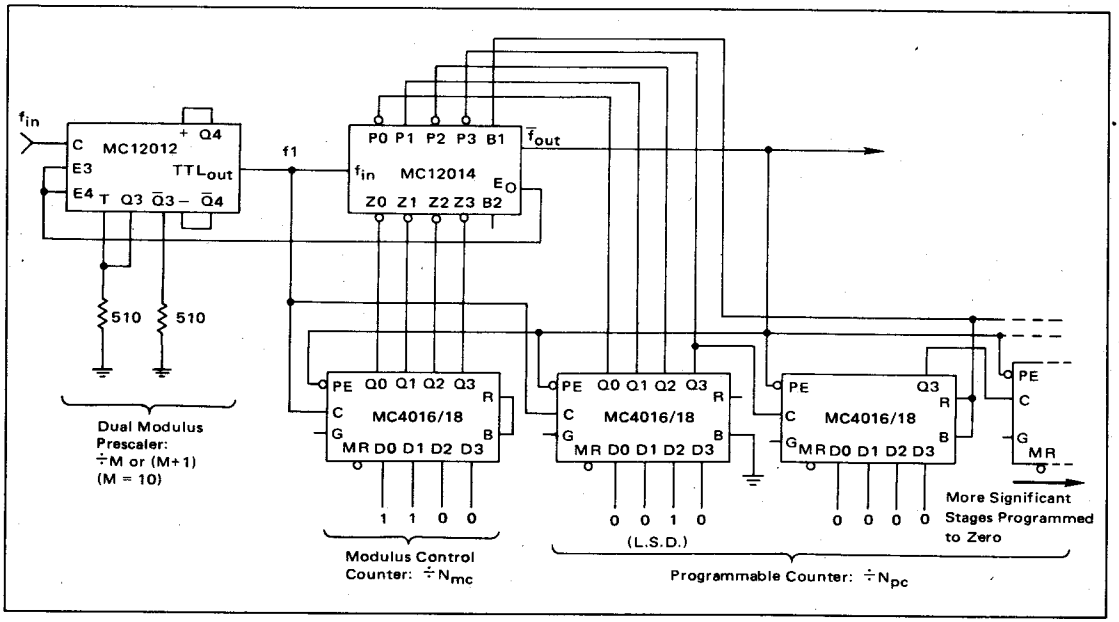


FIGURE 7a – DIVISION BY 43

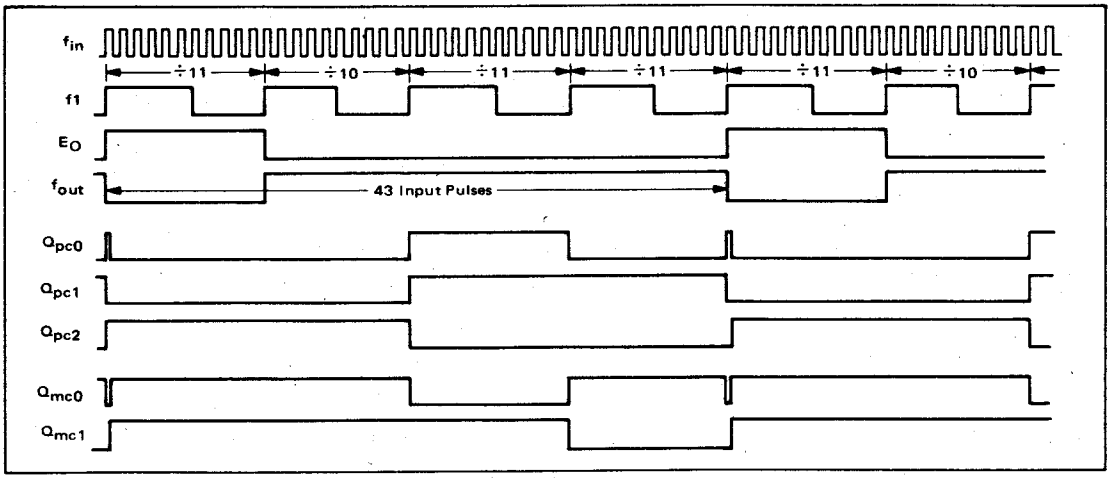
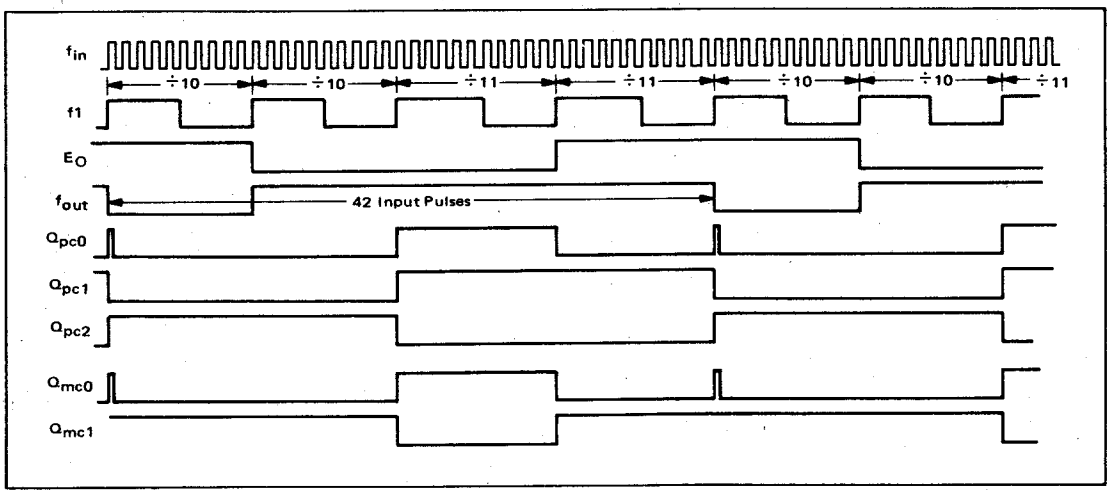


FIGURE 7b – DIVISION BY 42



E_O is reset by the trailing edge of the f_{out} pulse, E_O now remains high for two prescaler cycles leading to 10 + 10 + 11 + 11 = 42 input pulses for each output pulse.

Other combinations lead to similar results, however note that N_{pc} must be greater than or equal to N_{mc} for operation as described. If N_{mc} is greater than N_{pc} erroneous results are obtained, however this is not a serious restriction since N_{pc} is greater than N_{mc} in most practical applications.

The synthesizer shown in Figure 8 generates frequencies in the range from 144 to 178 MHz with 30 kHz channel spacing. It uses the dual modulus prescaler approach discussed earlier. General synthesizer design considerations are detailed in the publications listed in footnote 2, hence only the feedback counter is discussed here. Requirements for the feedback divider are determined from:

$$\text{Minimum Divider Ratio} = N_{Tmin} = \frac{144.00\ \text{MHz}}{30\ \text{kHz}} = 4800$$

$$\text{Maximum Divider Ratio} = N_{Tmax} = \frac{177.99\ \text{MHz}}{30\ \text{kHz}} = 5933$$

If the prescaler divides by at least ten, the maximum input frequency to the TTL counters will be 17.799 MHz, allowing use of MC4016 Programmable Counters with the MC12014 frequency extension feature.

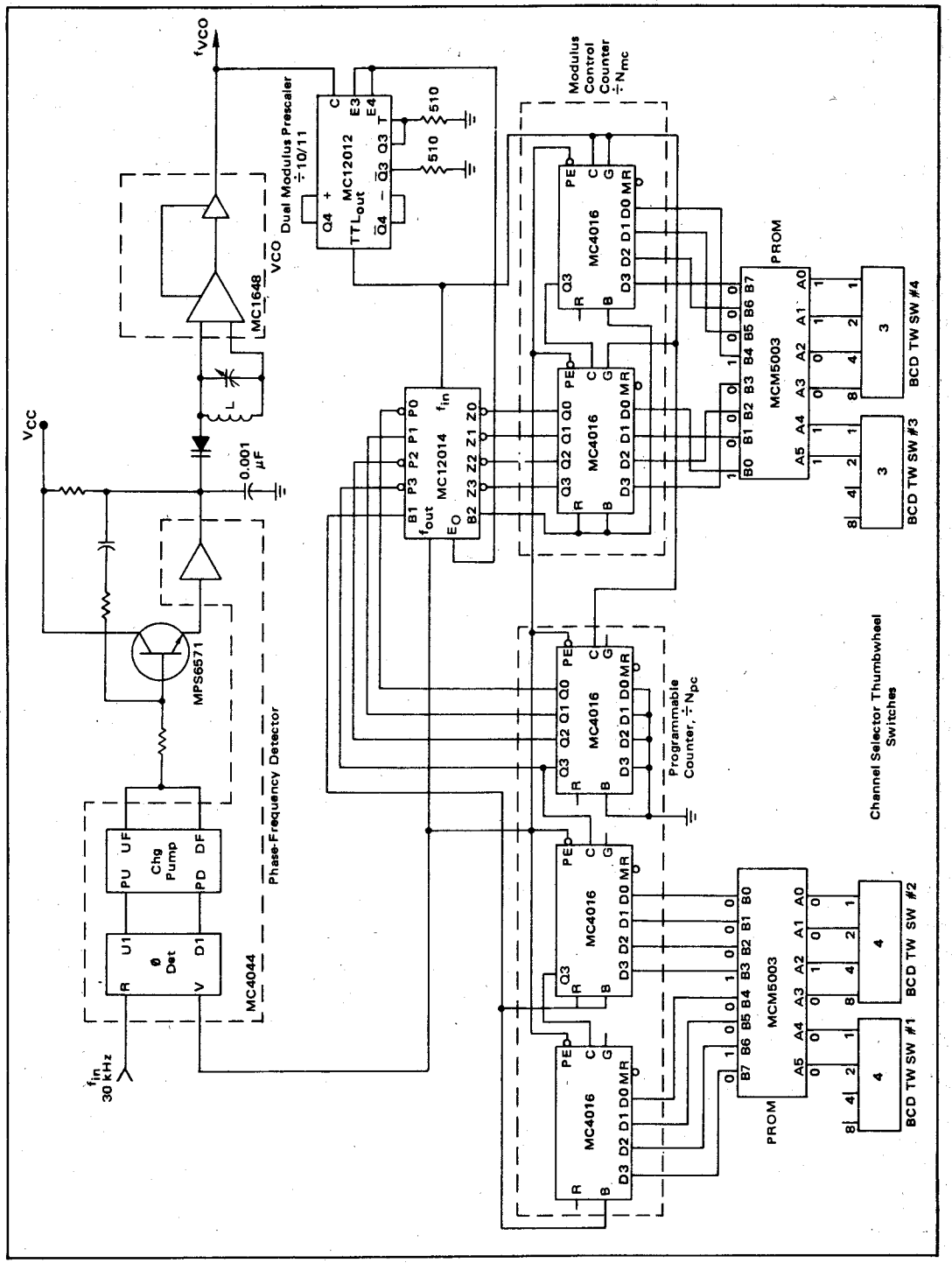


FIGURE 8 – 144 TO 178 MHz FREQUENCY SYNTHESIZER WITH 30 kHz CHANNEL SPACING

FIGURE 9 – N_{pc} PROM PROGRAMMING

	SW #1	SW #2	SW #1 A5 A4	SW #2 A3 A2 A1 A0	PROM WORD	PROM OUTPUT M.S.B.	PROM OUTPUT L.S.B.	N_{pc}	
(144 MHz)	44		0 1 0 0	0 1 0 0	4	0 1 0 0	1 0 0 0	48	480
	45		0 1 0 0	0 1 0 1	5	0 1 0 0	1 0 0 0	48	
	46		0 1 0 0	0 1 1 0	6	0 1 0 0	1 0 0 0	48	
	47		0 1 0 0	0 1 1 1	7	0 1 0 0	1 0 0 1	49	
	48		0 1 0 0	1 0 0 0	8	0 1 0 0	1 0 0 1	49	
	49		0 1 0 0	1 0 0 1	9	0 1 0 0	1 0 0 1	49	
	50		0 1 0 1	0 0 0 0	16	0 1 0 1	0 0 0 0	50	
	51		0 1 0 1	0 0 0 1	17	0 1 0 1	0 0 0 0	50	
	52		0 1 0 1	0 0 1 0	18	0 1 0 1	0 0 0 0	50	
	53		0 1 0 1	0 0 1 1	19	0 1 0 1	0 0 0 1	51	
	54		0 1 0 1	0 1 0 0	20	0 1 0 1	0 0 0 1	51	
	55		0 1 0 1	0 1 0 1	21	0 1 0 1	0 0 0 1	51	
	56		0 1 0 1	0 1 1 0	22	0 1 0 1	0 0 1 0	52	
	57		0 1 0 1	0 1 1 1	23	0 1 0 1	0 0 1 0	52	
	58		0 1 0 1	1 0 0 0	24	0 1 0 1	0 0 1 0	52	
	59		0 1 0 1	1 0 0 1	25	0 1 0 1	0 0 1 1	53	
	60		0 1 1 0	0 0 0 0	32	0 1 0 1	0 0 1 1	53	
	61		0 1 1 0	0 0 0 1	33	0 1 0 1	0 0 1 1	53	
	62		0 1 1 0	0 0 1 0	34	0 1 0 1	0 1 0 0	54	
	63		0 1 1 0	0 0 1 1	35	0 1 0 1	0 1 0 0	54	
	64		0 1 1 0	0 1 0 0	36	0 1 0 1	0 1 0 0	54	
	65		0 1 1 0	0 1 0 1	37	0 1 0 1	0 1 0 1	55	
	66		0 1 1 0	0 1 1 0	38	0 1 0 1	0 1 0 1	55	
	67		0 1 1 0	0 1 1 1	39	0 1 0 1	0 1 0 1	55	
	68		0 1 1 0	1 0 0 0	40	0 1 0 1	0 1 1 0	56	
	69		0 1 1 0	1 0 0 1	41	0 1 0 1	0 1 1 0	56	
	70		0 1 1 1	0 0 0 0	48	0 1 0 1	0 1 1 0	56	
	71		0 1 1 1	0 0 0 1	49	0 1 0 1	0 1 1 1	57	
	72		0 1 1 1	0 0 1 0	50	0 1 0 1	0 1 1 1	57	
	73		0 1 1 1	0 0 1 1	51	0 1 0 1	0 1 1 1	57	
	74		0 1 1 1	0 1 0 0	52	0 1 0 1	1 0 0 0	58	
	75		0 1 1 1	0 1 0 1	53	0 1 0 1	1 0 0 0	58	
	76		0 1 1 1	0 1 1 0	54	0 1 0 1	1 0 0 0	58	
(177 MHz)	77		0 1 1 1	0 1 1 1	55	0 1 0 1	1 0 0 1	59	590

WORD	BIT 7	6	5	4	3	2	1	0
0	–	–	–	–	–	–	–	–
1	–	–	–	–	–	–	–	–
2	–	–	–	–	–	–	–	–
3	–	–	–	–	–	–	–	–
4	0	1	0	0	1	0	0	0
5	0	1	0	0	1	0	0	0
6	0	1	0	0	1	0	0	0
7	0	1	0	0	1	0	0	1
8	0	1	0	0	1	0	0	1
9	0	1	0	0	1	0	0	1
10	–	–	–	–	–	–	–	–
11	–	–	–	–	–	–	–	–
12	–	–	–	–	–	–	–	–
13	–	–	–	–	–	–	–	–
14	–	–	–	–	–	–	–	–
15	–	–	–	–	–	–	–	–
16	0	1	0	1	0	0	0	0
17	0	1	0	1	0	0	0	0
18	0	1	0	1	0	0	0	0
19	0	1	0	1	0	0	0	1
20	0	1	0	1	0	0	0	1
21	0	1	0	1	0	0	0	1
22	0	1	0	1	0	0	1	0
23	0	1	0	1	0	0	1	0
24	0	1	0	1	0	0	1	0
25	0	1	0	1	0	0	1	1
26	–	–	–	–	–	–	–	–
27	–	–	–	–	–	–	–	–
28	–	–	–	–	–	–	–	–
29	–	–	–	–	–	–	–	–
30	–	–	–	–	–	–	–	–
31	–	–	–	–	–	–	–	–
32	0	1	0	1	0	0	1	1
33	0	1	0	1	0	0	1	1
34	0	1	0	1	0	1	0	0
35	0	1	0	1	0	1	0	0
36	0	1	0	1	0	1	0	0
37	0	1	0	1	0	1	0	1
38	0	1	0	1	0	1	0	1
39	0	1	0	1	0	1	0	1
40	0	1	0	1	0	1	1	0
41	0	1	0	1	0	1	1	0
42	–	–	–	–	–	–	–	–
43	–	–	–	–	–	–	–	–
44	–	–	–	–	–	–	–	–
45	–	–	–	–	–	–	–	–
46	–	–	–	–	–	–	–	–
47	–	–	–	–	–	–	–	–
48	0	1	0	1	0	1	1	0
49	0	1	0	1	0	1	1	1
50	0	1	0	1	0	1	1	1
51	0	1	0	1	0	1	1	1
52	0	1	0	1	1	0	0	0
53	0	1	0	1	1	0	0	0
54	0	1	0	1	1	0	0	0
55	0	1	0	1	1	0	0	1
56	–	–	–	–	–	–	–	–
57	–	–	–	–	–	–	–	–
58	–	–	–	–	–	–	–	–
59	–	–	–	–	–	–	–	–
60	–	–	–	–	–	–	–	–
61	–	–	–	–	–	–	–	–
62	–	–	–	–	–	–	–	–
63	–	–	–	–	–	–	–	–

The required divider range, 4800 to 5933, is obtained in the following manner: the MC12012 Dual Modulus Prescaler is connected in the divide by 10/11 mode; the modulus control counter uses two MC4016 stages with N_{mc} ranging from 00 to 99, establishing the two least significant digits of N_T. The remaining two digits of N_T are obtained from a three stage programmable counter generating N_{pc}. The least significant stage of the N_{pc} counter is fixed programmed to zero. The required programming for all remaining stages is derived from four channel selector BCD thumbwheel switches. The relationship between N_T and the counters is given by $N_T = MN_{pc} + N_{mc}$; for a typical channel, say 144.33 MHz, N_T = 4811 requires that M = 10, N_{pc} = 480, and N_{mc} = 11, or N_T = (10)(480) + 11 = 4811.

A general problem associated with synthesizer design arises from the fact that there is not always a one-to-one correspondence between the code provided by the channel selector switches and the code required for proper programming of the counters. For instance, in the example above where 144.33 MHz was selected, the channel selector switches are set to 44.33 while the required divider ratio is 4811. There are numerous solutions for a given translation requirement, however the method shown here using read only memories offers a straight-forward design method. While field programmable read only memories (PROMs)[3] are shown, they would normally be used only during development; suitable fixed ROMs are more economical in production quantities. The design procedure for the code conversion is illustrated in Figure 9. The required pro-

3 See the MCM5003 data sheet and AN-550 for details of operation; briefly, one of 64 eight-bit output words is selected by a six-bit address applied to the input. The word located at each address can be field programmed by the user.

FIGURE 10 – N_{mc} PROM # 1 PROGRAMMING

	SW #3	SW #4					PROM OUTPUT								
	SW #3	SW #4	A5	A4	A3	A2	A1	A0	PROM WORD	M.S.B				L.S.B.				N_{mc}
(144)	.00		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00
	.03		0	0	0	0	0	1	3	0	0	0	0	0	0	0	1	01
	.06		0	0	0	0	1	0	6	0	0	0	0	0	0	1	0	02
	.09		0	0	0	0	1	1	9	0	0	0	0	0	0	1	1	03
	.12		0	0	0	1	0	0	18	0	0	0	0	0	1	0	0	04
	.15		0	0	0	1	0	1	21	0	0	0	0	0	1	0	1	05
	.18		0	0	0	1	1	0	24	0	0	0	0	0	1	1	0	06
	.21		0	0	1	0	0	0	33	0	0	0	0	0	1	1	1	07
	.24		0	0	1	0	0	1	36	0	0	0	0	1	0	0	0	08
	.27		0	0	1	0	1	1	39	0	0	0	0	1	0	0	1	09
	.30		0	0	1	1	0	0	48	0	0	0	1	0	0	0	0	10
	.33		0	0	1	1	0	1	51	0	0	0	1	0	0	0	1	11
	.36		0	0	1	1	1	0	54	0	0	0	1	0	0	1	0	12
	.39		0	0	1	1	1	1	57	0	0	0	1	0	0	1	1	13
	.42		0	1	0	0	0	0	2	0	0	0	1	0	1	0	0	14
	.45		0	1	0	0	0	1	5	0	0	0	1	0	1	0	1	15
	.48		0	1	0	0	1	0	8	0	0	0	1	0	1	1	0	16
	.51		0	1	0	0	1	1	17	0	0	0	1	0	1	1	1	17
	.54		0	1	0	1	0	0	20	0	0	0	1	1	0	0	0	18
	.57		0	1	0	1	0	1	23	0	0	0	1	1	0	0	1	19
	.60		0	1	1	0	0	0	32	0	0	1	0	0	0	0	0	20
	.63		0	1	1	0	0	1	35	0	0	1	0	0	0	0	1	21
	.66		0	1	1	0	1	0	38	0	0	1	0	0	0	1	0	22
	.69		0	1	1	0	1	1	41	0	0	1	0	0	0	1	1	23
	.72		0	1	1	1	0	0	49	0	0	1	0	0	1	0	0	24
	.75		0	1	1	1	0	1	53	0	0	1	0	0	1	0	1	25
	.78		0	1	1	1	1	0	56	0	0	1	0	0	1	1	0	26
	.81		1	0	0	0	0	1	1	0	0	1	0	0	1	1	1	27
	.84		1	0	0	0	1	0	4	0	0	1	0	1	0	0	0	28
	.87		1	0	0	0	1	1	7	0	0	1	0	1	0	0	1	29
	.90		1	0	0	1	0	0	16	0	0	1	1	0	0	0	0	30
	.93		1	0	0	1	0	1	19	0	0	1	1	0	0	0	1	31
	.96		1	0	0	1	1	0	22	0	0	1	1	0	0	1	0	32
(144)	.99		1	0	0	1	1	1	25	0	0	1	1	0	0	1	1	33

Use with frequency ranges:

144.00 – 144.99	162.00 – 162.99
147.00 – 147.99	165.00 – 165.99
150.00 – 150.99	168.00 – 168.99
153.00 – 153.99	171.00 – 171.99
156.00 – 156.99	174.00 – 174.99
159.00 – 159.99	177.00 – 177.99

WORD	BIT 7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	1	1	1
2	0	0	0	1	0	1	0	0
3	0	0	0	0	0	0	0	1
4	0	0	1	0	1	0	0	0
5	0	0	0	1	0	1	0	1
6	0	0	0	0	0	0	1	0
7	0	0	1	0	1	0	0	1
8	0	0	0	1	0	1	1	0
9	0	0	0	0	0	0	1	1
10	–	–	–	–	–	–	–	–
11	–	–	–	–	–	–	–	–
12	–	–	–	–	–	–	–	–
13	–	–	–	–	–	–	–	–
14	–	–	–	–	–	–	–	–
15	–	–	–	–	–	–	–	–
16	0	0	1	1	0	0	0	0
17	0	0	0	1	0	1	1	1
18	0	0	0	0	0	1	0	0
19	0	0	1	1	0	0	0	1
20	0	0	0	1	1	0	0	0
21	0	0	0	0	0	1	0	1
22	0	0	1	1	0	0	1	0
23	0	0	0	1	1	0	0	1
24	0	0	0	0	0	1	1	0
25	0	0	1	1	0	0	1	1
26	–	–	–	–	–	–	–	–
27	–	–	–	–	–	–	–	–
28	–	–	–	–	–	–	–	–
29	–	–	–	–	–	–	–	–
30	–	–	–	–	–	–	–	–
31	–	–	–	–	–	–	–	–
32	0	0	1	0	0	0	0	0
33	0	0	0	0	0	1	1	1
34	–	–	–	–	–	–	–	–
35	0	0	1	0	0	0	0	1
36	0	0	0	0	1	0	0	0
37	–	–	–	–	–	–	–	–
38	0	0	1	0	0	0	1	0
39	0	0	0	0	1	0	0	1
40	–	–	–	–	–	–	–	–
41	0	0	1	0	0	0	1	1
42	–	–	–	–	–	–	–	–
43	–	–	–	–	–	–	–	–
44	–	–	–	–	–	–	–	–
45	–	–	–	–	–	–	–	–
46	–	–	–	–	–	–	–	–
47	–	–	–	–	–	–	–	–
48	0	0	0	1	0	0	0	0
49	0	0	1	0	0	1	0	0
50	–	–	–	–	–	–	–	–
51	0	0	0	1	0	0	0	1
52	–	–	–	–	–	–	–	–
53	0	0	1	0	0	1	0	1
54	0	0	0	1	0	0	1	0
55	–	–	–	–	–	–	–	–
56	0	0	1	0	0	1	1	0
57	0	0	0	1	0	0	1	1
58	–	–	–	–	–	–	–	–
59	–	–	–	–	–	–	–	–
60	–	–	–	–	–	–	–	–
61	–	–	–	–	–	–	–	–
62	–	–	–	–	–	–	–	–
63	–	–	–	–	–	–	–	–

gramming for the two most significant digits of N_{pc} is shown versus the code provided by switches #1 and #2 of the channel selector. If the four outputs of switch #2 and the two least significant outputs of switch #1 are regarded as address bits A0 through A5 for an MCM5003 PROM, a memory location can be associated with each switch setting. The required N_{pc} programming for each switch setting is then set into the appropriate memory location by the user. In Figure 9, the required programming has been transferred into a truth table to be used while programming the PROM. A similar result for the N_{mc} programming is shown in Figure 10. Note that the PROM shown, N_{mc} PROM #1, selects only N_{mc} numbers 00 through 33. This means that the synthesizer as shown in Figure 8 selects only the adjacent channels in a one megahertz slice of the total band. The frequency ranges that can be selected using N_{mc} PROM #1 are summarized in Figure 10. For other ranges, N_{mc} PROM #1 must be replaced by one of two additional PROMs required for generating the remaining N_{mc} numbers. Appropriate truth tables along with the ranges they can be used with are shown in Figures 11 and 12.

FIGURE 11 – N_{mc} PROM #2 TRUTH TABLE

WORD	BIT 7	6	5	4	3	2	1	0
0	0	1	1	0	0	0	0	0
1	0	1	0	0	0	1	1	1
2	0	0	1	1	0	1	0	0
3	0	1	1	0	0	0	0	1
4	0	1	0	0	1	0	0	0
5	0	0	1	1	0	1	0	1
6	0	1	1	0	0	0	1	0
7	0	1	0	0	1	0	0	1
8	0	0	1	1	0	1	1	0
9	0	1	1	0	0	0	1	1
10	–	–	–	–	–	–	–	–
11	–	–	–	–	–	–	–	–
12	–	–	–	–	–	–	–	–
13	–	–	–	–	–	–	–	–
14	–	–	–	–	–	–	–	–
15	–	–	–	–	–	–	–	–
16	0	1	0	1	0	0	0	0
17	0	0	1	1	0	1	1	1
18	0	1	1	0	0	1	0	0
19	0	1	0	1	0	0	0	1
20	0	0	1	1	1	0	0	0
21	0	1	1	0	0	1	0	1
22	0	1	0	1	0	0	1	0
23	0	0	1	1	1	0	0	1
24	0	1	1	0	0	1	1	0
25	0	1	0	1	0	0	1	1
26	–	–	–	–	–	–	–	–
27	–	–	–	–	–	–	–	–
28	–	–	–	–	–	–	–	–
29	–	–	–	–	–	–	–	–
30	–	–	–	–	–	–	–	–
31	–	–	–	–	–	–	–	–
32	0	1	0	0	0	0	0	0
33	–	–	–	–	–	–	–	–
34	0	1	0	1	0	1	0	0
35	0	1	0	0	0	0	0	1
36	–	–	–	–	–	–	–	–
37	0	1	0	1	0	1	0	1
38	0	1	0	0	0	0	1	0
39	–	–	–	–	–	–	–	–
40	0	1	0	1	0	1	1	0
41	0	1	0	0	0	0	1	1
42	–	–	–	–	–	–	–	–
43	–	–	–	–	–	–	–	–
44	–	–	–	–	–	–	–	–
45	–	–	–	–	–	–	–	–
46	–	–	–	–	–	–	–	–
47	–	–	–	–	–	–	–	–
48	–	–	–	–	–	–	–	–
49	0	1	0	1	0	1	1	1
50	0	1	0	0	0	1	0	0
51	–	–	–	–	–	–	–	–
52	0	1	0	1	1	0	0	0
53	0	1	0	0	0	1	0	1
54	–	–	–	–	–	–	–	–
55	0	1	0	1	1	0	0	1
56	0	1	0	0	0	1	1	0
57	–	–	–	–	–	–	–	–
58	–	–	–	–	–	–	–	–
59	–	–	–	–	–	–	–	–
60	–	–	–	–	–	–	–	–
61	–	–	–	–	–	–	–	–
62	–	–	–	–	–	–	–	–
63	–	–	–	–	–	–	–	–

Use with frequency ranges:

145.02 – 145.98	163.02 – 163.98
148.02 – 148.98	166.02 – 166.98
151.02 – 151.98	169.02 – 169.98
154.02 – 154.98	172.02 – 172.98
157.02 – 157.98	175.02 – 175.98
160.02 – 160.98	

FIGURE 12 – N_{mc} PROM #3 TRUTH TABLE

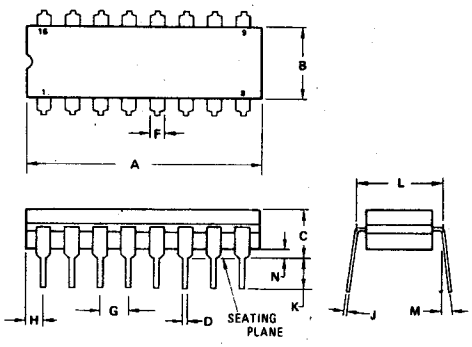
WORD	BIT 7	6	5	4	3	2	1	0
0	1	0	0	0	0	0	0	0
1	0	1	1	0	0	1	1	1
2	1	0	0	1	0	1	0	0
3	1	0	0	0	0	0	0	1
4	0	1	1	0	1	0	0	0
5	1	0	0	1	0	1	0	1
6	1	0	0	0	0	0	1	0
7	0	1	1	0	1	0	0	1
8	1	0	0	1	0	1	1	0
9	1	0	0	0	0	0	1	1
10	–	–	–	–	–	–	–	–
11	–	–	–	–	–	–	–	–
12	–	–	–	–	–	–	–	–
13	–	–	–	–	–	–	–	–
14	–	–	–	–	–	–	–	–
15	–	–	–	–	–	–	–	–
16	0	1	1	1	0	0	0	0
17	1	0	0	1	0	1	1	1
18	1	0	0	0	0	1	0	0
19	0	1	1	1	0	0	0	1
20	1	0	0	1	1	0	0	0
21	1	0	0	0	0	1	0	1
22	0	1	1	1	0	0	1	0
23	1	0	0	1	1	0	0	1
24	1	0	0	0	0	1	1	0
25	0	1	1	1	0	0	1	1
26	–	–	–	–	–	–	–	–
27	–	–	–	–	–	–	–	–
28	–	–	–	–	–	–	–	–
29	–	–	–	–	–	–	–	–
30	–	–	–	–	–	–	–	–
31	–	–	–	–	–	–	–	–
32	–	–	–	–	–	–	–	–
33	1	0	0	0	0	1	1	1
34	0	1	1	1	0	1	0	0
35	–	–	–	–	–	–	–	–
36	–	–	–	–	–	–	–	–
37	0	1	1	1	0	1	0	1
38	1	0	0	0	1	0	0	0
39	1	0	0	0	1	0	0	1
40	0	1	1	1	0	1	1	0
41	–	–	–	–	–	–	–	–
42	–	–	–	–	–	–	–	–
43	–	–	–	–	–	–	–	–
44	–	–	–	–	–	–	–	–
45	–	–	–	–	–	–	–	–
46	–	–	–	–	–	–	–	–
47	–	–	–	–	–	–	–	–
48	1	0	0	1	0	0	0	0
49	0	1	1	1	0	1	1	1
50	–	–	–	–	–	–	–	–
51	1	0	0	1	0	0	0	1
52	0	1	1	1	1	0	0	0
53	–	–	–	–	–	–	–	–
54	1	0	0	1	0	0	1	0
55	0	1	1	1	1	0	0	1
56	–	–	–	–	–	–	–	–
57	1	0	0	0	0	0	1	1
58	–	–	–	–	–	–	–	–
59	–	–	–	–	–	–	–	–
60	–	–	–	–	–	–	–	–
61	–	–	–	–	–	–	–	–
62	–	–	–	–	–	–	–	–
63	–	–	–	–	–	–	–	–

Use with frequency ranges:

146.01 – 146.97	164.01 – 164.97
149.01 – 149.97	167.01 – 167.97
152.01 – 152.97	170.01 – 170.97
155.01 – 155.97	173.01 – 173.97
158.01 – 158.97	176.01 – 176.97
161.01 – 161.97	

OUTLINE DIMENSIONS

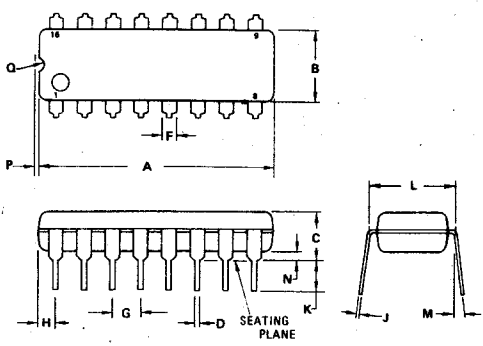
CASE 620-02



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2. PKG. INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.31	0.008	0.012
K	3.18	0.30	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15^0	–	15^0
N	0.51	1.02	0.020	0.040

CASE 648-03



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030