MC12020 • MC12520

OFFSET CONTROL

MC12021 • MC12521

OFFSET PROGRAMMER

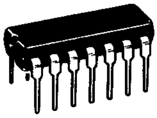
MC12020 • MC12520

The MC12020/520 is an IF offset control block that provides a digital means of producing automatic IF offset generation for synthesizer tuned transceivers when used in conjunction with the MC12021 or MC12521. It is a modified D-type flip-flop that is capable of two modes of operation. The mode of operation is controlled by the receive/transmit input. When the R/T input is at a logical one level, the part becomes simply a toggle flip-flop and divides by two at both Q and $\overline{Q}$ outputs. With the R/T input at a logical zero level, the Q output becomes a buffer gate that follows the clock input and the $\overline{Q}$ output produces a constant one level. An inverter gate is provided which can be used to invert the clock polarity. This option is to ensure the device can always be clocked on the same edge that clears the counter presets. This device was designed for low frequency operation which allows low power operation. Its maximum current drain is 9.6 mA over temperature.

MC12021 • MC12521

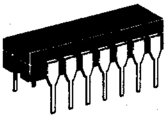
The MC12021/521 is an IF offset programmer that provides a means of producing automatic IF offset generation for synthesizer tuned transceivers when used in conjunction with the MC12020 or the MC12520 control block. The part is an eight-input, four-output data selector. It is the logic implementation of a four-pole, two position switch with the switch position controlled by the enable input. One set of input codes determine the frequency of transmission and is programmable with either switches or circuitry; the other code determines the IF offset frequency. The enable input is controlled by the $\overline{Q}$ output of the MC12020/520. This device was designed for low frequency operation which allows for low power operation. Maximum current drain is 9.4 mA over temperature.

MC12020, MC12520



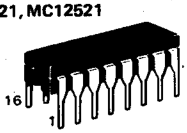
L SUFFIX
CERAMIC PACKAGE
CASE 632

MC12020



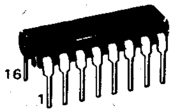
P SUFFIX
PLASTIC PACKAGE
CASE 646

MC12021, MC12521



L SUFFIX
CERAMIC PACKAGE
CASE 620

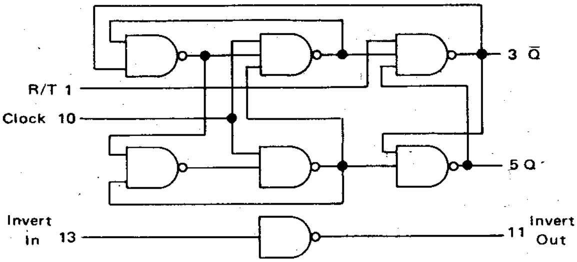
MC12021



P SUFFIX
PLASTIC PACKAGE
CASE 648

LOGIC DIAGRAMS

MC12020 • MC12520

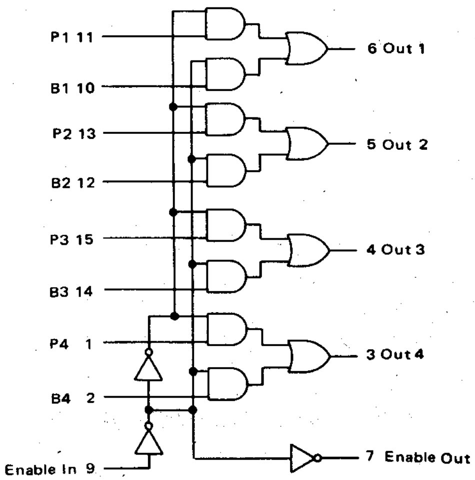


MC12020 • MC12520

Functional Truth Table			
Input		Output	
R/T	Clock	Q	$\overline{Q}$
0	0	0	1
0	1	1	1
1	1	1	0
1	0	1	0
1	1	0	1

V_{CC} = Pin 14 = +5.0 Vdc
Gnd = Pin 7
0 @ Clock, R/T = +0.5 Vdc
1 @ Clock, R/T = +4.0 Vdc

MC12021 • MC12521



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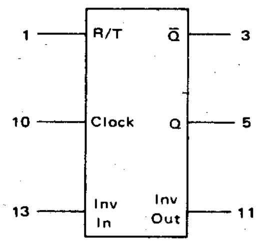
ELECTRICAL CHARACTERISTICS

Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

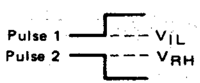
*The device must be tested by sequencing through the tests maintaining power supply and ground voltages between tests. Procedures with (**) are necessary to get device into proper state for testing.



TEST CURRENT/VOLTAGE VALUES (All Temperatures)

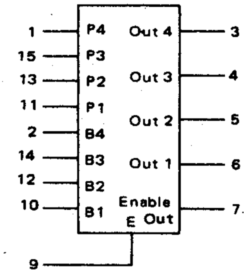
	I_{OL} (mA)	I_{OH} (mA)	I_{IC} (mA)	V_{IL} (Volts)	V_{IH}	V_{IHH}	V_{RH}	V_{ILT}	V_{IHT}	V_{CCL}	V_{CCH}
MC12520	8.0	0.2	-10	0.5	2.4	5.5	4.0	0.7	2.0	4.5	5.5
MC12020	8.0	0.2	-10	0.5	2.4	5.5	4.0	0.7	2.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC12520 Test Limits -55 to +125°C Min	Max	Unit	MC12020 Test Limits -30 to +85°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{IC}	V_{IL}	V_{IH}	V_{IHH}	V_{RH}	V_{ILT}	V_{IHT}	V_{CCL}	V_{CCH}	Pulse 1	Pulse 2	Gnd
Input Forward Current	I_{IL}	1	-1.0	–	mAdc	-1.0	–	mAdc	–	–	–	1	–	–	10	–	–	–	14	–	–	7
		10	-0.75	–	mAdc	-0.75	–	mAdc	–	–	–	1,10	–	–	–	–	–	–	14	–	–	7
		13	-1.0	–	mAdc	-1.0	–	mAdc	–	–	–	13	–	–	–	–	–	–	14	–	–	7
Leakage Current*	I_{IH}	10	–	150	µAdc	–	150	µAdc	–	–	–	1	10	–	–	–	–	–	14	10	–	7
		1	–	↓	µAdc	–	↓	µAdc	–	–	–	–	1	–	10	–	–	–	14	–	–	7
		13	–	↓	µAdc	–	↓	µAdc	–	–	–	–	13	–	–	–	–	–	14	–	–	7
	I_{IHH}	10	–	1.0	mAdc	–	1.0	mAdc	–	–	–	1	–	10	–	–	–	–	14	10	–	7
		**	–	–	–	–	–	–	–	–	–	10	–	–	1	–	–	–	14	–	10	7
		1	–	1.0	mAdc	–	1.0	mAdc	–	–	–	–	–	1	10	–	–	–	14	–	–	7
		13	–	1.0	mAdc	–	1.0	mAdc	–	–	–	–	–	13	–	–	–	–	14	–	–	7
Clamp Voltage	V_{IC}	1	-1.5	–	Vdc	-1.5	–	Vdc	–	–	1	–	–	–	10	–	–	14	–	–	–	7
		10	-1.5	–	Vdc	-1.5	–	Vdc	–	–	10	–	–	–	1	–	–	14	–	–	–	7
		13	-1.5	–	Vdc	-1.5	–	Vdc	–	–	13	–	–	–	–	–	–	14	–	–	–	7
Output Output Voltage*	V_{OL}	5	–	0.5	Vdc	–	0.5	Vdc	5	–	–	–	–	–	–	1,10	–	14	–	–	–	7
		**	–	–	–	–	–	–	–	–	–	–	–	–	–	1	–	14	–	10	–	7
		3	–	0.5	Vdc	–	0.5	Vdc	3	–	–	–	–	–	–	–	1,10	14	–	–	–	7
		11	–	0.5	Vdc	–	0.5	Vdc	11	–	–	–	–	–	–	–	13	14	–	–	–	7
	V_{OH}	3	2.4	–	Vdc	2.4	–	Vdc	–	3	–	–	–	–	–	1,10	–	14	–	–	–	7
		5	2.4	–	Vdc	2.4	–	Vdc	–	5	–	–	–	–	–	1	10	14	–	–	–	7
		11	2.4	–	Vdc	2.4	–	Vdc	–	11	–	–	–	–	–	13	–	14	–	–	–	7
Short-Circuit Current*	I_{OS}	3	-38	–	mAdc	-38	–	mAdc	–	–	–	1	–	–	10	–	–	–	14	10	–	3,7
		5	-38	–	mAdc	-38	–	mAdc	–	–	–	1	–	–	10	–	–	–	14	–	–	5,7
		11	-38	–	mAdc	-38	–	mAdc	–	–	–	13	–	–	–	–	–	–	14	–	–	7,11
Power Requirements (Total Device) Power Supply	I_{PD}	14	–	9.6	mAdc	–	9.6	mAdc	–	–	–	–	–	–	–	–	–	–	14	–	–	7



ELECTRICAL CHARACTERISTICS

Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

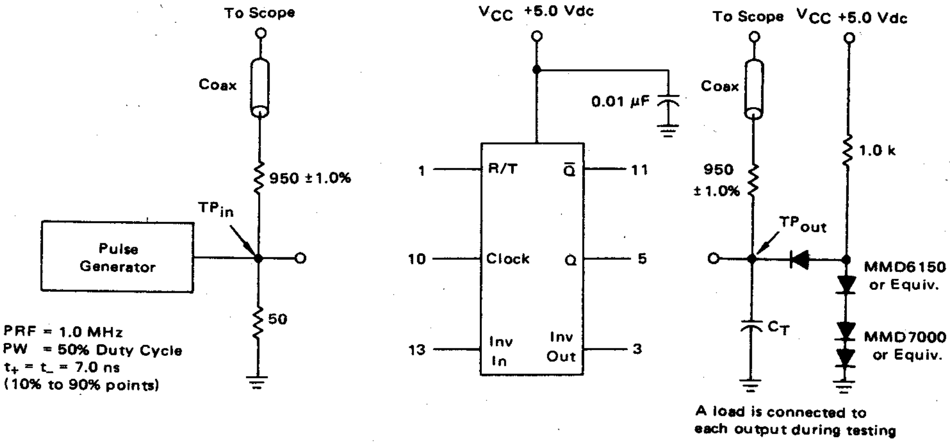


TEST CURRENT/VOLTAGE VALUES (All Temperatures)

	mA					Volts							
	I_{OL1}	I_{OL2}	I_{OH1}	I_{OH2}	I_{IC}	V_{IL}	V_{IH}	V_{IHH}	V_{RH}	V_{ILT}	V_{IHT}	V_{CCL}	V_{CCH}
MC12521	13	1.6	0.4	0.1	-10	0.5	2.4	5.5	4.0	0.7	2.0	4.5	5.5
MC12021	13	1.6	0.4	0.1	-10	0.5	2.4	5.5	4.0	0.7	2.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC12521 Test Limits -55 to +125°C Min	Max	Unit	MC12021 Test Limits -30 to +85°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH1}	I_{OH2}	I_{IC}	V_{IL}	V_{IH}	V_{IHH}	V_{RH}	V_{ILT}	V_{IHT}	V_{CCL}	V_{CCH}	Gnd
Input Forward Current	I_{IL}	1	-0.12	–	mAdc	-0.12	–	mAdc	–	–	–	–	–	1	–	–	9	–	–	–	16	8
		2	-0.12	–	mAdc	-0.12	–	mAdc	–	–	–	–	–	2,9	–	–	–	–	–	–	16	8
		9	-0.12	–	mAdc	-0.12	–	mAdc	–	–	–	–	–	9	–	–	–	–	–	–	16	8
Leakage Current	I_{IH}	1		40	µAdc	–	40	µAdc	–	–	–	–	–	9	1	–	–	–	–	–	16	8
		2		40	µAdc	–	40	µAdc	–	–	–	–	–	–	2	–	9	–	–	–	16	8
		9		40	µAdc	–	40	µAdc	–	–	–	–	–	–	9	–	–	–	–	–	16	8
	I_{IHH}	1		1.0	mAdc		1.0	mAdc	–	–	–	–	–	9	–	1	–	–	–	–	16	8
		2		1.0	mAdc	–	1.0	mAdc	–	–	–	–	–	–	–	2	9	–	–	–	16	8
		9	–	1.0	mAdc	–	1.0	mAdc	–	–	–	–	–	–	–	9	–	–	–	–	16	8
Clamp Voltage	V_{IC}	1	-1.5	–	Vdc	-1.5	–	Vdc		–	–	–	1	–	–	–	–	–	–	16	–	8
		2	-1.5	–	Vdc	-1.5	–	Vdc		–	–	–	2	–	–	–	–	–	–	16	–	8
		9	-1.5	–	Vdc	-1.5	–	Vdc		–	–	–	9	–	–	–	–	–	–	16	–	8
Output Output Voltage	V_{OL}	6		0.5	Vdc	–	0.5	Vdc	–	6		–	–	–	–	–	–	9,10	1,2,11,12, 13,14,15	16	–	8
		7		0.5	Vdc		0.5	Vdc	7	–	–	–	–	–	–	–	–	9	1,2,10,11, 12,13,14,15	16	–	8
	V_{OH}	6	2.4	–	Vdc	2.4	–	Vdc	–	–	–	6	–	–	–	–	–	1,13,15	2,9,10,11, 12,14	16	–	8
		7	2.4	–	Vdc	2.4	–	Vdc	–	–	7	–	–	–	–	–	–	1,11,13,15	2,9,10, 12,14	16	–	8
Short-Circuit Current	I_{OS}	6	-8.0	–	mAdc	-8.0	–	mAdc	–	–	–	–	–	–	–	–	–	1,13,15	2,9,10,11, 12,14	–	16	6,8
		7	-70	–	mAdc	-70		mAdc		–	–	–	–	–	–	–	–	1,11,13,15	2,9,10,12, 14	–	16	7,8
Power Requirements (Total Device) Power Supply	I_{PDL}	16	–	9.4	mAdc	–	9.4	mAdc	–			–	–	1,2,9,10, 11,12,13, 14,15	–	–	–	–	–	–	16	8

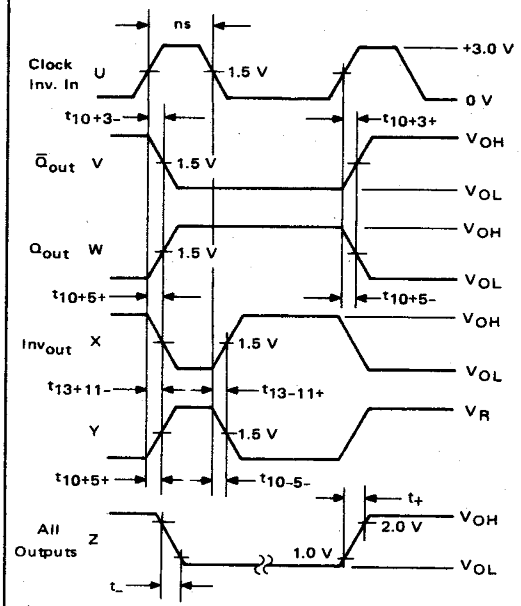
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS FOR MC12020, MC12520



A load is connected to each output during testing

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.
The coax delays from input to scope and output to scope must be matched.
The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

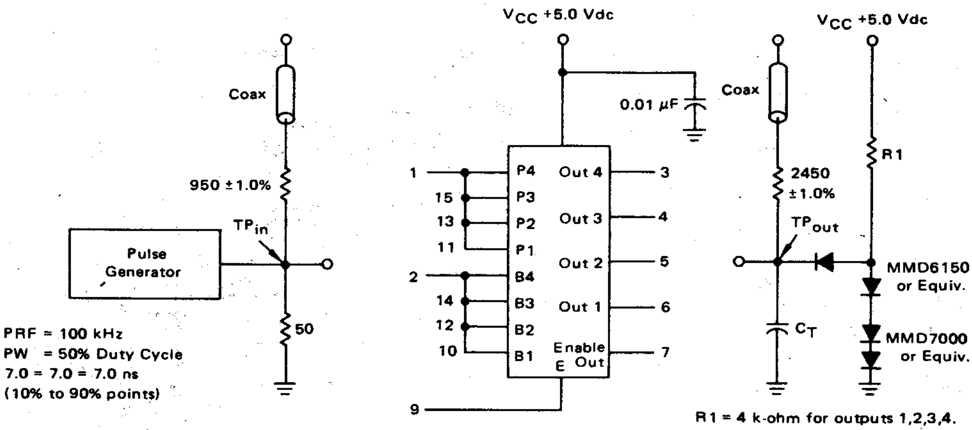
PROPAGATION DELAY TIMES



AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, waveform letters refer to the waveforms.)

Characteristic	Symbol	Pin Under Test In	Pin Under Test Out	Test Limits (ns) MC12020/520 −55°C to +25°C Typ	Test Limits (ns) MC12020/520 +85°C to +125°C Max	Pulse Gen. Waveform	Pulse Gen. Pin	Pulse Out Waveform	Pulse Out Pin	Voltage Applied to Pins Listed Below 2.4 V	Voltage Applied to Pins Listed Below 0.5 V
Propagation Delay	t_{10+3+}	10	3	95	87	U	10	V	3	1	–
	t_{10+3-}	10	3	56	48	U	10	V	3	1	–
	t_{10+5+}	10	5	47	48	U	10	W	5	1	–
	t_{10+5-}	10	5	99	87	U	10	W	5	1	–
	t_{10+5+}	10	5	47	48	U	10	Y	5	–	1
	t_{10-5-}	10	5	29	36	U	10	Y	5		1
	t_{13+11-}	13	11	5.6	3.3	U	13	X	11	–	–
	t_{13-11+}	13	11	18	50	U	13	X	11	–	–
Risetime	t_{3+}	10	3	11.1	18	U	10	Z	3	1	–
	t_{5+}	10	5	8.7	17	U	10	Z	5	1	–
	t_{11+}	13	11	18	35	U	13	Z	11	–	–
Falltime	t_{3-}	10	3	3.5	3.5	U	10	Z	3	1	–
	t_{5-}	10	5	4.0	4.6	U	10	Z	5	1	–
	t_{11-}	13	11	3.4	3.3	U	13	Z	11	–	–

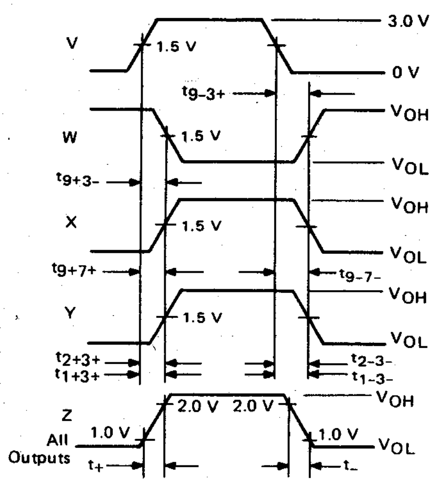
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS FOR MC12021, MC12521



C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched.
The scope must be terminated in 50-ohm impedance. The 2450-ohm resistor and the scope termination impedance constitute a 50:1 attenuator probe. The 950 Ω resistor and the scope impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

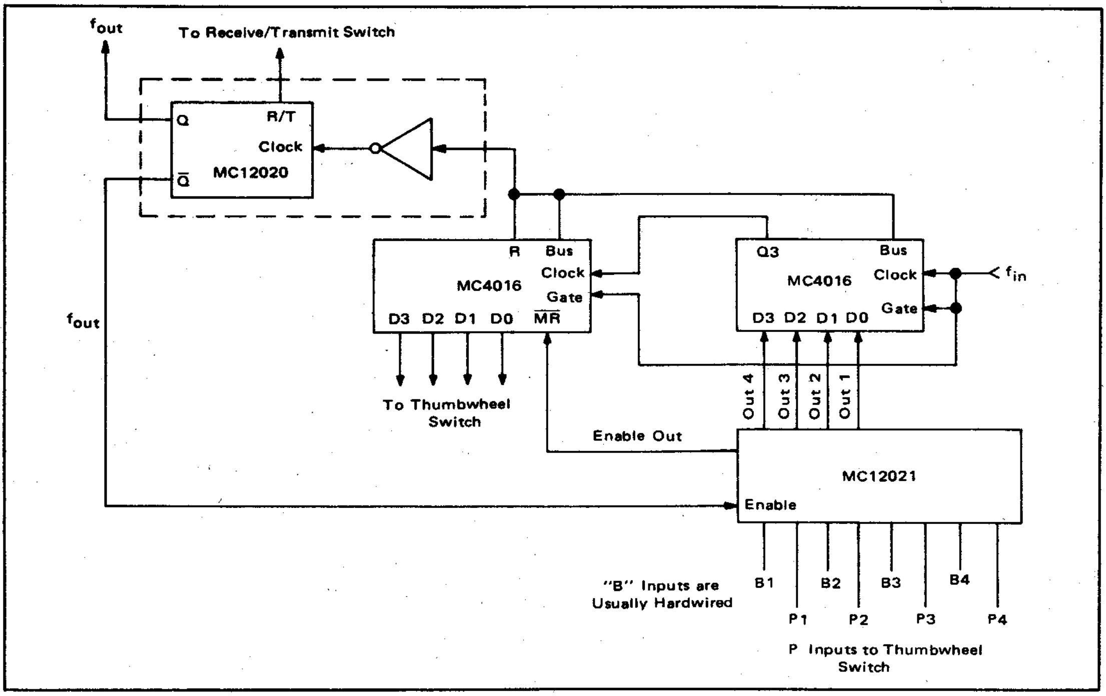
PROPAGATION DELAY TIMES



AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, waveform letters refer to the waveforms.)

Characteristic	Symbol	Pin Under Test In	Pin Under Test Out	Test Limits (ns) MC12021/521 −55°C to +25°C Typ	Test Limits (ns) MC12021/521 +85°C to +125°C Max	Pulse Gen. Waveform	Pulse Gen. Pin	Pulse Out Waveform	Pulse Out Pin	Voltage Applied to Pins Listed Below 2.4 V	Voltage Applied to Pins Listed Below 0.5 V
Propagation Delay	t_{9+3-}	9	3	234	231	V	9	W	3	2	1
	t_{9-3+}	9	3	108	132	V	9	W	3	2	1
	t_{2-3-}	2	3	164	171	V	2	Y	3	1	9
	t_{2+3+}	2	3	129	119	V	2	Y	3	1	9
	t_{1-3-}	1	3	161	170	V	1	Y	3	9	2
	t_{1+3+}	1	3	128	117	V	1	Y	3	9	2
	t_{9-7-}	9	7	80	84	V	9	X	7	2	1
	t_{9+7+}	9	7	128	147	V	9	X	7	2	1
Risetime	t_{3+}	9	3	23	32	V	9	Z	3	2	1
	t_{7+}	9	7	9.6	12	V	9	Z	7	2	1
Falltime	t_{3-}	9	3	18	21	V	9	Z	3	2	1
	t_{7-}	9	7	20	23	V	9	Z	7	2	1

FIGURE 1 – BASIC DUAL PRESETTING TECHNIQUE



APPLICATION INFORMATION

The frequency generating section of a multichannel transceiver must be capable of two major functions: 1) generate the exact transmit frequency for any one of many channels selectable by a front panel control, and 2) offset, within milliseconds, the transmit frequency by plus (or minus) the intermediate frequency (IF) when the receive mode is selected. The digitally programmed frequency synthesizer (PLL) is well suited to the solution of multichannel frequency generation, and its use as the local oscillator in channelized transceivers is widely accepted. With the parts and literature available, the implementation of a synthesizer to generate a band of channelized frequencies is straightforward with only the V_{CO} and loop filter left as design variables. A synthesizer allows channel selection by the use of front panel thumbwheel switches which display the transmit frequency selected.

Several methods exist for obtaining the frequency offset required during receive. Unfortunately, none of the present techniques offer a universal solution for all transceivers. Three methods for frequency offsetting presently available to the transceiver designer are mixing, direct logic implementation, and adders. The mixing method is widely used because of price and simplicity. The mixing technique has the disadvantage of: 1) requiring an additional oscillator at the IF frequency; 2) except for applications requiring a narrow tuning range, the tank circuit for the mixer must be designed to track the synthesizer oscillator; and 3) spurious frequencies are generated which can severely degrade system performance.

For certain applications where tuning range is wide and the IF frequency is simple (10 MHz, 20 MHz, etc.) the addition of logic circuitry to the programming inputs to add, on command, the IF frequency to the transmit frequency is simple and inexpensive. This technique is used in several aircraft radios built today. The technique becomes prohibitive because of logic complexity, number of packages, and power for standard IF frequencies, such as 10.7 MHz, 21.4 MHz, etc., and for frequency bands where the IF offset cannot be accomplished by adding (or subtracting) a number to the most significant divider in the divider chain.

Adders offer a universal solution for frequency offsetting for any IF frequency but are used in very few applications because of: 1) the large number of packages required; 2) power dissipation; 3) the price; and 4) the difficulty of obtaining NBCD adders.

The MC12020/520 (offset control) and the MC12021/521 (offset programmer) combination offers a new method for frequency offsetting. The new method is referred to as "dual presetting" and allows the implementation of any IF frequency in a very straightforward manner. The complexity of the system depends on the IF frequency required, but is always less complex than the adder method and is competitive with the direct implementation method for specific applications.

The dual presetting method is applied in the low frequency section of a synthesizer and does not require high performance, high powered units to accomplish its function. The method does not require an additional oscillator and tank circuits as does the mixing method.

The dual presetting (MC12020 and MC12021) system produces the required shift in frequency by adding the IF frequency to the transmit frequency. The system accomplishes this addition by alternately programming the divide counters to the transmit frequency and the IF frequency.

The MC12020/520 is a modified D-type flip-flop that is capable of two modes of operation. The mode is controlled by the R/T (Receive/Transmit) input. With the R/T input at a logical one level, the part divides by two at both the Q and $\overline{Q}$ outputs. With the R/T input at a logical zero level, the Q output becomes a buffer gate that follows the clock input, and the $\overline{Q}$ output produces a logical one level. An inverter gate is provided which can be used to invert the clock polarity of the MC12020. This option is to ensure the MC12020 can always be clocked on the same edge that clears the counter presets.

The MC12021/521 is an eight-input, four-output data selector constructed from low level TTL gates. It is the logic implementation of a four-pole, two-position switch with the switch position controlled by the enable input. A buffer output that follows the enable input is provided and can be used to program divide counters to zero when necessary.

The operation of the dual presetting method can best be described for one MC12020, one MC12021 and two MC4016 counters (see Figure 1). The transmit code (N1) is seventeen (0001, 0111) and the IF code (N2) is eight (0000, 1000). The buffer out of the MC12021 is connected to the master reset ($\overline{MR}$) of the most significant counter (MS). The outputs of the MC12021 are connected to the programming inputs of the least significant (LS) counter. The number one is programmed into the MS counter programming inputs, and the numbers seven and eight are programmed into the P and B inputs, respectively, of the MC12021. The inverter gate in the MC12020 is used to invert the bus out from the counters allowing the MC12021

FIGURE 2 – TIMING DIAGRAM FOR SYSTEM OF FIGURE 1 (R/T Input High)

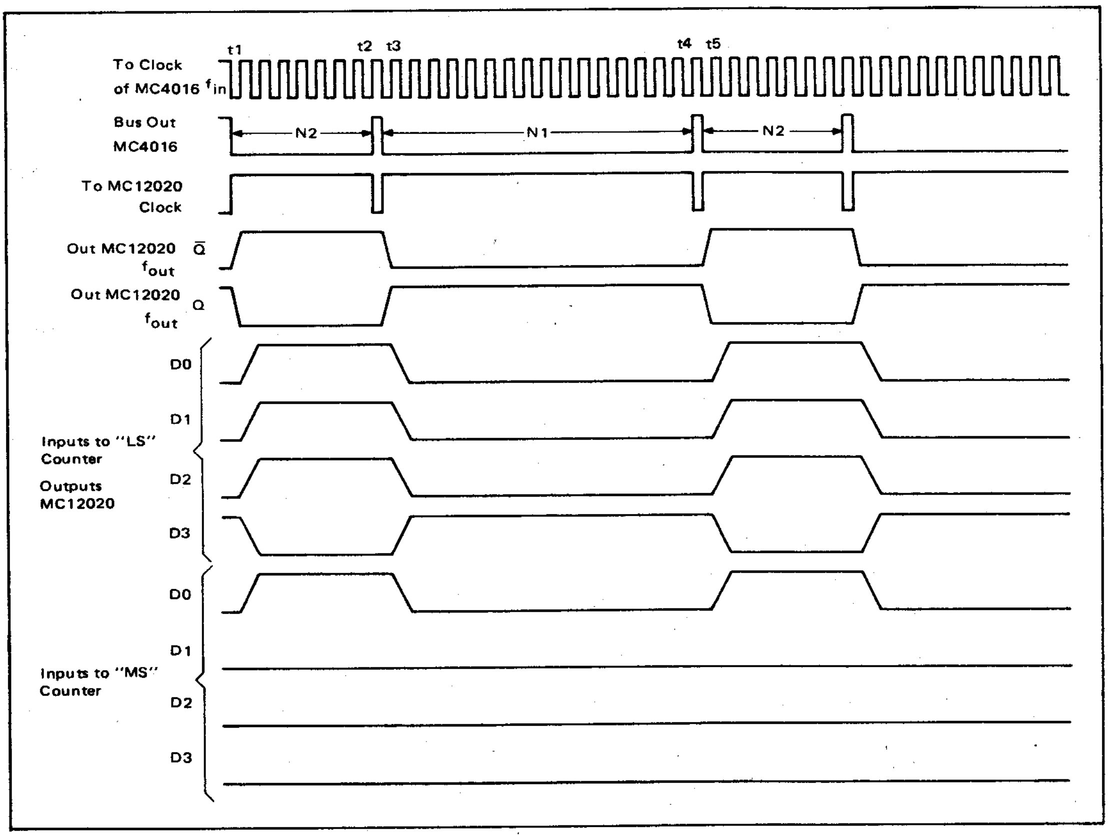
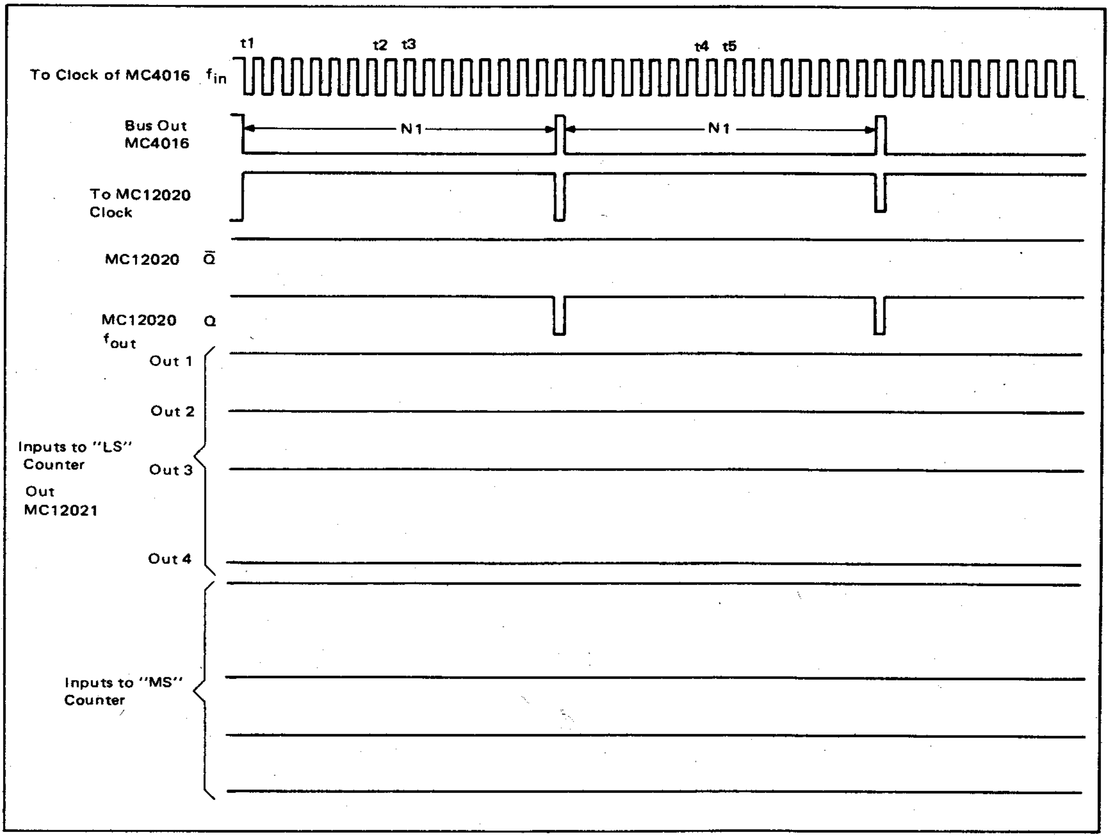


FIGURE 3 – TIMING DIAGRAM FOR SYSTEM OF FIGURE 1 (R/T Input Low)



the maximum time to change the counters' programming.

To illustrate the operation of the system, assume the R/T input at a logical one level, the Q out is a logical one, the counters have been decremented to zero, and the bus output has just gone to a logical one level (see Figure 2). The $\overline{Q}$ output is a logical zero level, the number eight is on the programming inputs of the LS counter, the number zero is on the $\overline{MR}$ of the MS counter, and the preset logic of the counters is enabled.

The negative transition of the clock at t1 presets the number eight in the LS counter and zero in the MS counter. The change in programming forces the bus output to a logical zero level, inhibiting the counter preset logic, changing the state of the MC12020, and enabling the counters. The state change of the MC12020 puts the $\overline{Q}$ output at a logical one level which forces the MC12021 to route the number seven to the LS counter and clears the zero from the $\overline{MR}$ of the MS counter allowing the number one to be programmed. Since the counters preset new information only when the bus output is high, the changing numbers have no effect until the next positive transition of the bus output. The positive transition at t2 decrements the counters to zero causing the bus output to go high enabling the counter presets. The negative transition of the clock at t3 presets the number one and seven into the MS and LS counters, respectively. The bus output goes low, clears the preset, enables the count down, and clocks the MC12020. The $\overline{Q}$ output goes low routing zero and eight counters. Seventeen clock pulses later the transition at t4 and t5 brings the system back to the initial conditions completing one cycle. The system will continue in a like manner until the R/T input is taken low. The frequency out will be the frequency in divided by N1 plus N2 (f_{in} $\div$[8+17]). The MC12020 and MC12021 combination has added the IF code to the transmit code by alternately programming the divide counters to N1 and N2.

The R/T input is taken low to place the MC12020 in the transmit mode. The logical zero on the R/T input forces the $\overline{Q}$ output to a logical one level selecting, through the MC12021, code N1. The $\overline{Q}$ output will remain a logical one and the Q output will follow the input to the MC12020 until the R/T input is taken high.

For purposes of description, assume that some time prior to the transition at t1 (see Figure 3) the R/T input was taken low. The transitions at t1 and t2 program the counters to N1 and seventeen clock pulses later the transitions at t3 and t4 repeat the process. As long as the R/T input remains low the code on the counter inputs will remain unchanged and the output frequency will be the input frequency divided by N1 ($f_{in} \div 17$).

The operation for this simplified system is valid for any number of MC12021's and counters. The number of MC12021's required by any system is a function of the required IF frequency. The number needed to implement a given IF frequency is equal to the number of non-zero integers in the IF frequency. The buffer output of the MC12021 and the master reset on the MC4016's allow zeros to be programmed without the addition of a package. For example, the IF of 67.02 MHz requires three MC12021's while the IF of 100.02 MHz requires only two.

The synthesizer shown in Figure 4 is designed to operate over the aircraft frequencies from 118 to 136 MHz in 25 kHz steps while in the transmit mode and will add 10.7 MHz to any transmit frequency in the receive mode. The synthesizer is a typical phase-lock loop (PLL) system that uses one MC12020 and two MC12021's. The system's mode of operation is controlled by the R/T input of the MC12020; a logical one for receive mode and a logical zero for transmit mode.

The MC12020/520 and MC12021/521 are implemented

FIGURE 4 – TYPICAL PLL SYNTHESIZER SYSTEM USING MC12020/520, MC12021/521 CIRCUITS TO ACCOMPLISH IF OFFSET

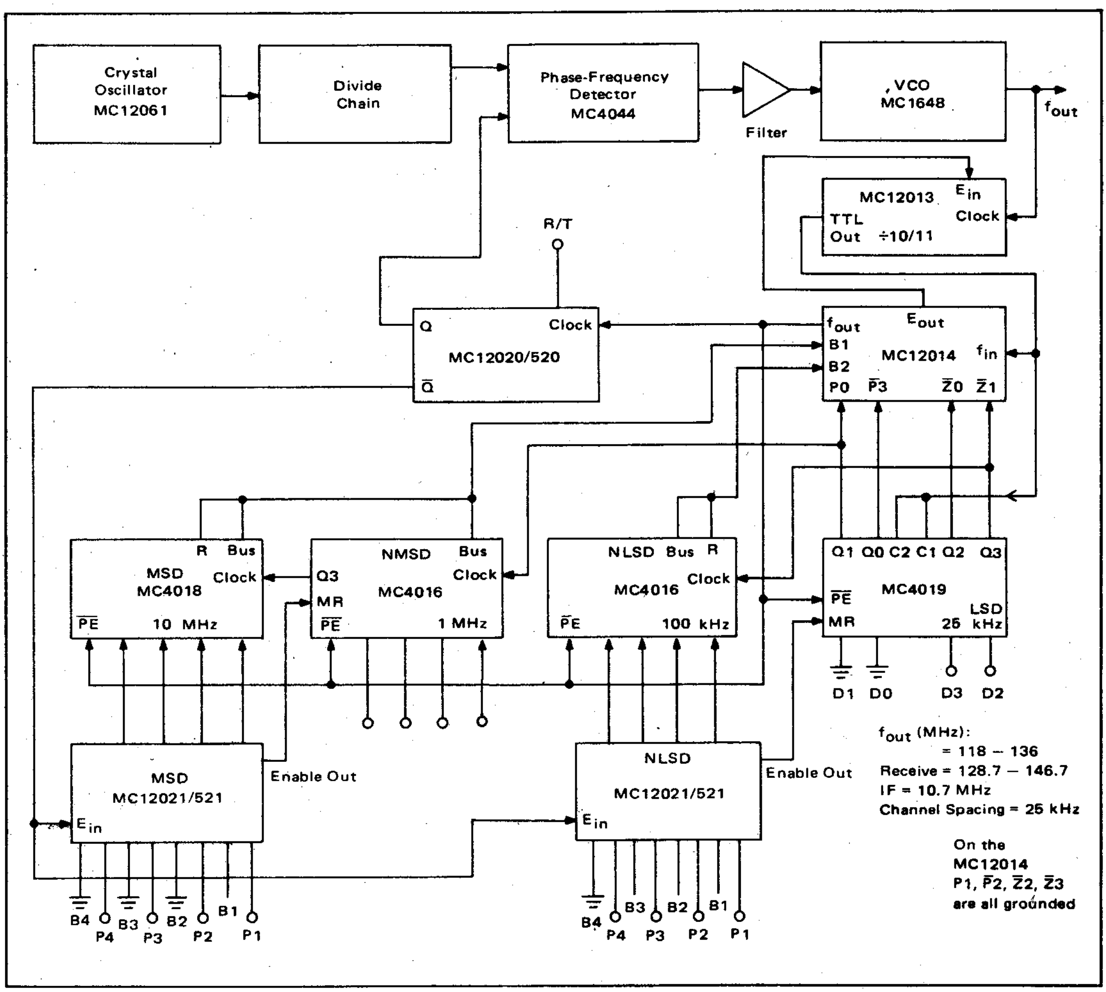


FIGURE 5 – PROGRAMMING EXAMPLES FOR SYNTHESIZER SYSTEM OF FIGURE 4

	÷Np Counter			÷A Counter	
Sample Transmit/Receive Frequency (MHz)	MSD MC4018	NMSD MC4016	÷4 P/O MC4019	NLSD MC4016	LSD P/O MC4019
118.000	11	8	4	0	0
.025	11	↓	↓	0	1
.050	11	↓	↓	0	2
.075	11	↓	↓	0	3
.100	11	↓	↓	1	0
.125	11	↓	↓	1	1
.150	11	↓	↓	1	2
.175	11	↓	↓	1	3
.200	11	↓	↓	2	0
↓	↓	↓	↓	↓	↓
119.000	11	9	↓	0	0
↓	↓	↓	↓	↓	↓
120.175	12	0	↓	1	3
↓	↓	↓	↓	↓	↓
128.000	12	8	↓	0	0
↓	↓	↓	↓	↓	↓
136.000	13	6	↓	10	10

NOTE: Columns below counters indicate the number to be programmed into that respective counter. For direct frequency, read out the four programming switches as viewed from the front panel, display the same column numbers, except for the LSD switch. The LSD switch displays 00, 25, 50, and 75 when programmed for 0, 1, 2, and 3 respectively.

to add the IF offset for the receive mode as described previously. Programming details for the balance of the counting system are as follows:

The MC4019 contains two modulo four counters. One of these forms the LSD section of the ÷A counter and is programmed by D2 and D3 to divide by 0, 1, 2, or 3. The second modulo four counter acts as a fixed divide by four and forms the LSD counter for the ÷Np counter (see MC12012 data sheet for a discussion of ÷A and ÷Np counters in conjunction with two modulus prescaling). The NLSD counter makes up the rest of the ÷A counter and provides for 100 kHz frequency increments. The rest of the ÷Np counter is formed by the NMSD and MSD counters which provide for 1 MHz and 10 MHz steps respectively.

Direct frequency readout is easily achieved as shown by the example frequencies in Figure 5. Note that a four section selector can be used to generate the necessary programming.

The dual presetting method offers an efficient and economical solution to the problem of IF offsetting, and the MC12020 and MC12021 make implementation straightforward.

Circuit diagrams utilizing Motorola products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.