MC1345P

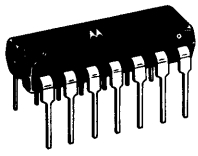
TV SIGNAL PROCESSOR

. . . a monolithic TV circuit with sync separator, advanced noise inversion, AGC comparator, and versatile RF AGC delay amplifier for use in color or monochrome TV receivers.

- Video Internally Delayed for Total Noise Inversion
- Low Impedance, Noise Cancelled Sync Output
- Refined AGC Gate
- Small IF AGC Output Change During RF AGC Interval
- Positive and Negative Going RF AGC Outputs
- Noise Threshold May Be Externally Adjusted
- Time Constants for Sync Separator Externally Chosen
- Stabilized for ±10% Supply Variations

TV SIGNAL PROCESSOR

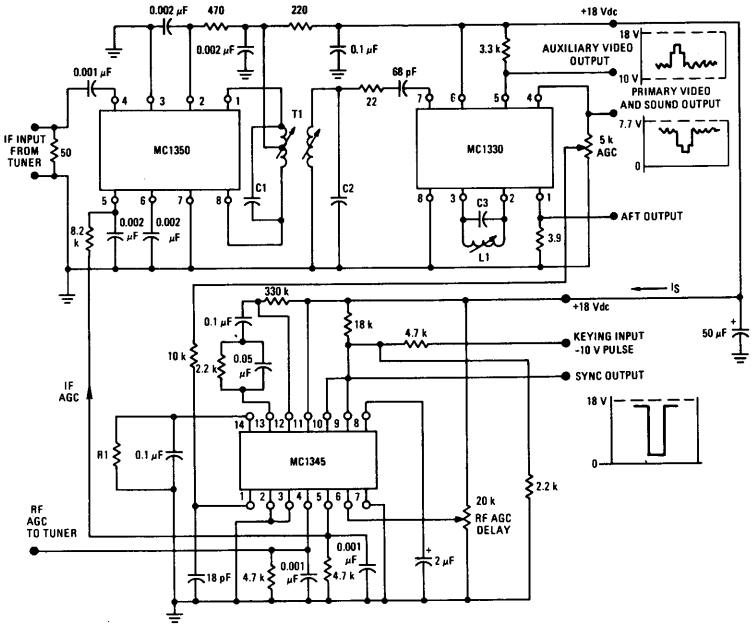
MONOLITHIC SILICON INTEGRATED CIRCUIT

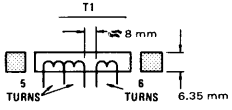


PLASTIC PACKAGE
CASE 646

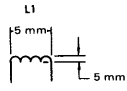
TO-116

FIGURE 1 – TYPICAL MC1345 APPLICATION WITH VIDEO IF AMPLIFIER





All windings #30 AWG tinned nylon acetate wire tuned with high permeability cores. Complete transformer is available from Coilcraft, Type R4786.



L1 wound with #26 AWG tinned nylon acetate wire tuned by distorting winding.

	39 MHz	45 MHz	58 MHz
C1	24 pF	15 pF	10 pF
C2	18 pF	12 pF	10 pF
C3	33 pF	33 pF	18 pF
L1	12 Turns	10 Turns	
R1	See Operating Characteristics, "Noise Inverter" section.		

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Value	Unit
Power Supply Voltage (Pin 11)	+22	Vdc
Video Input Voltage (Pin 1)	+10	Vdc
Negative RF AGC Supply Voltage (Pin 3)	-10	Vdc
Gating Voltage (Pin 9)	15	V_{p-p}
Sync Separator Drive Voltage (Pin 12)	7.0	V_{p-p}
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	0 to +70	°C
Storage Temperature Range	-55 to +150	°C

Maximum Ratings as defined in MIL-S-19500, Appendix A.

ELECTRICAL CHARACTERISTICS (V^+ = +18 Vdc, T_A = +25°C unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Sync Tip dc Level of Input Signal	3.6	3.9	4.2	Vdc
Temperature Coefficient of Sync Tip (Input)	–	–	1.0	mV/°C
Sync Output Amplitude	–	16	–	V_{p-p}
Sync Output Impedance	–	–	100	Ohms
Sync Tip to Noise Threshold Separation (Input)	0.45	0.7	0.95	Vdc
IF AGC Voltage Change During RF Interval	–	0.10	0.5	Vdc
Peak AGC Charge Current	–	15	–	mAdc
Peak AGC Discharge Current	–	0.9	–	mAdc
IF AGC Voltage Range (See Figures 2 and 3)	9.0	–	–	Vdc
Positive RF AGC Voltage Range	–	10	–	Vdc
Positive RF AGC Minimum Voltage	0.5	1.5	2.0	Vdc
Negative RF AGC Voltage Range	–	10	–	Vdc
Negative RF AGC Maximum Voltage	9.5	10.5	11.5	Vdc
Total Supply Current, I_S (Circuit of Figure 1)	–	26	–	mAdc

FIGURE 2 – TEST CIRCUIT FOR AGC AMPLIFIER MEASUREMENTS

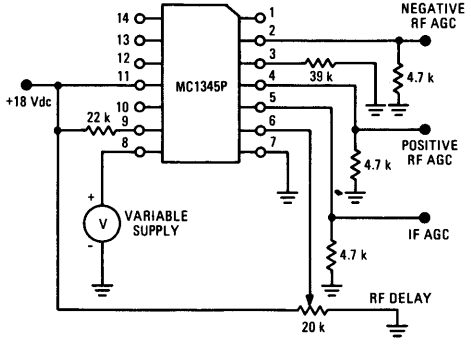


FIGURE 3 – AGC AMPLIFIER RESPONSE

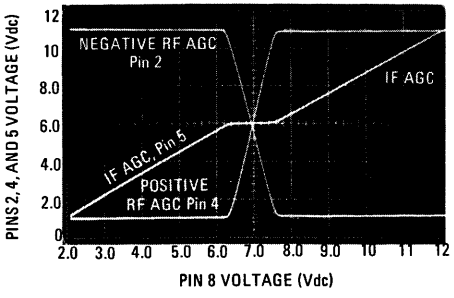
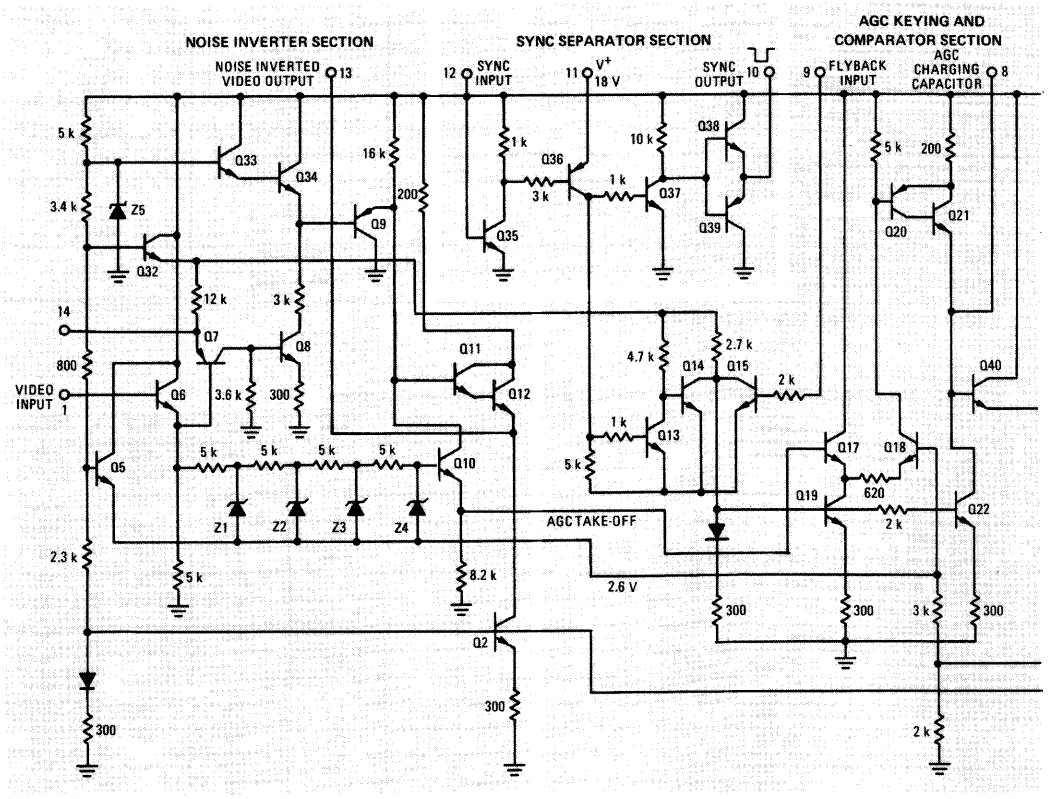


FIGURE 4 – CIRCUIT SCHEMATIC



OPERATING CHARACTERISTICS

NOISE INVERTER

A composite video signal of from 1 to 3 volts peak-to-peak amplitude with negative-going sync, superimposed on a positive dc offset voltage, is required at the input, pin 1. The amplitude of the dc offset voltage will determine the allowable magnitude of the video input, since the sync tip will always be clamped at 3.9 V. See Figure 5.

The noise threshold is set by Q7's emitter voltage determined by Q32 and the bias-chain Zener diode. The resulting dc level (or noise threshold) may be lowered by adding an external resistor, R1 (Figure 1), connected from pin 14 to ground. With this arrangement, the lowered threshold would be given by:

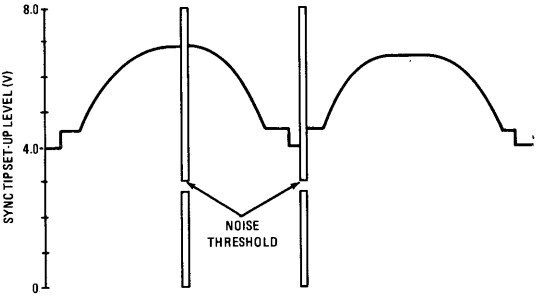
$$V = \frac{R1\ V_n}{R1 + 12{,}000\ \Omega}$$

where V_n = noise threshold without R1 connected.

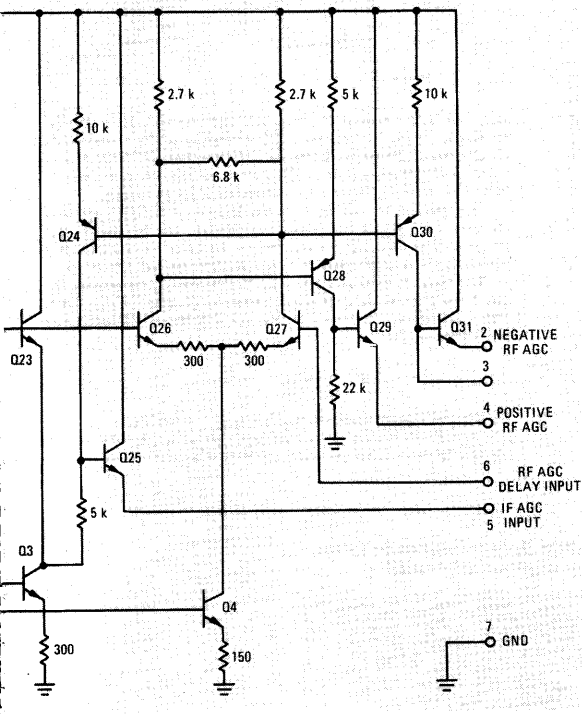
The noise threshold can also be raised to the same degree by connecting R1 from pin 14 to the supply voltage level. However, in this case, care should be exercised to insure that the resulting voltage appearing at pin 14 does not exceed the sync threshold (approximately 3.9 V).

Noise inversion is achieved as follows: first the composite input signal is impedance-buffered by the Q6 emitter-follower. Then,

FIGURE 5



IF AND RF AGC AMPLIFIER AND DELAY SECTION



the buffered signal is fed to Q10's base through an RC delay line (Z1 – Z4). Finally the signal appears, inverted and delayed by approximately 300 ns, at the base of Q11.

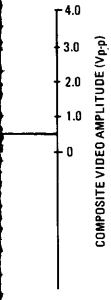
If an interference pulse occurs, with an amplitude enough above the sync tip level to reach the noise threshold, the pulse will drive the emitter of Q6 below its pre-set level. Q7 will conduct, and charge from the external capacitor connected to pin 14 will pass through Q7, turning on both Q8 and Q9. When Q9 is on, Q11's base is grounded, blanking the output of Q10's collector.

The video signal with the interfering noise cancelled, emerges at pin 13. Polarity is inverted, so the sync pulses are positive-going.

Blanking commences before the interference pulse itself emerges from the delay line, and the blanking action persists for a short time interval after the end of the noise pulse, due to energy stored in Q9's junction.

For very long noise pulses, the rate of discharge of the external capacitor sets the end of the blanking interval. In such a case, blanking could extend over several horizontal line-sweep periods, depending on the capacitor value used. The external capacitor is typically 0.1 μF, and this value allows continuous cancellation for approximately 4 line-sweep intervals.

Under weak signal conditions, high frequency noise from thermal or tropospheric sources is common. To prevent this type of interference from spuriously triggering the inverter, some RC filtering is required between the video detector and the video input at pin 1. For this filter, RC values of 10 kΩ and 18 pF are typical.



SYNC SEPARATOR

The noise-inverted video output at pin 13 is passed through an external RC filter network, to the sync separator input at pin 12, cutting off Q35, Q36, and Q37, except during the positive sync tips. Time constants for the filter are a matter of the designer's preference, and are chosen as for discrete-circuit sync separators.

Operation of the sync separator is as follows. Q35 conducts only during the positive-going sync pulse. Q36 amplifies and inverts the sync pulse, driving Q37 into saturation during the sync pulse interval. The output of Q37 drives the complementary pair, Q38/Q39, which yield a low output impedance negative-going sync pulse of greater than 15 V peak-to-peak amplitude. It should be noted that the first sync pulse occurring after noise inversion ends, will be slightly longer in duration than other sync pulses. Typical resistance and capacitance values for the RC sync input network are given in Figure 6A.

FIGURE 6A – NORMAL SYNC SEPARATION NETWORK

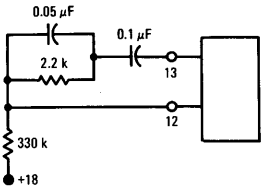
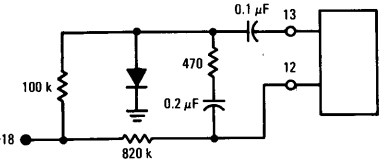


FIGURE 6B – ALTERNATE DIODE SYNC SEPARATION NETWORK



An alternate input network is shown in Figure 6B, it uses a diode to separate the sync pulses. In this case the pulses will be clamped to +0.7 V above ground. As a result, Q35 and the transistors following it serve as over-driven amplifiers.

KEYER AND COMPARATOR

The AGC system is internally connected to the video input at Q10's emitter. The sync signal at Q36 is internally connected to the AGC sync keyer which consists of Q13 and Q14. An externally-derived negative-going flyback pulse (≃ 12 V peak-to-peak) is applied to Q15 for flyback keying the AGC. Since the detected video output level is sampled only when the sync pulse and the flyback pulse are coincident, true keyed AGC action occurs.

An AGC comparator is formed by Q17 and Q18. The base of Q18 is connected to a fixed reference of 2.6 V. The base of Q17 is connected to the emitter of Q10, where the video signal has negative-going sync pulses. The emitters of both devices are supplied

from a gated current source, Q19. This current source conducts only when Q14 and Q15 are simultaneously switched off. To do this, a positive sync pulse is required on the base of Q13, coincident with a negative flyback pulse on the base of Q15 (pin 9).

If the video signal at the emitter of Q10 increases in amplitude, the sync pulse becomes more negative. Thus, when Q19 is gated on, Q18 conducts and turns on both Q20 and Q21, which charge the external AGC filter capacitor connected at pin 8. A typical value for this capacitor is 2.0 μF.

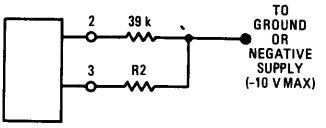
If the video signal decreases, Q18 will not conduct. However, Q22 will conduct and permit a current of 0.9 mA to flow out of the capacitor at pin 8. In effect, this "charge dumping" through Q22 promotes faster AGC action than could be attained with a conventional "charge only" system. Coupling between the charging capacitor and the AGC amplifier is through an emitter follower, Q40.

The MC1345 will operate without flyback pulses if pin 9 is grounded. However, the AGC noise immunity and aircraft flutter rejection will be impaired.

THE AGC AMPLIFIER

AGC for the IF is supplied by the emitter of Q25. The RF AGC is generated in the following way: Given a weak signal condition, Q26 is barely conducting, while Q27 passes the bulk of the current flowing from the current source, Q4. Assume that the base of Q27 is biased "on" by the RF AGC delay control connected to pin 6. The IF AGC will increase if the AGC input voltage from Q40 increases. When this latter voltage increases to a predetermined level (set by the delay control), Q26 turns on. Then, when Q26 turns on, Q27 turns off, which also turns Q24 off. As Q24 turns off, it will cancel any further increases at the base of Q25, which would come from Q23 through the 5.0 kΩ resistor. The result is that the IF AGC level is held constant during the RF AGC excursion. As Q26 is now conducting, Q28 and Q29 will also be turned on supplying the forward RF AGC voltage to pin 4. Then, when the RF AGC voltage excursion is complete, Q24 will have reached cutoff and will be unable to oppose the voltage rise at the base of Q25, thus allowing the IF AGC voltage to begin increasing.

FIGURE 7 – ALTERNATE RF AGC OUTPUT FOR FET OR TUBE TUNER



The negative RF AGC action is similar, except that Q30 and Q31 are turned off as Q28 and Q29 are turned on. The RF AGC delay, or turn-off of Q27, can be adjusted by the delay control so that it occurs at any selected point in the IF AGC range (see Figure 3).

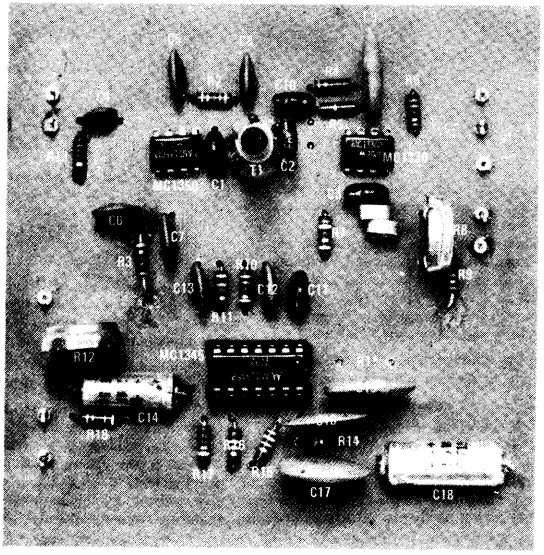
The negative AGC swing may be level-shifted by connecting the pin 2 and pin 3 resistors to a negative supply instead of to ground. The value of the pin 3 resistor, R2, for a given voltage swing, can be determined as:

$$R2 = \frac{V}{25{,}000}$$

(See Figure 7 for component connections for negative AGC.)

All external component values given are only suggested values; the final choices will depend on the designer's preferences.

FIGURE 8 –PRINTED CIRCUIT BOARD COMPONENT LAYOUT OF IF AND JUNGLE CIRCUIT OF FIGURE 1



C1 See chart of Figure 1
C2 See chart of Figure 1
C3 See chart of Figure 1
C4 0.001 μF
C5 0.002 μF
C6 0.002 μF
C7 0.002 μF
C8 0.002 μF
C9 0.1 μF
C10 68 pF
C11 18 pF
C12 0.001 μF
C13 0.001 μF
C14 2 μF/10 V
C15 0.1 μF
C16 0.05 μF
C17 0.1 μF
C18 50 μF/25 V
L1 See Figure 1
T1 See Figure 1

R1 See Operating Characteristics discussion, Noise Inverter section
R2 470 ohms
R3 8200 ohms
R4 220 ohms
R5 22 ohms
R6 3300 ohms
R7 3900 ohms
R8 5 kilohm potentiometer
R9 10 kilohms
R10 4700 ohms
R11 4700 ohms
R12 2 kilohm potentiometer
R13 50 ohms
R14 2200 ohms
R15 330 kilohms
R16 18 kilohms
R17 2200 ohms
R18 4700 ohms

*See Noise Inverter Section (part can be omitted).