# MC1697

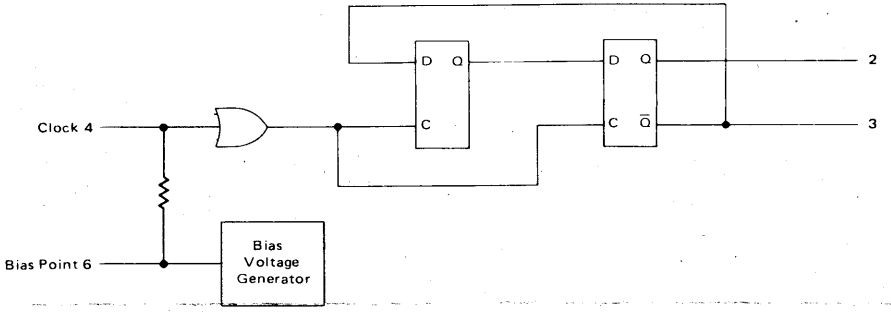
## 1-GHz DIVIDE-BY-FOUR PRESCALER

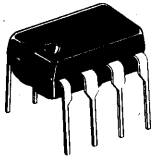
The MC1697 is a divide-by-four gigahertz prescaler in an 8 pin plastic package. The clock input requires an ac coupled driving signal of 800 mV amplitude (typical). The clock toggles two divide-by-two stages, and the complementary outputs (50% duty cycle) are taken from the second stage. The complementary outputs are capable of driving 50-ohm lines.

Pin 6 is available for connection of a decoupling capacitor to ground. This capacitor stabilizes the reference point which is internally coupled to the clock input.

$V_{CC1}$ = Pin 1
$V_{CC2}$ = Pin 8
$V_{EE}$ = Pin 5

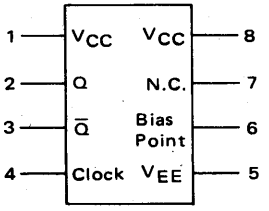
Power Dissipation = 320 mW Typ/Pkg
(No Load – 7.0 V Supply)



**P SUFFIX**
PLASTIC PACKAGE
CASE 626

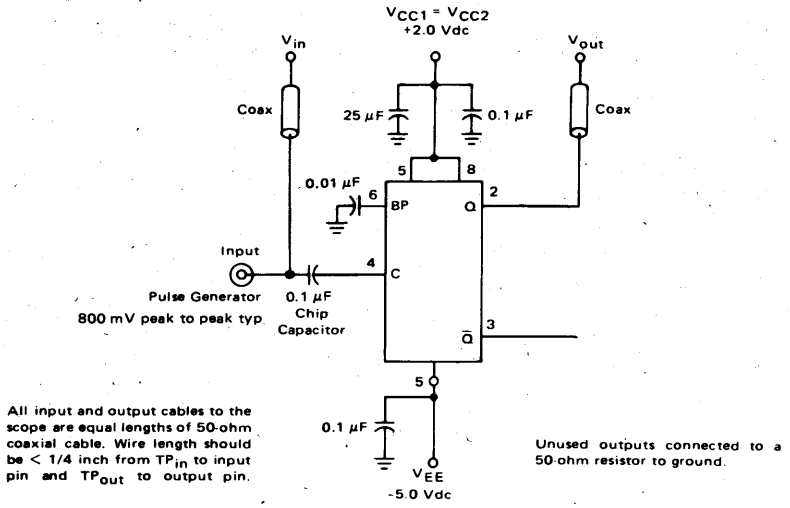
**PIN ASSIGNMENT**



## ELECTRICAL CHARACTERISTICS

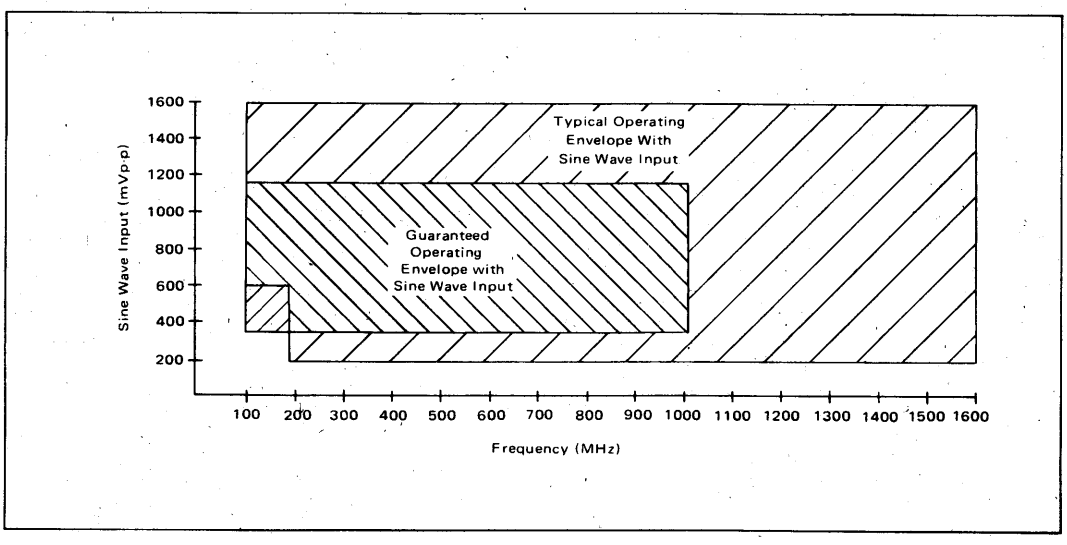
| Characteristic | Symbol | MC1697P Test Limits | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | 0°C | | +25°C | | +75°C | | |
| | | Min | Max | Min | Max | Min | Max | |
| Power Supply Drain Current | $I_E$ | – | – | – | 57 | – | – | mAdc |
| Toggle Frequency (high frequency operation) | $f_{Tog}$ | 1.0 | – | 1.0 | – | 1.0 | – | GHz |
| Toggle Frequency (low frequency sine wave input) | $f_{Tog}$ | – | – | – | 100 | – | – | MHz |

### COUNT FREQUENCY TEST CIRCUIT




Note: All power supply and logic levels are shown shifted 2 volts positive.

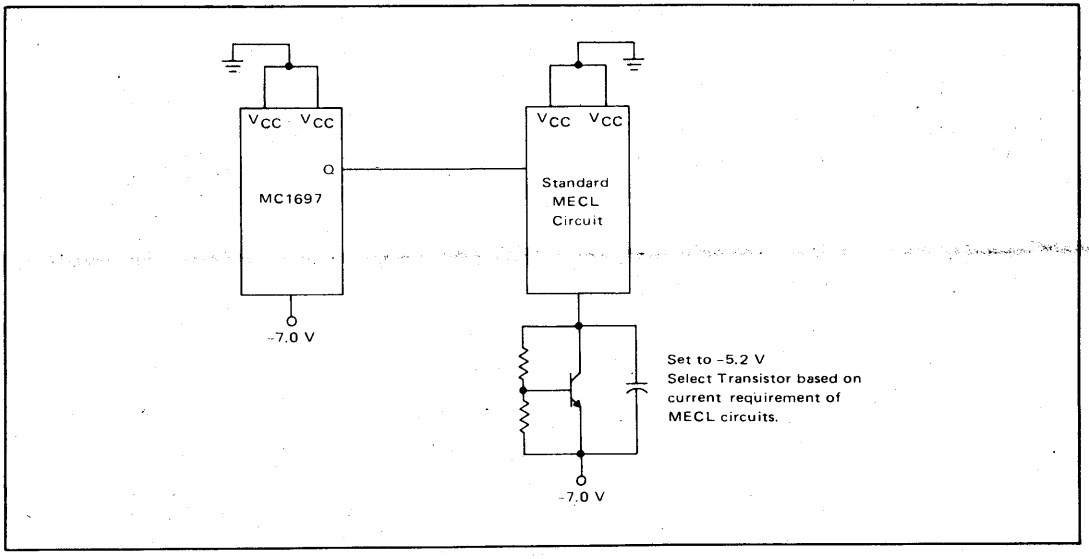
### TIMING DIAGRAM



## APPLICATION INFORMATION

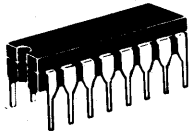
The MC1697 is a very high speed divide-by-four prescaler designed to operate on a nominal supply voltage of -7.0 volt. In some applications it may be necessary to interface the output of the MC1697 with other MECL circuits requiring a supply voltage of -5.2 volts. One method of interfacing the circuits is shown below. This configuration is adequate for frequencies up to 1 GHz over the temperature range of $0^{o}$ to $+75^{o}C$. For best performance it is recommended that separate regulated supplies be used.

**METHOD OF INTERFACING MC1697 WITH STANDARD MECL CIRCUITS**

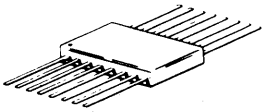


# MC1699

## DIVIDE-BY-FOUR GIGAHERTZ COUNTER



**L SUFFIX**
CERAMIC PACKAGE
CASE 620

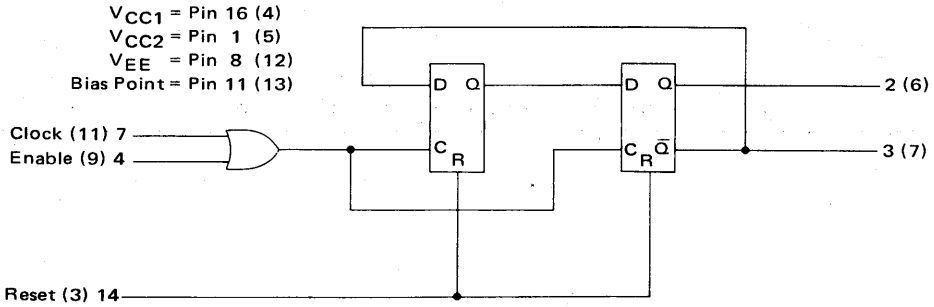


**F SUFFIX**
CERAMIC PACKAGE
CASE 650

The MC1699 is a divide-by-four gigahertz counter. The clock input requires an ac coupled driving signal of 800 mV amplitude (typical). The clock toggles two divide-by-two stages, and the complementary outputs (50% duty cycle) are taken from the second stage.

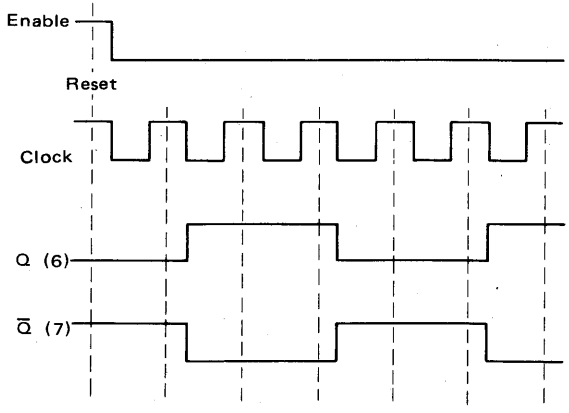
The MC1699 includes clock enable and reset. The reset is compatible with MECL III voltage levels. The enable input requires a $V_{IL}$ of -2.0 V max. Reset operates only when either the clock or the enable is high.

Pin 11 (13) is available for connection of a decoupling capacitor to ground. This capacitor stabilizes the reference point which is internally coupled to the clock input.




Number at end of terminal denotes pin number for L package (Case 620).
Number in parenthesis denotes pin number for F package (Case 650).

### TIMING DIAGRAM

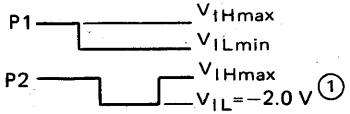


## ELECTRICAL CHARACTERISTICS

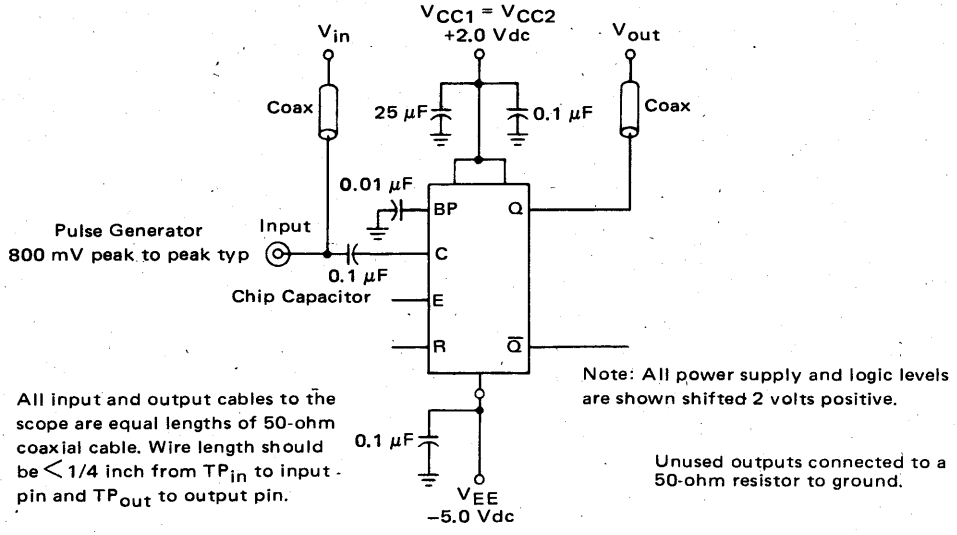
| Characteristic | Symbol | -30°C | | +25°C | | +85°C | | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Power Supply Drain Current | $I_E$ | – | – | – | 57 | – | – | mAdc | All inputs and outputs open except Clock = $V_{IHC} \cong$ -4.0 Vdc |
| Input Current | $I_{inH}$ | | | | | | | μAdc | $V_{IHmax}$ to Reset, $V_{IL}$ to Enable, $V_{EE}$ to Clock. $V_{ILmin}$ to reset, $V_{IHmax}$ to Enable, $V_{EE}$ to Clock. |
| Reset | | – | – | – | 500 | – | – | | |
| Enable | | – | – | – | 265 | – | – | | |
| Logic "1" Output Voltage | $V_{OH}$ | -1.085 | -0.875 | -1.000 | -0.810 | -0.930 | -0.700 | Vdc | See Note ②. Or, apply P1 to Reset and $V_{IHmax}$ to Enable |
| Logic "0" Output Voltage | $V_{OL}$ | – | -1.630 | – | -1.600 | – | -1.555 | Vdc | |
| Toggle Frequency (high frequency operation) | $f_{Tog}$ | 1.0 | – | 1.0 | – | 1.0 | – | GHz | $V_{IL}$ ① to Enable. See Test Circuit and Application Information on next page. |
| Toggle Frequency (low frequency sine wave input) | $f_{Tog}$ | – | – | – | 100 | – | – | MHz | |

① Enable input requires $V_{IL}$ = -2.0 V max.

② Reset counter by applying pulse P1 to pin 14, then toggle outputs by applying pulse P2 to pin 4 for 2 cycles. Hold power during pulse sequence. Hold clock input @ $V_{EE}$.



## TOGGLE FREQUENCY TEST CIRCUIT




## APPLICATION INFORMATION

The MC1699 is a very high speed divide-by-four counter intended for prescaler applications. The reset provides increased flexibility for counter and time measuring requirements.

The clock input is designed to accept a capacitor-coupled sine wave signal for frequencies above 100 MHz. Below 100 MHz waveshaping is recommended to obtain good MECL III or MECL 10,000 edge speeds.

With a continuous input signal the clock can be capacitor-coupled with no problems. However, if the clock is interrupted and the clock input floats to the bias point reference voltage, the counter may oscillate. To prevent this oscillation, an external resistor can be added as shown in Figure 1. This resistor is recommended only when the clock is interrupted and serves no useful function with a continuous signal. Also, this external resistor is not required when the enable input is used to gate the clock signal.

### FIGURE 1