

### FEATURES

- Fast Settling Time ..... 1  $\mu$ s to 0.1% Max
- High Slew Rate ..... 12V/ $\mu$ s Min
- Power Bandwidth ..... 150kHz Min
- Low Power Consumption ..... 90mW Max
- Excellent DC Specifications
- Internally Compensated
- Ideal DAC Output Amplifier
- MIL-STD-883 Processing Available
- Fits Standard 741 Sockets
- Low Cost
- Available in Die Form

and excellent DC input characteristics. An internal feed-forward frequency compensation network provides simplicity of application — no external capacitors are required for stable, high-speed performance. The fast output response is achieved without sacrifice of input bias current or power consumption. A 250kHz typical power bandwidth is attained with a small-signal bandwidth of only 2.5MHz, thus board layout is non-critical. The OP-01 is completely protected at both input and output, fits standard 741 sockets, and is offset nulled with a 10k $\Omega$  potentiometer.

The fast output response combined with excellent settling time makes the OP-01 ideal for use as a D/A converter output amplifier.

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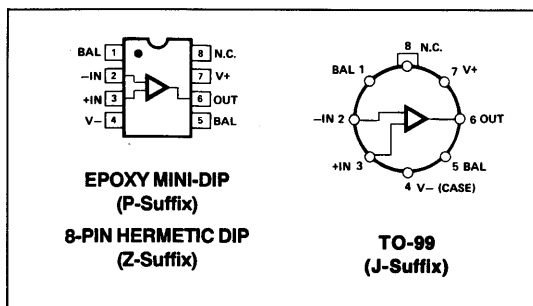
### ORDERING INFORMATION †

| T <sub>A</sub> = 25°C<br>V <sub>OS</sub> MAX<br>(mV) | PACKAGE |                 |                  | OPERATING<br>TEMPERATURE<br>RANGE |
|--|---------|-----------------|------------------|-----------------------------------|
|  | TO-99   | CERDIP<br>8-PIN | PLASTIC<br>8-PIN |                                   |
| 0.7  | OP01J*  | —               | —                | MIL                               |
| 0.7  | —       | —               | OP01HP           | COM                               |
| 5.0  | OP01GJ  | —               | —                | MIL                               |
| 5.0  | OP01CJ  | OP01CZ          | OP01CP           | COM                               |

\* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

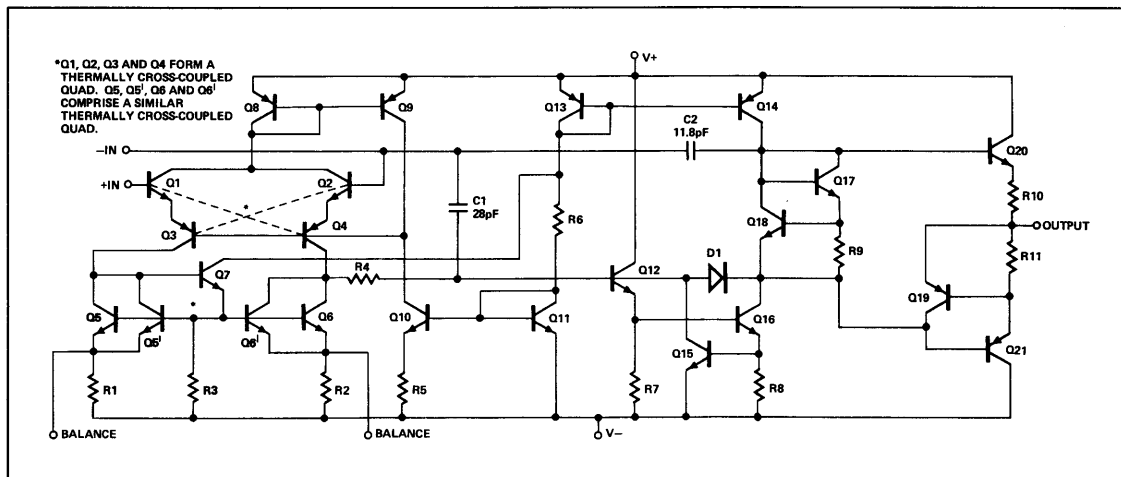
### PIN CONNECTIONS



### GENERAL DESCRIPTION

The OP-01 series of monolithic inverting high-speed operational amplifiers combines high slew rate, fast settling time

### SIMPLIFIED SCHEMATIC



# OP-01

## ABSOLUTE MAXIMUM RATINGS (Note 1)

|  |                 |
|--|-----------------|
| Total Supply Voltage, OP-01, OP-01H, OP-01N, OP-01NT,<br>OP-01G, OP-01GT ..... | ±22V            |
| OP-01G, OP-01C, OP-01GR .....  | ±20V            |
| Differential Input Voltage .....   | ±30V            |
| Input Voltage (Note 2) .....   | ±15V            |
| Short-Circuit Duration .....   | Indefinite      |
| Operating Temperature Range  |                 |
| OP-01, OP-01G .....  | -5°C to +125°C  |
| OP-01H, OP-01C .....   | 0°C to +70°C    |
| Junction Temperature ( $T_j$ ) .....   | -65°C to +150°C |
| Storage Temperature  |                 |
| J and Z Packages .....   | -65°C to +150°C |
| P Packages .....   | -65°C to +150°C |

Lead Temperature (Soldering, 60 sec) ..... +300°C

| PACKAGE TYPE           | $\theta_{JA}$ (NOTE 3) | $\theta_{JC}$ | UNITS |
|------------------------|------------------------|---------------|-------|
| TO-99 (J)              | 170                    | 24            | °C/W  |
| 8-Pin Hermetic DIP (Z) | 162                    | 26            | °C/W  |
| 8-Pin Plastic DIP (P)  | 110                    | 50            | °C/W  |

### NOTES:

- Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
- For supply voltages less than ±15V, the maximum input voltage is the supply voltage.
- $\theta_{JA}$  is specified for worst case mounting conditions, i.e.,  $\theta_{JA}$  is specified for device in socket for TO, CerDIP and P-DIP packages.

## ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ , $T_A = 25^\circ C$ , unless otherwise noted.

| PARAMETER  | SYMBOL   | CONDITIONS  | OP-01<br>OP-01H |       |     | OP-01G<br>OP-01C |       |     | UNITS      |
|--|----------|---|-----------------|-------|-----|------------------|-------|-----|------------|
|  |          |   | MIN             | TYP   | MAX | MIN              | TYP   | MAX |            |
| Input Offset Voltage                             | $V_{OS}$ | $R_S \leq 20k\Omega$                                | —               | 0.3   | 0.7 | —                | 2.0   | 5.0 | mV         |
| Input Offset Current                             | $I_{OS}$ |   | —               | 0.5   | 2.0 | —                | 2.0   | 20  | nA         |
| Input Bias Current                               | $I_B$    |   | —               | 18    | 30  | —                | 25    | 100 | nA         |
| Input Voltage Range                              | IVR      |   | ±12             | ±13   | —   | ±12              | ±13   | —   | V          |
| Common-Mode<br>Rejection Ratio                   | CMRR     | $V_{CM} = \pm 10V$<br>$R_S \leq 20k\Omega$          | 85              | 110   | —   | 80               | 100   | —   | dB         |
| Power Supply<br>Rejection Ratio                  | PSRR     | $V_S = \pm 5V$ to $\pm 20V$<br>$R_S \leq 20k\Omega$ | —               | 10    | 60  | —                | 100   | 150 | $\mu V/V$  |
| Output Voltage Swing                             | $V_O$    | $R_L \geq 5k\Omega$<br>$R_L \geq 2k\Omega$          | ±12.5           | ±13.5 | —   | ±12.5            | ±13.5 | —   | V          |
| Large-Signal<br>Voltage Gain                     | $A_{VO}$ | $R_L \geq 2k\Omega$<br>$V_O = \pm 10V$              | 50              | 100   | —   | 25               | 75    | —   | V/mV       |
| Power Consumption                                | $P_d$    | $V_{OUT} = 0$                                       | —               | 50    | 90  | —                | 50    | 90  | mW         |
| Settling Time<br>to 0.1% (Summing<br>Node Error) | $t_s$    | $A_V = -1$<br>(Notes 1, 2)<br>$V_{IN} = 5V$         | —               | 0.7   | 1.0 | —                | 0.7   | 1.0 | $\mu s$    |
| Slew Rate<br>(Notes 2, 3)                        | SR       | $A_V = -1$ ,<br>$R_S = 3k$ to $5k\Omega$            | 12              | 18    | —   | 12               | 18    | —   | V/ $\mu s$ |
| Large-Signal<br>Bandwidth<br>(Notes 3, 4)        |          |   | 150             | 250   | —   | 150              | 250   | —   | kHz        |
| Small-Signal<br>Bandwidth<br>(Notes 3, 4)        |          |   | 1.5             | 2.5   | —   | 1.5              | 2.5   | —   | MHz        |
| Risetime   | $t_r$    | $A_V = -1$<br>$V_{IN} = 50mV$                       | —               | 150   | —   | —                | 150   | —   | ns         |
| Overshoot  | OS       |   | —               | 2     | —   | —                | 2     | —   | %          |

### NOTES:

- $R_L = 25k\Omega$ ;  $C_L = 50pF$ . See Settling Time Test Circuit.
- Sample tested.
- See applications information.
- Guaranteed by design.

**ELECTRICAL CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $-55^\circ C \leq T_A \leq +125^\circ C$  for OP-01, OP-01G and  $0^\circ C \leq T_A \leq +70^\circ C$  for OP-01H, OP-01C, unless otherwise noted.

| PARAMETER                     | SYMBOL     | CONDITIONS  | OP-01<br>OP-01H          |                          |     | OP-01G<br>OP-01C         |                          |     | UNITS            |
|-------------------------------|------------|---|--------------------------|--------------------------|-----|--------------------------|--------------------------|-----|------------------|
|                               |            |   | MIN                      | TYP                      | MAX | MIN                      | TYP                      | MAX |                  |
| Input Offset Voltage          | $V_{OS}$   | $R_S \leq 20k\Omega$                                | —                        | 0.4                      | 1.0 | —                        | 3.0                      | 6.0 | mV               |
| Input Offset Current          | $I_{OS}$   |   | —                        | 1                        | 4   | —                        | 4                        | 40  | nA               |
| Input Bias Current            | $I_B$      |   | —                        | 30                       | 50  | —                        | 50                       | 200 | nA               |
| Input Voltage Range           | IVR        |   | $\pm 10$                 | $\pm 13$                 | —   | $\pm 10$                 | $\pm 13$                 | —   | V                |
| Common-Mode Rejection Ratio   | CMRR       | $V_{CM} = \pm 10V$<br>$R_S \leq 20k\Omega$          | 85                       | 110                      | —   | 80                       | 100                      | —   | dB               |
| Power Supply Rejection Ratio  | PSRR       | $V_S = \pm 5V$ to $\pm 20V$<br>$R_S \leq 20k\Omega$ | —                        | 10                       | 60  | —                        | 100                      | 150 | $\mu V/V$        |
| Large-Signal Voltage Gain     | $A_{VO}$   | $R_L \geq 2k\Omega$<br>$V_O = \pm 10V$              | 30                       | 60                       | —   | 15                       | 50                       | —   | V/mV             |
| Output Voltage Swing          | $V_O$      | $R_L \geq 5k\Omega$<br>$R_L \geq 2k\Omega$          | $\pm 12.5$<br>$\pm 12.0$ | $\pm 13.5$<br>$\pm 13.0$ | —   | $\pm 12.5$<br>$\pm 12.0$ | $\pm 13.5$<br>$\pm 13.0$ | —   | V                |
| Offset Voltage Drift (Note 1) | $TCV_{OS}$ | $R_S \leq 5k\Omega$                                 | —                        | 2                        | 8   | —                        | 5                        | 20  | $\mu V/^\circ C$ |

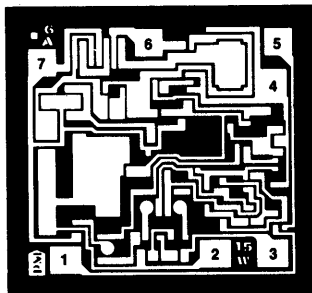
**NOTE:**

1. Sample tested.

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# OP-01

## DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



1. NULL
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V-
5. NULL
6. OUTPUT
7. V+

**DIE SIZE 0.047 × 0.043 inch, 2021 sq. mils**  
(1.19 × 1.09 mm, 1.30 sq. mm)

**WAFER TEST LIMITS** at  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$  for OP-01N, OP-01G and OP-01GR devices;  $T_A = 125^\circ C$  for OP-01NT and OP-01GT devices, unless otherwise noted.

| PARAMETER                    | SYMBOL   | CONDITIONS  | OP-01NT<br>LIMIT         | OP-01N<br>LIMIT          | OP-01GT<br>LIMIT         | OP-01G<br>LIMIT          | OP-01GR<br>LIMIT         | UNITS         |
|------------------------------|----------|---|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|---------------|
| Input Offset Voltage         | $V_{OS}$ | $R_S \leq 20k\Omega$                                | 1.0                      | 0.7                      | 3.0                      | 2.0                      | 5.0                      | mV MAX        |
| Input Offset Current         | $I_{OS}$ |   | 4                        | 2                        | 10                       | 5                        | 20                       | nA MAX        |
| Input Bias Current           | $I_B$    |   | 50                       | 30                       | 100                      | 50                       | 100                      | nA MAX        |
| Input Voltage Range          | IVR      |   | $\pm 10$                 | $\pm 12$                 | $\pm 10$                 | $\pm 12$                 | $\pm 12$                 | V MIN         |
| Common-Mode Rejection Ratio  | CMRR     | $V_{CM} = \pm 10V$<br>$R_S \leq 20k\Omega$          | 85                       | 85                       | 80                       | 80                       | 80                       | dB MIN        |
| Power Supply Rejection Ratio | PSRR     | $V_S = \pm 5V$ to $\pm 20V$<br>$R_S \leq 20k\Omega$ | 60                       | 60                       | 100                      | 100                      | 150                      | $\mu V/V$ MAX |
| Output Voltage Swing         | $V_{OM}$ | $R_L \geq 5k\Omega$<br>$R_L \geq 2k\Omega$          | $\pm 12.5$<br>$\pm 12.0$ | $\pm 12.5$<br>$\pm 12.0$ | $\pm 12.5$<br>$\pm 12.0$ | $\pm 12.5$<br>$\pm 12.0$ | $\pm 12.5$<br>$\pm 12.0$ | V MIN         |
| Large-Signal Voltage Gain    | $A_{VO}$ | $R_L \geq 2k\Omega$<br>$V_O = \pm 10V$              | 30                       | 50                       | 25                       | 50                       | 25                       | V/mV MIN      |
| Power Consumption            | $P_d$    | $V_{OUT} = 0$                                       | —                        | 90                       | —                        | 90                       | 90                       | mW MAX        |

### NOTES:

For 25°C characteristics of NT & GT devices, see N & G characteristics respectively.

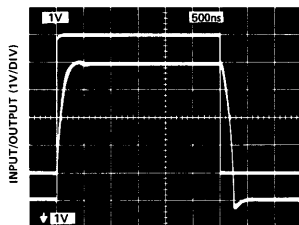
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

### TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$ , $T_A = 25^\circ C$ , unless otherwise noted.

| PARAMETER                                  | SYMBOL | CONDITIONS   | ALL GRADES<br>TYPICAL | UNITS      |
|--|--------|--|-----------------------|------------|
| Slew Rate                                  | SR     | $A_{VCL} = -1$ , $R_S = 3k\Omega$ to $5k\Omega$  | 18                    | V/ $\mu s$ |
| Settling Time to 0.1% (Summing Node Error) | $t_S$  | $V_{IN} = 5V$<br>$A_V = -1$<br>$R_L = 2k\Omega$ (See Settling Time Test Circuit)<br>$C_L = 50pF$ | 1.0                   | $\mu s$    |
| Large-Signal Bandwidth                     |        |  | 250                   | kHz        |
| Small-Signal Bandwidth                     |        |  | 2.5                   | MHz        |
| Risetime                                   | $t_r$  | $V_{IN} = 50mV$<br>$A_V = -1$  | 150                   | ns         |

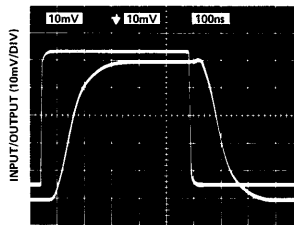
TYPICAL PERFORMANCE CHARACTERISTICS

LARGE-SIGNAL PULSE RESPONSE



$V_S = \pm 15V, A_V = -1, R_L = 2k\Omega, C_L = 50pF$

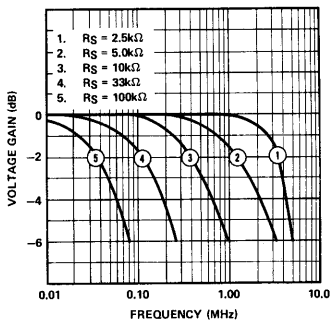
SMALL-SIGNAL PULSE RESPONSE



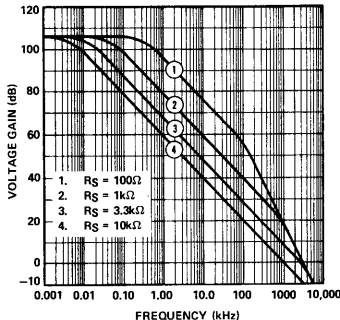
$V_S = \pm 15V, A_V = -1, R_L = 2k\Omega, C_L = 50pF$

2

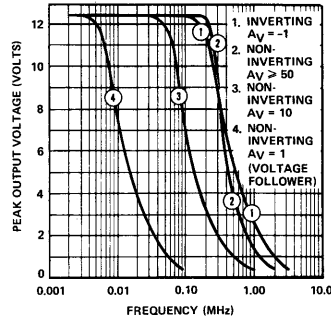
UNITY-GAIN BANDWIDTH vs SOURCE RESISTANCE



OPEN-LOOP GAIN vs FREQUENCY



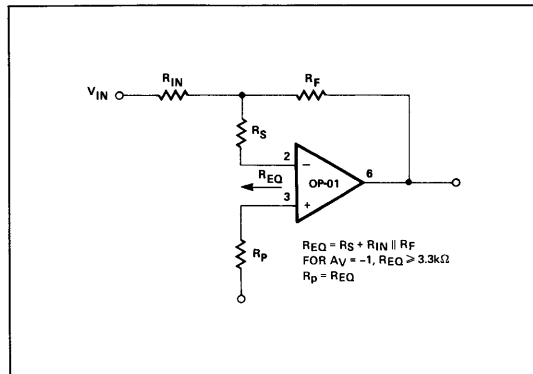
LARGE-SIGNAL OUTPUT SWING vs FREQUENCY



APPLICATIONS INFORMATION

The OP-01 incorporates an internal feed-forward compensation network to provide fast slewing and settling times in all inverting and moderate-to-high-gain noninverting applications. Unity-gain bandwidth is a function of the total equivalent source resistance seen by the inverting terminal. Proper choice of this resistance will allow the user to maximize bandwidth while assuring proper stability. The equivalent-inverting-terminal-resistance is defined as  $R_{IN} \parallel R_F$ , and it must be greater than  $3.3k\Omega$  to assure stability in all closed-loop gain configurations including unity gain. Should  $R_{IN} \parallel R_F \leq 3.3k\Omega$ , a resistor ( $R_S$ ) may be placed between the inverting input and the sum node to provide the required resistance. (See Fast Inverting Amplifier Diagram.) Lower values of total equivalent resistance may be used to improve bandwidth in higher closed-loop gain configurations, as indicated by the Open-Loop Gain vs. Frequency plot.

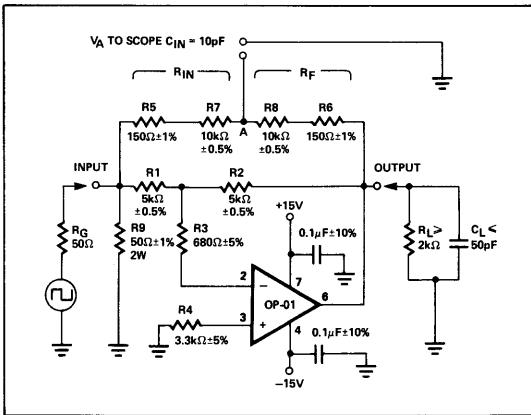
FAST INVERTING AMPLIFIER



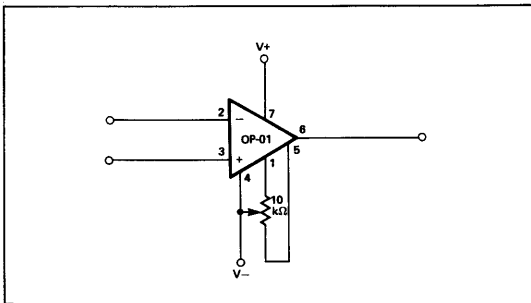
# OP-01

## SETTLING-TIME TEST CIRCUIT

Settling time may be measured using the circuit shown below. This circuit incorporates the "false sum node" technique to produce accurate, repeatable results. For a 5V input step, 0.1% settling will be achieved when the false sum node settles to within  $\pm 2.5\text{mV}$  of its final value. The oscilloscope used for observation of the false sum node should have wide bandwidth, fast overload recovery time, and be used with a low capacity probe ( $\leq 10\text{pF}$ , including strays). A Tektronix 7504 scope with a 7A11 probe or equivalent is suggested. The pulse generator should have a  $50\Omega$  output impedance and be capable of a 5V rise time in  $\leq 20\text{ns}$  with ringing less than  $2.5\text{mV}$  after  $0.5\mu\text{s}$ . Measurements to 0.1% require  $R_{IN}$  to equal  $R_F$  within 0.01%;  $R_5$  and  $R_6$  are used as trimming resistors to achieve this matching.

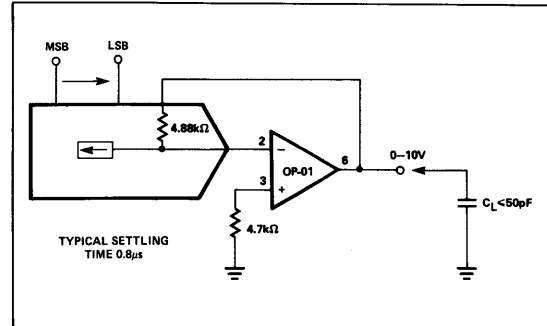


## OFFSET NULLING CIRCUIT



## TYPICAL APPLICATIONS

### FAST VOLTAGE-OUTPUT D/A CONVERTER



### PRECISION POWER-BOOSTER CIRCUIT

