FEATURES

- **Low Bias Current** ..... **5pA Max**
- **Low Current Consumption** ..... **1.0mA Max**
- **High Gain** ..... **1000V/mV Min**
- **High Common-Mode Rejection** ..... **100dB Min**
- **Symmetrical Slew-Rates** ..... **±1.0V/μs Min**
- **Low Harmonic Distortion** ..... **<0.01% at 5kHz**
- **Phase Margin** ..... **77° Typ**

ORDERING INFORMATION†

T_A = 25°C V_{OS} MAX (μV)	PACKAGE TO-99 8-PIN	PACKAGE PLASTIC DIP 8-PIN	OPERATING TEMPERATURE RANGE
500	OP-41AJ*	—	MIL
250	OP-41EJ	—	IND
1000	OP-41BJ*	—	MIL
750	OP-41FJ	—	IND
2000	—	OP-41GP	COM

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

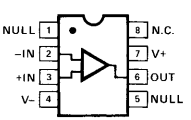
†Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic dip, and TO-can packages. For ordering information, see 1988 Data Book, Section 2.

GENERAL DESCRIPTION

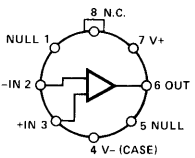
The OP-41 JFET-input op amp features a 5pA max bias current with an open-loop gain of over 1 million. 77° of phase margin provides exceptional stability, even in unity-gain with capacitive loads. The output is guaranteed stable with 250pF loads at unity-gain, and will typically drive several thousand pF. Transient response is extremely clean, and is considerably improved over industry-standard JFET amplifiers.

The OP-41's cascode input stage boosts CMR to over 100dB, improves CMR linearity, and stabilizes bias current with changing common-mode voltage. The linear common-mode rejection of 100dB min is unusually good for a FET input amplifier. The OP-41 consumes only 750μA supply current and has a power-supply rejection ratio of 25μV/V, making it an ideal choice for battery-operated systems. Despite the low supply-drain, the slew-rate is a respectable 1.3V/μs, and symmetrical. Using zener-zap trimming techniques, offset voltage is adjusted to below 500μV which eliminates the need for external nulling in many applications. The OP-41's guaranteed gain of 1 million into a 2kΩ load, combined with the linear 100dB minimum CMR, vastly improves linearity over competitive low-cost devices. Linearity is excellent in both low-gain and high-gain amplifier configurations. In voltage follower applications CMR effects dominate linearity, and in high-gain applications open-loop gain dominates linearity, hence the performance advantage of the OP-41.

PIN CONNECTIONS

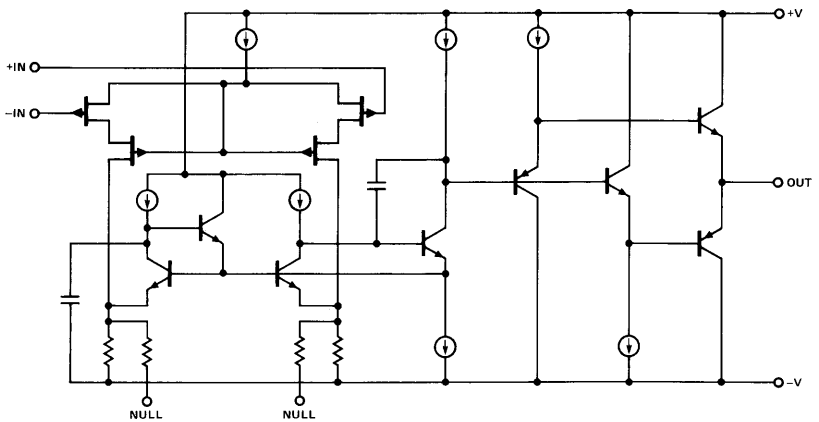


EPOXY MINI-DIP
(P-Suffix)



TO-99
(J-Suffix)

SIMPLIFIED SCHEMATIC



Manufactured under the following U.S. patent: 4,538,115.

OP 41

The device exhibits rapid recovery from signal overload. Following saturation at the positive supply, the output recovers in only 6μs, and from a negative overdrive in only 100ns.

The combination of low-power, low bias current, and high-gain, plus the superior CMR and PSRR performance of the OP-41, make it suitable in a wide variety of demanding applications. The device makes an excellent output amplifier for CMOS DACs. Where low-power consumption is needed in portable instrumentation, the OP-41 permits high-gain and high-accuracy amplification with good speed performance. The low and stable bias current makes it an excellent choice as a photodiode amplifier in medical applications.

A standard 741 pin-out allows existing JFET designs and low-power bipolar designs to be upgraded by switching to the OP-41.

ABSOLUTE MAXIMUM RATINGS

(Note 3)

Supply Voltage ..... ±18V
Internal Power Dissipation (Note 1) 500mW
Input Voltage (Note 2) ..... ±18V
Output Short-Circuit Duration ..... Indefinite
Differential Input Voltage (Note 2) ..... ±18V
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range
OP-41A, B (J) ..... −55°C to +125°C
OP-41E, F (J) ..... −25°C to +85°C
OP-41G (P) ..... 0°C to +70°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature ..... −65°C to +150°C

NOTES:

1. See table for maximum ambient temperature rating and derating factor.

PACKAGE TYPE	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
TO-99 (J)	80°C	7.1mW/°C
8-Pin Plastic DIP (P)	62°C	5.6mW/°C

2. For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.
3. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

			OP-41A/E			OP-41B/F			OP-41G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Offset Voltage	V_{OS}	OP-41E/F/G OP-41A/B	— —	200 200	250 500	— —	400 400	750 1000	— —	500 —	2000 —	μV
Offset Current	I_{OS}	(Note 1)	—	0.04	1	—	0.05	2	—	0.05	5	pA
Bias Current	I_B	(Note 1)	—	3.0	5	—	3.5	10	—	3.5	20	pA
Open-Loop Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	1000	5000	—	500	4000	—	500	4000	—	V/mV
Output Voltage Swing	V_O	$R_L = 2k\Omega$	±12.3	±12.6	—	±12.0	±12.6	—	±12.0	±12.6	—	V
Supply Current	I_{SY}	$V_O = 0V$	—	.75	1.0	—	.75	1.2	—	.75	1.2	mA
Input Voltage Range	IVR	(Note 2)	±11	+15 −11.5	—	±11	+15 −11.5	—	±11	+15 −11.5	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	100	115	—	90	110	—	90	110	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$	—	5	25	—	10	80	—	10	80	μV/V
Noise Voltage Density Referred to Input	e_n	1kHz	—	32	—	—	32	—	—	32	—	$nV/\sqrt{Hz}$
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	±12	+20 −18	±36	±12	+20 −18	±36	±6	+20 −18	±36	mA
Slew Rate	SR		1	1.3	—	1	1.3	—	1	1.3	—	V/μs
Gain Bandwidth	GBW		—	500	—	—	500	—	—	500	—	kHz
Power Bandwidth	BW_P		—	20	—	—	20	—	—	20	—	kHz

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-41A/E MIN	OP-41A/E TYP	OP-41A/E MAX	OP-41B/F MIN	OP-41B/F TYP	OP-41B/F MAX	OP-41G MIN	OP-41G TYP	OP-41G MAX	UNITS
Settling Time	t_s	10V Step $A_V = -1$ to 0.1%	—	10	—	—	10	—	—	10	—	μs
		to 0.01%	—	12	—	—	12	—	—	12	—	
Overload Recovery		Positive Going	—	0.1	—	—	0.1	—	—	0.1	—	μs
		Negative Going	—	6.0	—	—	6.0	—	—	6.0	—	
Capacitive Load Stability		$A_V = +1$ (Note 3)	250	>1000	—	250	>1000	—	250	>1000	—	pF
Open-Loop Output Resistance	R_O		—	150	—	—	150	—	—	150	—	Ω

NOTES:
1. Warmed up. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = -55°C/+125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-41A MIN	OP-41A TYP	OP-41A MAX	OP-41B MIN	OP-41B TYP	OP-41B MAX	UNITS
Offset Voltage	V_{OS}		—	400	1000	—	600	2000	μV
Temperature Coefficient of Input Offset Voltage	TCV_{OS}		—	2.5	5	—	3.5	10	μV/°C
Offset Current	I_{OS}	(Note 1)	—	40	1000	—	50	2000	pA
Bias Current	I_B	(Note 1)	—	4000	7500	—	4500	15000	pA
Open-Loop Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	1000	5000	—	500	3000	—	V/mV
Output Voltage Swing	V_O	$R_L = 2k\Omega$	±12.0	±12.5	—	±11.5	±12.5	—	V
Supply Current	I_{SY}	$V_O = 0V$	—	.75	1.2	—	.75	1.2	mA
* Input Voltage Range	IVR	(Note 2)	±11	+15 −11.5	—	±11	+15 −11.5	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	95	105	—	85	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$	—	5	40	—	10	100	μV/V
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	±6	+12 −17	±36	±6	+12 −17	±36	mA
Slew Rate	SR		1	1.3	—	1	1.3	—	V/μs
Gain Bandwidth	GBW		—	500	—	—	500	—	kHz
Power Bandwidth	BW_P		—	20	—	—	20	—	kHz
Capacitive Load Stability		$A_V = +1$ (Note 3)	100	>1000	—	100	>1000	—	pF

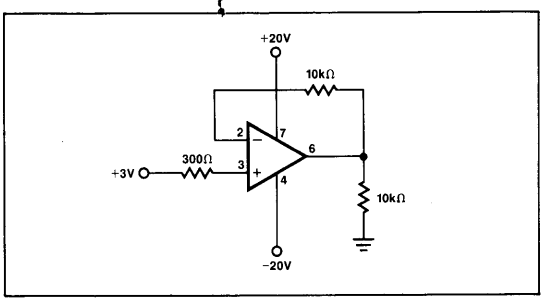
NOTES:
1. Warmed up. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = -25°C/+85°C$ for E/F grades and 0°C/70°C for G grade, unless otherwise noted.

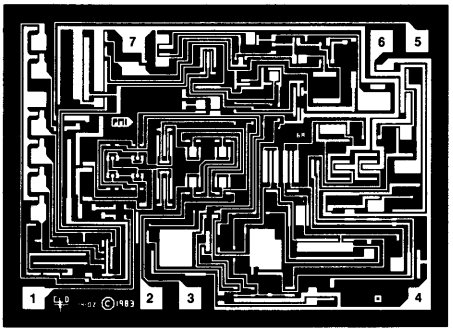
			OP-41E			OP-41F			OP-41G			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Offset Voltage	V_{OS}		—	250	750	—	500	1750	—	500	2500	μV
Temperature Coefficient of Input Offset Voltage	TCV_{OS}		—	3.5	8	—	7.5	—	—	7.5	—	μV/°C
Offset Current	I_{OS}	(Note 1)	—	5	100	—	10	200	—	20	—	pA
Bias Current	I_B	(Note 1)	—	240	500	—	300	1000	—	100	500	pA
Open-Loop Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	1000	5000	—	500	4000	—	500	4000	—	V/mV
Output Voltage Swing	V_O	$R_L = 2k\Omega$	±12.0	±12.6	—	±11.5	±12.5	—	±11.5	±12.5	—	V
Supply Current	I_{SY}	$V_O = 0V$	—	0.75	1.2	—	0.75	1.2	—	0.75	1.2	mA
Input Voltage Range	IVR	(Note 2)	±11	+15 −11.5	—	±11	+15 −11.5	—	±11	+15 −11.5	—	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	95	110	—	85	100	—	85	100	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$	—	5	40	—	10	100	—	10	100	μV/V
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	±6	+16 −18	±36	±6	+16 −18	±36	±6	+20 −18	±36	mA
Slew Rate	SR		1	1.3	—	1	1.3	—	1	1.3	—	V/μs
Gain Bandwidth	GBW		—	500	—	—	500	—	—	500	—	kHz
Power Bandwidth	BW_P		—	20	—	—	20	—	—	20	—	kHz
Capacitive Load Stability		$A_V = +1$ (Note 3)	100	>1000	—	100	>1000	—	100	>1000	—	pF

NOTES:
1. Warmed up. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

BURN-IN CIRCUIT



DICE CHARACTERISTICS



DIE SIZE 0.103 × 0.074 inch, 7622 sq. mils (2.62 × 1.88mm, 4.92 sq. mm)

1. **OFFSET VOLTAGE NULL**
2. **INVERTING INPUT**
3. **NONINVERTING INPUT**
4. **NEGATIVE SUPPLY**
5. **OFFSET VOLTAGE NULL**
6. **AMPLIFIER OUTPUT**
7. **POSITIVE SUPPLY**

For additional DICE ordering information, refer to 1988 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

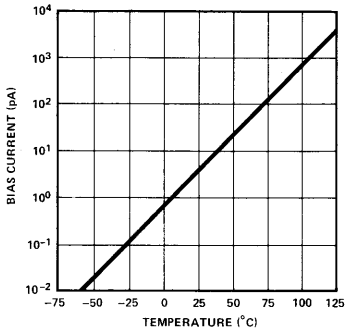
PARAMETER	SYMBOL	CONDITIONS	OP-41N LIMIT	UNITS
Offset Voltage	V_{OS}		1000	μV MAX
Bias Current	I_B	(Note 1)	20	pA MAX
Open-Loop Voltage Gain	A_{VO}	$R_L = 2k\Omega$	500	V/mV MIN
Output Voltage Swing	V_O	$R_L = 2k\Omega$	±12	V MIN
Supply Current	I_{SY}	$V_O = 0V$	1.2	mA MAX
Input Voltage Range	IVR	(Note 2)	±11	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	90	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 10V$ to $\pm 18V$	80	μV/V MAX
Short Circuit Output Current	I_{SC}	Short Circuit to Ground	±6 ±36	mA MIN mA MAX
Slew Rate	SR		1	V/μs MIN
Capacitive Load Stability	$A_V = +1$	(Note 3)	250	pF MIN

NOTES:
1. $V_{CM} = 0$
2. Guaranteed by CMR test.
3. Guaranteed but not tested.

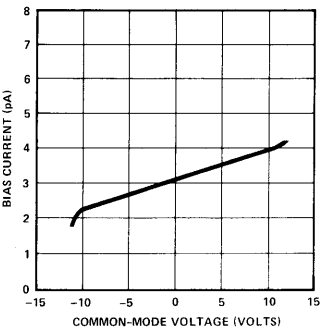
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

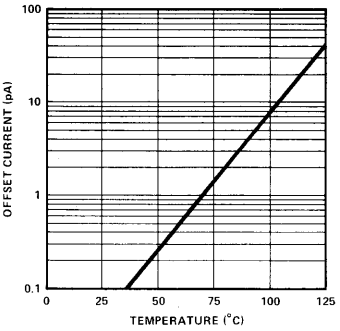
BIAS CURRENT vs TEMPERATURE



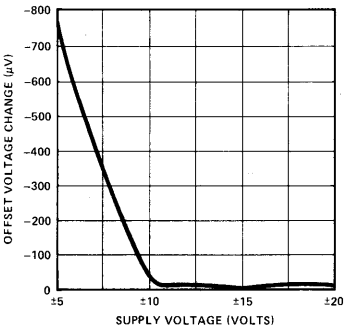
BIAS CURRENT vs COMMON-MODE VOLTAGE



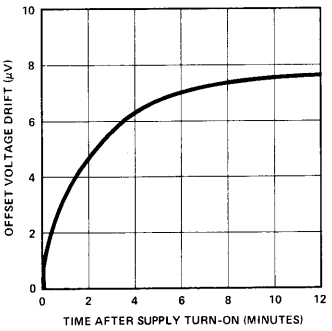
OFFSET CURRENT vs TEMPERATURE



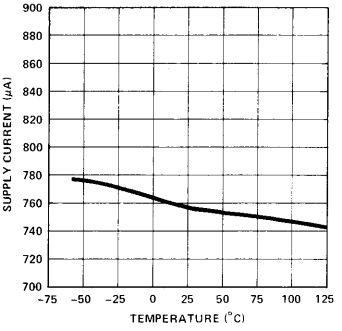
OFFSET VOLTAGE vs SUPPLY VOLTAGE



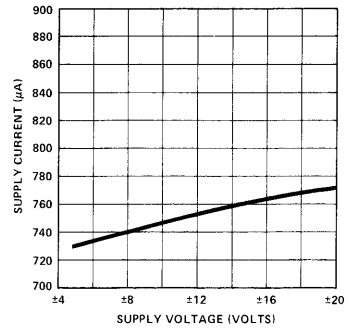
WARM-UP DRIFT vs TIME



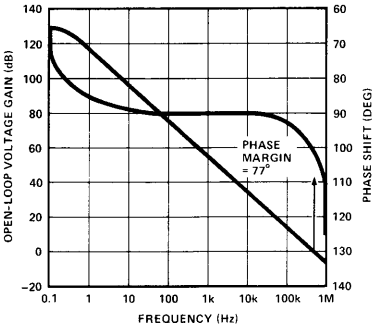
SUPPLY CURRENT vs TEMPERATURE



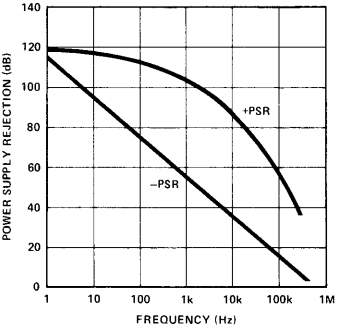
SUPPLY CURRENT vs SUPPLY VOLTAGE



OPEN-LOOP GAIN AND PHASE vs FREQUENCY

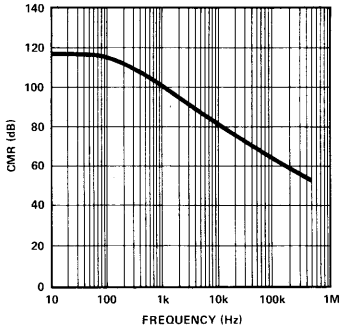


POWER SUPPLY REJECTION vs FREQUENCY

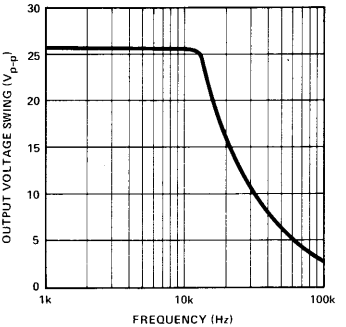


TYPICAL PERFORMANCE CHARACTERISTICS

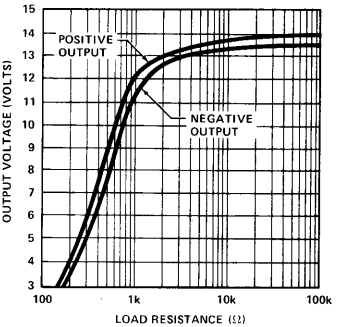
COMMON-MODE REJECTION vs FREQUENCY



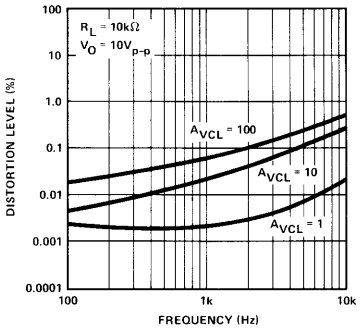
MAXIMUM OUTPUT SWING vs FREQUENCY



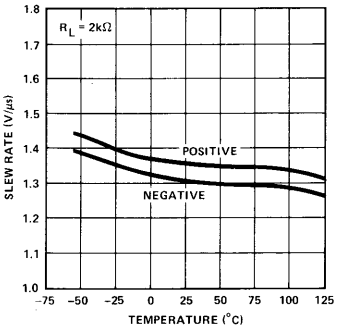
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



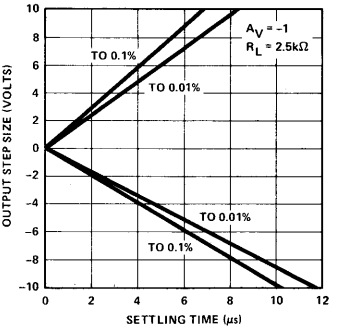
TOTAL HARMONIC DISTORTION vs FREQUENCY



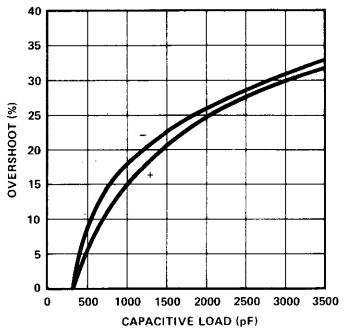
SLEW RATE vs TEMPERATURE



SETTLING TIME



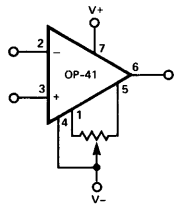
SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD



OFFSET VOLTAGE ADJUSTMENT

Offset voltage is adjusted by a potentiometer of 10kΩ to 100kΩ resistance. This potentiometer should be connected between pins 1 and 5 with the wiper connected to the V- supply. (See Figure 1.) Nulling V_{OS} will change TCV_{OS} by no more than 5μV/°C per millivolt of V_{OS} change.

FIGURE 1: INPUT OFFSET VOLTAGE NULLING



NOTE:
V_{OS} CAN BE TRIMMED WITH POTENTIOMETER RANGING FROM 10kΩ TO 100kΩ.

APPLICATIONS INFORMATION

TYPICAL AC PERFORMANCE CHARACTERISTICS

Figure 2 shows the overload recovery time after the output saturates at each supply. A high degree of slew-rate symmetry is maintained even during severe input overload. The photo also shows the well controlled linear characteristics of the amplifier and freedom from oscillations. The OP-41's symmetry greatly reduces the generation of large DC components in the output when the amplifier is overdriven. This significantly reduces system recovery time after an overload.

Figure 3 shows the unity-gain small-signal transient response of the OP-41. Note the clean symmetrical waveform.

Figure 4 illustrates the high degree of stability even when loaded with 1000pF at unity-gain. Heavy capacitive loading will cause stability problems with many amplifiers.

Figure 5 illustrates the use of the OP-41 in a high sensitivity, wide-dynamic-range light detector. This circuit will produce an output voltage proportional to the light input over a 60dB range.

FIGURE 2: OVERLOAD RECOVERY TIME AT A_V = 10

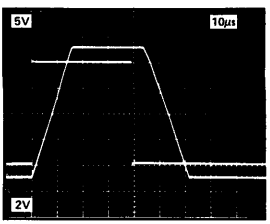


FIGURE 3: SMALL-SIGNAL TRANSIENT RESPONSE

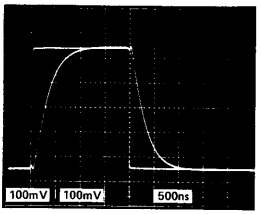


FIGURE 4: SMALL-SIGNAL TRANSIENT RESPONSE WITH 1000pF LOAD

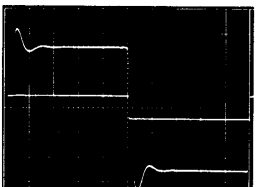
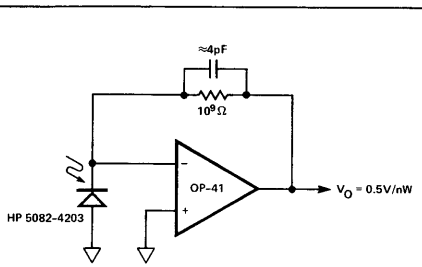


FIGURE 5: WIDE-DYNAMIC-RANGE LIGHT DETECTOR

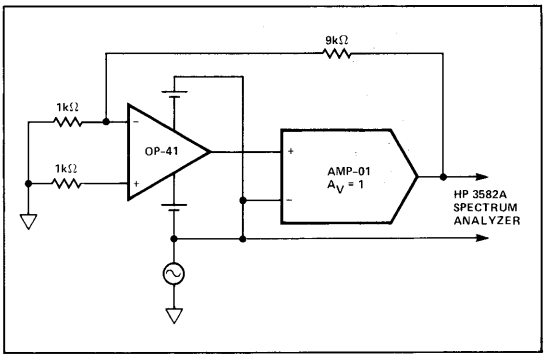


CMR MEASUREMENT METHODS

Two separate methods are used to measure the CMR. The first method is used over the range of 10Hz to 20kHz. This method grounds the input circuitry and applies the common-mode signal to the remainder of the op amp, Figure 6.

The AMP-01 eliminates loading on the output stage. This assures that the OP-41 output is not required to deliver current into the feedback circuit. The effects of the DUT open-loop gain changing with frequency are therefore significantly reduced. The circuit does not require tight resistor matching. DC data sheet limits may be verified using this method. Circuit accuracy is dependent on the high CMR of the AMP-01.

FIGURE 6: CIRCUIT USED TO MEASURE CMR FROM 10Hz TO 20kHz

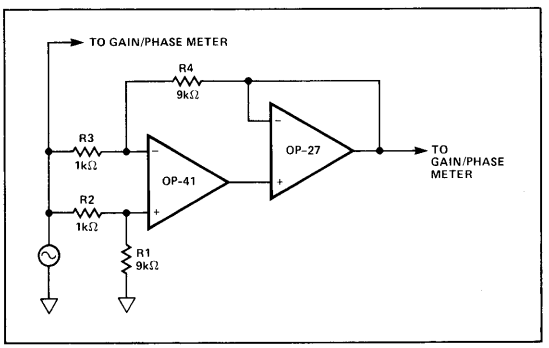


An alternate circuit may be used to make high-frequency measurements from 2kHz to 500kHz, Figure 7. The 2kHz to 20kHz data overlap can be used to verify the accuracy of the respective test methods.

This method drives the input stage with the test signal and requires an accurate ratio of resistors, R4/R3 = R1/R2. To measure CMR to 100dB requires ratio matching to better than 10ppm. For this reason, it is not practical to use the second method at low frequencies where CMR is greater than 80–100dB.

The DUT output is normally connected directly to R4 which may cause problems. If the DUT is not buffered with a broadband low-output-impedance amplifier, the frequency-dependent output impedance of the DUT, in series with R4, rapidly unbalances the resistor ratios. This causes frequency dependent errors. The OP-27 provides good performance over the range of frequencies used.

FIGURE 7: CIRCUIT USED TO MEASURE CMR FROM 2kHz TO 500kHz



GUARDING AND SHIELDING

In applications where the input is at high impedance, careful shielding is required to prevent hum pickup from power line sources or detection of RF from radio stations and nearby radar transmitters. Loss of accuracy can also occur from surface and bulk leakages in printed circuit boards. Both of these conditions can be avoided by the following methods.

Hum and RF pickup are eliminated or reduced by keeping all high impedance leads, including feedback resistor leads, inside shielded enclosures. In addition to shielding, power supply lines should be bypassed where they pass through the shielding. This will prevent noise from being retransmitted from the power supply lines inside the shielded enclosure.

Noise can also be created by the flexing of coax cable. These signals can be caused by mechanical vibrations inside or outside the shielding. Prevention consists of securely supporting all high-impedance shielded lines to prevent motion.

Printed circuit board leakage currents can easily exceed the OP-41 bias currents or the incoming signal. Leakage currents can be minimized by using Teflon insulators to support wires instead of using PC traces. An alternate method is guarding the high impedance traces. When the OP-41 is in the inverting mode, the signal traces should have grounded guard traces on both sides, Figure 8. The opposite side of the board should be used as a ground plane and shield, if not otherwise used. A ground plane is implemented by leaving copper on all areas that are not being used for signal or power conduction. Ground connection should be made to all areas of isolated copper. In the noninverting configuration, the OP-41's output signal or a portion of it should be used to drive the guard traces, Figure 9. When the guard drive voltage is equal to the input signal, leakage currents will be effectively eliminated.

FIGURE 8: CURRENT-TO-VOLTAGE CONVERTER

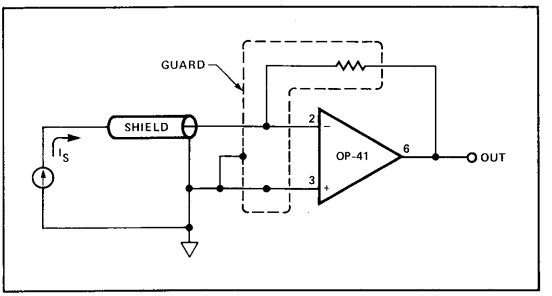
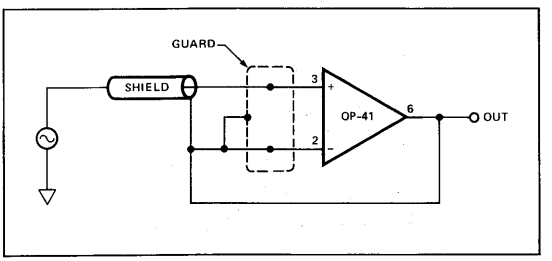
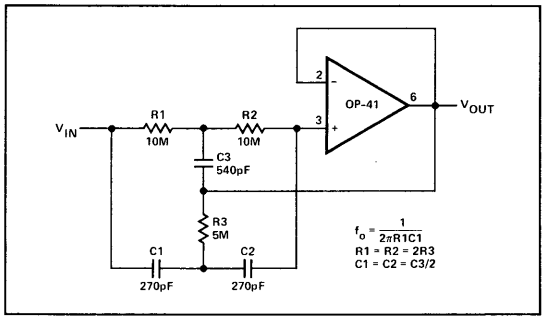


FIGURE 9: VERY HIGH IMPEDANCE NONINVERTING AMPLIFIER



The High Q Notch Filter benefits from the low bias current and high input impedance of the OP-41, Figure 10. These features enable small value capacitors and large resistors to be used in this 60Hz notch filter. The 5pA bias current only develops 100μV across R1 and R2.

FIGURE 10: HIGH Q NOTCH FILTER



Low power consumption, low bias current, and low offset voltage make the OP-41 an ideal current-to-voltage converter, Figure 11.

In this application, the PM-7541 and the OP-41 provide complete 12-bit digital-to-analog conversion with less than 3mA supply current.

FIGURE 11: DAC CIRCUIT USING THE OP-41

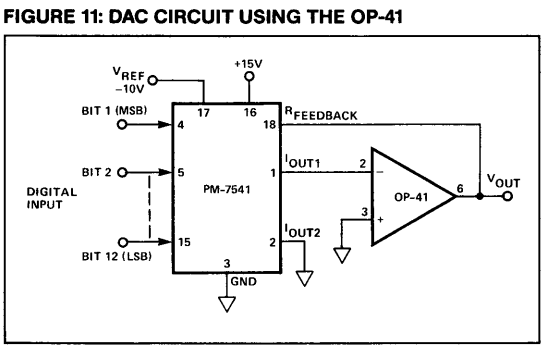
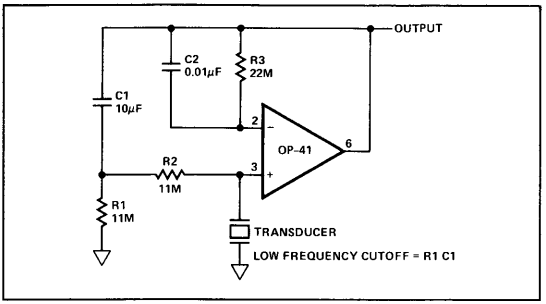


Figure 12 shows an amplifier for high-impedance ac transducers like a piezoelectric accelerometer. These sensors normally require a high-input-resistance amplifier. The OP-41 can provide input resistance in the range of $10^{12}\Omega$, however, a dc return for bias current is needed. To maintain a high R_{IN}, large value resistors above 22MΩ are often required. These may not be practicable.

Using the circuit in Figure 12, input resistances that are orders of magnitude greater than the values of the dc return resistors can be obtained. This is accomplished by bootstrapping the resistors to the output. With this arrangement, the lower cutoff frequency is determined more by the RC product of R1 and C1 than it is by resistor values and the equivalent capacitance of the transducer.

FIGURE 12: AMPLIFIER FOR PIEZOELECTRIC TRANSDUCERS



WIDE RANGE LOW-CURRENT AMMETER

The circuit shown in Figure 13 can measure currents from 100pA to 100μA without the use of high value resistors. Accuracy is better than 1% over most of the range, depending upon the accuracy of the divider resistor and the input bias current of the op amp. Using the OP-41 as the input amplifier allows low end measurement down to a few pA due to the 3.5pA input bias current.

One of the requirements for a good current meter is low series voltage drop. Since the voltage across the inputs of an op amp is forced to virtually zero, it makes a good choice for the input of a current meter. Amplifier A1 is used as an inverting amplifier for the input. This ensures less than 500μV drop at any current level.

Feedback around the op amp is accomplished with a transistor, rather than a resistor. The op amp forces the collector current of Q1A to equal the input current. This causes the emitter-base voltage of Q1A to be proportional to the log of the input current. Resistors R1, R2, R3 and capacitors C1, C2 frequency compensate the log circuit since Q1A provides gain in the feedback loop.

The output of the log amplifier is taken from the emitter of Q1A to drive Q1B. Q1B anti-logs the output and drives the meter. The output of Q1B is proportional to the log of the input current scaled by a constant, which is proportional to the voltage from the divider, selected by S1. For transistors operating at different current levels, the V_{be} difference equals:

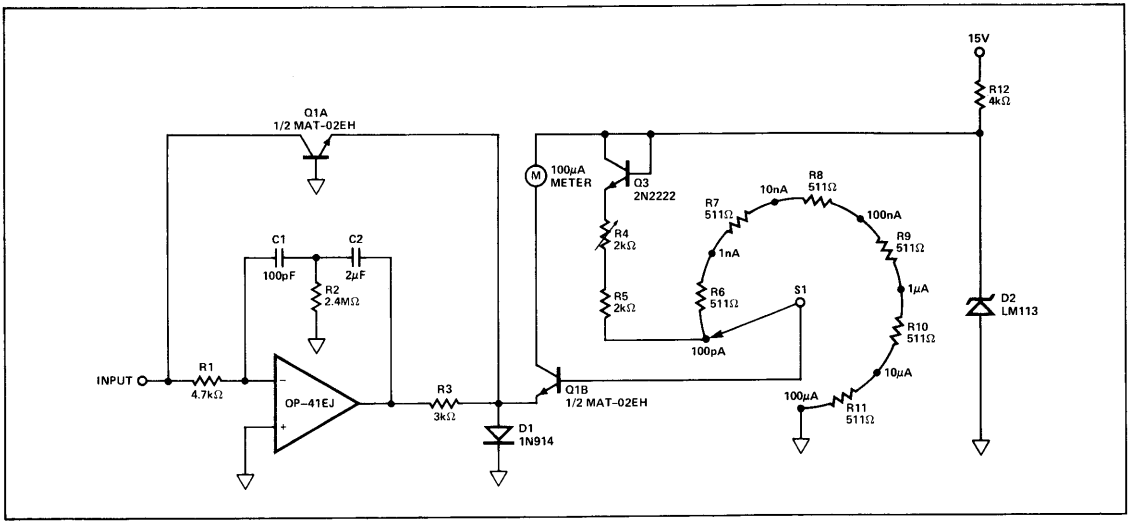
$$\Delta V_{be} = \frac{kT}{q} \ln \frac{IC2}{IC1}$$

solving for IC2

$$IC2 = IC1\ e^{\left(\frac{\Delta V_{be}\, q}{kT}\right)}$$

Where IC1 and IC2 are the collector currents of Q1A and Q1B; Q is the charge of an electron; k is Boltzmann's constant; T is temperature in degrees Kelvin; and V_{be} is the voltage applied to the base of Q1B. If V_{be} varies as absolute temperature, the exponent will be a constant.

FIGURE 13: WIDE RANGE LOW-CURRENT AMMETER



The voltage driving the divider is obtained from a 1.22V low voltage reference diode (LM113) through a 2N2222 transistor and resistor string. The voltage across the divider varies with absolute temperature, keeping the multiplier constant.

Calibration is simple, requiring only one adjustment. R4 is used to adjust full scale deflection with a 1μA input current. This will give maximum accuracy over the operating range of currents.

The low V_{OS} and exceptionally good log conformance of the MAT-02 assure high accuracy over the full 6 decade operating range.

Figure 14 is the test circuit used to measure the settling time. This circuit uses the "false sum-node" technique. When the system is initially set up, the 200Ω pot is adjusted until the DC output voltage to the scope is unchanged when the input is changed from +10V to -10V. The 2N4416 FET buffer isolates the sum node from the scope probe load capacitance. The pulse generator must be properly terminated and have ringing below the expected error signal. (2.5mV in a 5V pulse for 0.1% overshoot measurement.)

FIGURE 14: SETTLING-TIME TEST CIRCUIT