PA09 • PA09A

VIDEO POWER OP AMPS

FEATURES

- V-MOS TECHNOLOGY — 4A peak rating
- HIGH GAIN BANDWIDTH PRODUCT — 150MHz
- VERY FAST SLEW RATE — 400μs
- PROTECTED OUTPUT STAGE — Thermal Shutoff
- EXCELLENT LINEARITY — Class A/B Output
- WIDE SUPPLY RANGE — ±10V to ±40V
- LOW BIAS CURRENT, LOW NOISE — FET Input

APPLICATIONS

- VIDEO DISTRIBUTION AND AMPLIFICATION
- HIGH SPEED DEFLECTION CIRCUITS
- POWER TRANSDUCERS UP TO 5MHz
- COAXIAL LINE DRIVERS
- POWER LED OR LASER DIODE EXCITATION

DESCRIPTION

The PA09 is a high voltage, high current operational amplifier optimized to drive a variety of loads from DC through the video frequency range. Excellent input accuracy is achieved with a dual monolythic FET input transistor which is cascaded by two high voltage transistors to provide outstanding common mode characteristics. All internal current and voltage levels are referenced to a zener diode biased on by a current source. As a result, the PA09 exhibits superior DC and AC stability over a wide supply and temperature range.

High speed and freedom from secondary breakdown is assured by a complimentary V-MOS output stage. For optimum linearity, especially at low levels, the V-MOS transistors are biased in the class A/B mode. Thermal shutoff provides full protection against overheating and limits the heatsink requirements to dissipate the internal power losses under normal operating conditions. A built-in current limit protects the amplifier against overloading. Inductive load kickback protection is provided by two internal clamping diodes. External phase compensation allows the user maximum flexibility in obtaining the optimum slew rate and gain bandwidth product at all gain settings. For continuous operation under load, a heatsink of proper rating is recommended.

These hybrid integrated circuits utilize thick film (cermet) resistors, ceramic capacitors and silicon semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnection at all operating temperatures. The 8 pin TO-3 package is hermetically sealed by resistance welding.

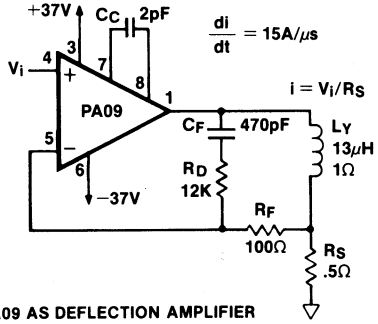
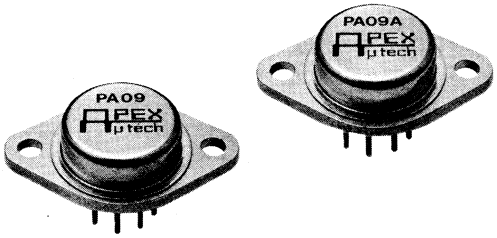
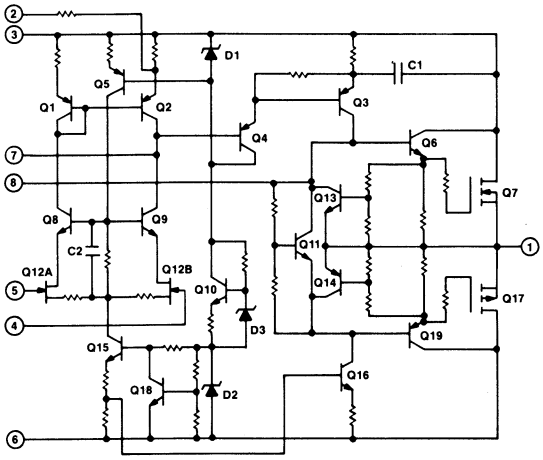


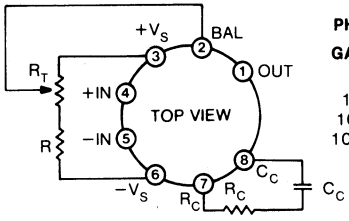
FIG 1: PA09 AS DEFLECTION AMPLIFIER



EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



PHASE COMPENSATION		
GAIN	C_C	R_C
1	100pf	200Ω
10	15pf	0Ω
100	5pf	0Ω
1000	none	none

$$R = (|+V_S| + |-V_S|)\, R_T / 1.6$$

NOTE: Input offset voltage trim optional R_T = 10KΩ MAX

PA09

PA09 ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	80V
OUTPUT CURRENT, source	5A
OUTPUT CURRENT, sink	see SOA
POWER DISSIPATION, internal[1]	78W
INPUT VOLTAGE, differential	40V
INPUT VOLTAGE, common-mode	$\pm V_S$
TEMPERATURE, pin solder-10s	300°C
TEMPERATURE, junction[1]	150°C
TEMPERATURE RANGE, storage	−65 to +150°C
TEMPERATURE RANGE, powered (case)	−55 to +125°C

SPECIFICATIONS

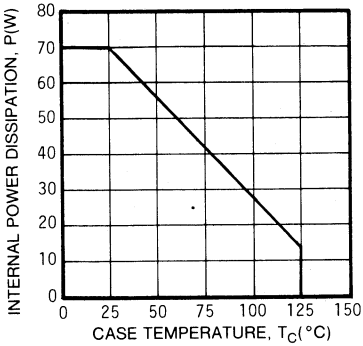
		PA09			PA09A			
PARAMETER	**TEST CONDITIONS[2]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		.5	±3		±.25	±.5	mV
OFFSET VOLTAGE, vs. temperature	T_C = 25°C to +85°C		10	30		5	10	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		10			*		µV/V
OFFSET VOLTAGE, vs. power	T_C = 25°C to +85°C		20			*		µV/W
BIAS CURRENT, initial	T_C = 25°C		5	100		3	20	pA
BIAS CURRENT, vs. supply	T_C = 25°C		.01			*		pA/V
OFFSET CURRENT, initial	T_C = 25°C		2.5	50		1.5	10	pA
INPUT IMPEDANCE, dc	T_C = 25°C		10^{11}			*		Ω
INPUT CAPACITANCE	T_C = 25°C		6			*		pF
COMMON-MODE VOLT. RANGE[3]	T_C = −25°C to +85°C	$\pm V_S$ −10	$\pm V_S$ −8		*	*		V
COMMON-MODE REJECTION, dc	T_C = −25°C to +85°C, V_{CM} = ±20V		104			*		db
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, R_L = 1kΩ		90			*		db
OPEN LOOP GAIN at 10Hz	T_C = 25°C, R_L = 15Ω	80	88		*	*		db
GAIN BANDWIDTH PRODUCT at 1MHz	T_C = 25°C, R_L = 15Ω, C_C = 5pF		150			*		MHz
POWER BANDWIDTH, high gain	T_C = 25°C, R_L = 15Ω, C_C = 5pF		1.2			*		MHz
POWER BANDWIDTH, low gain	T_C = 25°C, R_L = 15Ω, C_C=100pF		.75			*		MHz
OUTPUT								
VOLTAGE SWING[3]	T_C = −25°C to +85°C, I_O = 2A	$\pm V_S$ −8	$\pm V_S$ −7		*	*		V
CURRENT, short circuit	T_C = 25°C		4.5			*		A
SETTLING TIME to .1%	T_C = 25°C, 2V step		.3			*		µs
SETTLING TIME to .01%	T_C = 25°C, 2V step		1.2			*		µs
SLEW RATE, high gain	T_C = 25°C, C_C = 5pF		400			*		V/µs
SLEW RATE, low gain	T_C = 25°C, C_C = 100pF		75			*		V/µs
POWER SUPPLY								
VOLTAGE	T_C = −25°C to +85°C	±12	±35	±40	*	*	*	V
CURRENT, quiescent	T_C = 25°C		70	85		*	*	mA
THERMAL								
RESISTANCE, ac junction to case[4]	T_C = −25°C to +85°C, F>60Hz		1.2	1.3		*	*	°C/W
RESISTANCE, dc junction to case	T_C = −25°C to +85°C, F<60Hz		1.6	1.8		*	*	°C/W
RESISTANCE, junction to air	T_C = −25°C to +85°C		30			*		°C/W

NOTES: * The specification of PA09A is identical to the specification for PA09 in applicable column to the left.

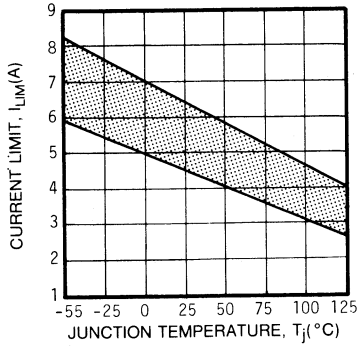
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all tests is ±35V unless otherwise specified as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. The internal substrate contains beryllia (BeO). Do not break the seal. If accidently broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.
6. The PA09M is screened to MIL-STD-883C Class B Method 5008. See Military Models.

PA09 TYPICAL PERFORMANCE GRAPHS

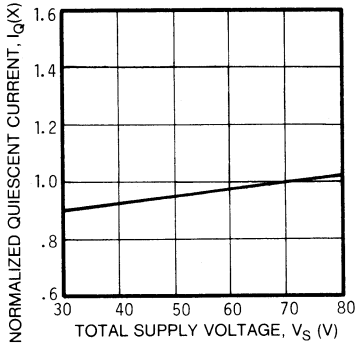
POWER DERATING



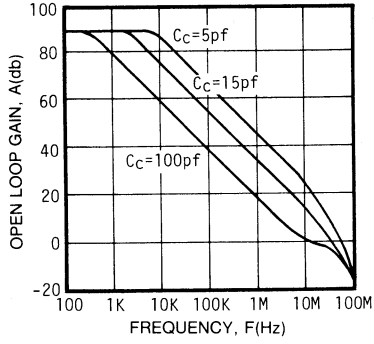
CURRENT LIMIT



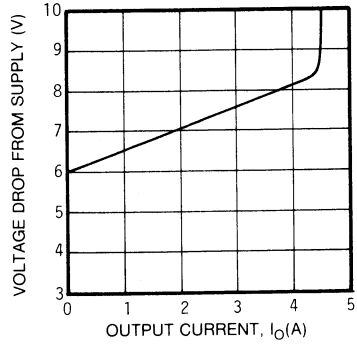
QUIESCENT CURRENT



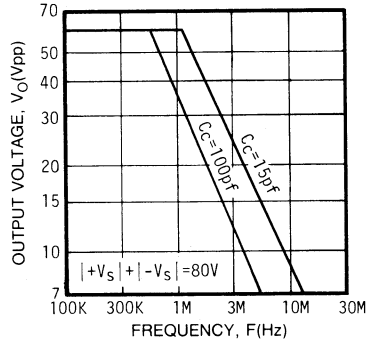
SMALL SIGNAL RESPONSE



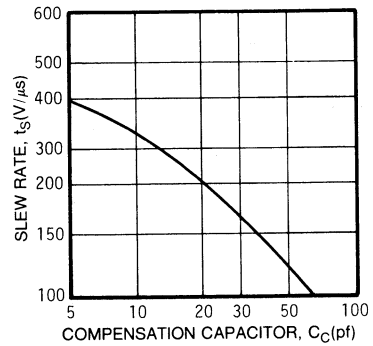
OUTPUT VOLTAGE SWING



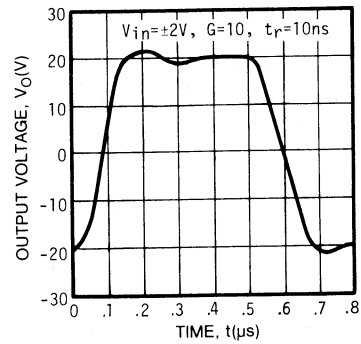
POWER RESPONSE



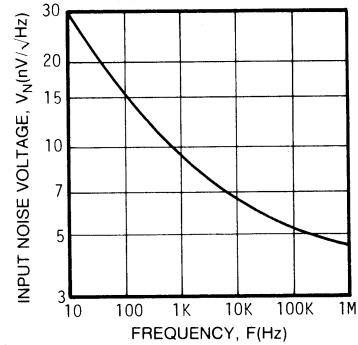
SLEW RATE VS. COMP.



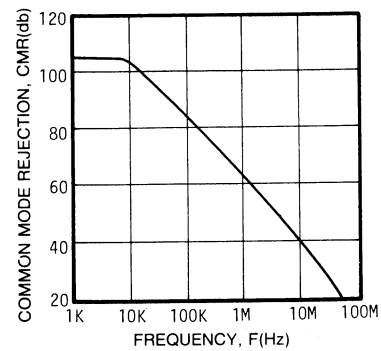
PULSE RESPONSE



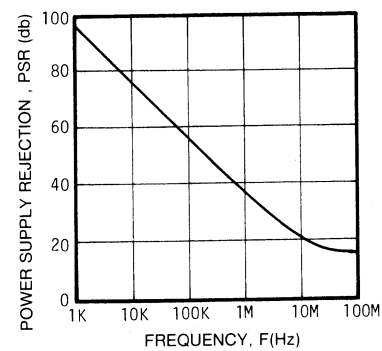
INPUT NOISE



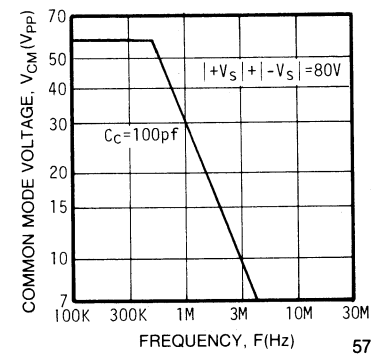
COMMON MODE REJECTION



POWER SUPPLY REJECTION



COMMON MODE VOLTAGE



PA09 OPERATING CONSIDERATIONS

GENERAL

Please consult Power Operational Amplifier Applications, Note 1, "General Operating Considerations", which covers stability, supply, heatsinking, symbols used, and interpretation of specifications. For information on the package outline, heatsinks, and mating sockets, see the "Package Outlines" and "Accessories" sections of the APEX Power Op Amp Handbook. The information given here covers specific considerations for this model.

DEFECTION AMPLIFIER (FIG. 1)

The deflection amplifier circuit on the first page of this data sheet achieves arbitrary beam positioning for a fast heads up display. Maximum transition times are 4μs while delivering 2A pk currents to the 13mH coil. The key to this circuit is the sense resistor (R_S) which converts yoke current to voltage for op amp feedback. This negative feedback forces the coil current to stay exactly proportional to the control voltage. The network consisting of R_d, R_f and C_f serves to shift from a current feedback via R_S to a direct voltage feedback at the upper frequencies. This removes the extra phase shift caused by the inductor thus preventing oscillation. See Application Note 5 for details of this and other precision magnetic deflection circuits.

SUPPLY VOLTAGE

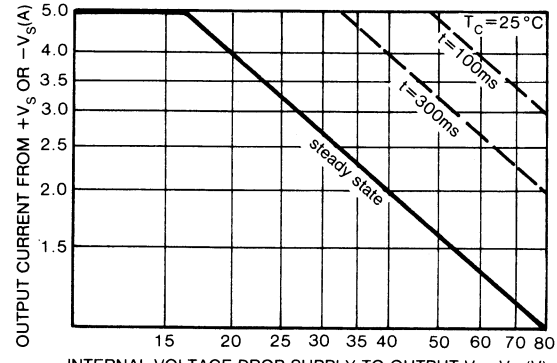
The specified voltage ($\pm V_S$) applies for a dual ($\pm$) supply having equal voltages. A nonsymmetrical (ie. +70/−10V) or a single supply (ie. 80V) may be used as long as the total voltage between the $+V_S$ and $-V_S$ rails does not exceed the sum of the voltages of the specified dual supply.

SAFE OPERATING AREA (SOA)

The output stage of these V-MOS power op amps has 2 distinct limitations:

1. The current handling capability of the wire bonds.
2. The junction temperature of the output transistors.

SAFE OPERATING AREA CURVES



The SOA curves combine the effect of these limits and allow for internal thermal delays. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts:

1. Capacitive and inductive loads up to the following maximums are safe:

$\pm V_S$	CAPACITIVE LOAD	INDUCTIVE LOAD
40V	.1μF	11mH
30V	500μF	24mH
20V	2500μF	75mH
15V	∞	100mH

2. Short circuits to ground are safe with dual supplies up to ±20V.

BYPASSING OF SUPPLIES

Each supply rail must be bypassed to common with a tantalum capacitor of at least 47μF in parallel with a .47μF ceramic capacitor directly connected from the power supply pins to the ground plane.

OUTPUT LEADS

Keep the output leads as short as possible. In the video frequency range, even a few inches of wire have significant inductance, raising the interconnection impedance and limiting the output current slew rate. Futhermore, the skin effect increases the resistance of heavy wires at high frequencies. Multistrand Litz Wire is recommended to carry large video currents with low losses.

GROUNDING

Single point grounding of the input resistors and the input signal to a common ground plane will prevent undesired current feedback, which can cause large errors and/or instabilities.

THERMAL SHUTDOWN

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds safe limits. This allows the heatsink design to be based solely on normal conditions but prevents excessive temperatures during abnormal high power conditions without overdesigning the heatsink.

Under abnormal operating conditions, activation of the thermal shutdown is a sign that the internal temperatures have reached approximately 150°. Continued operation in this temperature range will reduce the life of the product. Also, in this operating mode the device may oscillate in and out of thermal shutoff destroying useful signals.

STABILITY

Due to its large bandwidth the PA09 is more likely to oscillate than lower bandwidth Power Operational Amplifiers. To prevent oscillations a reasonable phase margin must be maintained by:

1. Selection of the proper phase compensation capacitor and resistor. Use the values given in the table under external connections on Page 1 and interpolate if necessary. The phase margin can be increased by using a large capacitor and a smaller resistor than the slew rate optimized values listed in the table.
2. Keeping the external sumpoint stray capacitance to ground at a minimum and the sumpoint load resistance (input and feedback resistors in parallel) below 500Ω. Larger sumpoint load resistances can be used with increased phase compensation and/or bypassing of the feedback resistor.
3. Connect the case to a local AC ground potential.