PA 436

ELECTRONIC INNOVATIONS IN ACTION

SEMICONDUCTORS

85.31 9/68

(Supersedes 85.31 4/68)

Integrated Circuit
Phase Control

PA436

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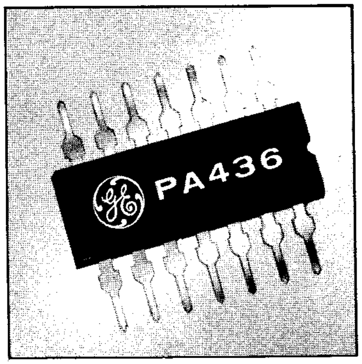
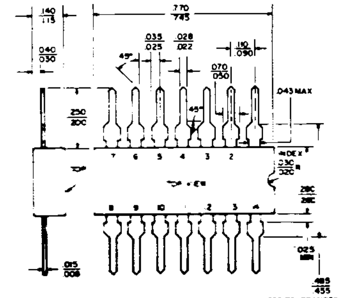
Including Application Notes

The PA436 is a monolithic, phase control, integrated circuit that is intended for use as a triac triggering circuit for resistive and induction motor loads. Its power supply is derived directly from the AC line and requires only 6 external components for complete operation. The circuit offers ramp and pedestal operation, adjustable gain and low power dissipation. In addition, the circuit also has an inhibit function which prevents premature gating of the triac when used with inductive loads, and establishes a minimum triac blocking voltage before gating.

The PA436 operates in either open-loop or feedback mode, using either a DC voltage source or transducer bridge to establish pedestal level. Superimposed on the pedestal level is an adjustable cosine ramp function for a linear relationship between input and output voltage. The slope of the ramp determines the circuit gain and is controlled by external components R_g and C_g.





NOTE: ALL DIMENSIONS ARE IN INCHES AND ARE REFERENCE UNLESS TOLERANCED

Package Outline

absolute maximum ratings: (25°C) (See test circuit)

Supply Current (peak)	$I_{5\text{-}6}$	± 36 mA
Gate Current (pulse)	I_3	± 2 A
Enable Current (peak)	I_9	± 2 mA
AC Terminal Voltage Drop	$V_{5\text{-}6}$	15 Volts
Thermal Impedance (free air)	θ_{JA}	125°C/watt
Operating Temperature (ambient)	T_{opr}	-55° to +85°C
Storage Temperature	T_{stg}	-65° to +150°C
Junction Temperature	T_J	-55° to +125°C

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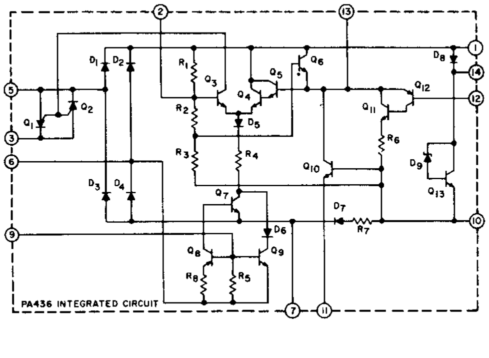
electrical characteristics: (25°C) (See test circuit)

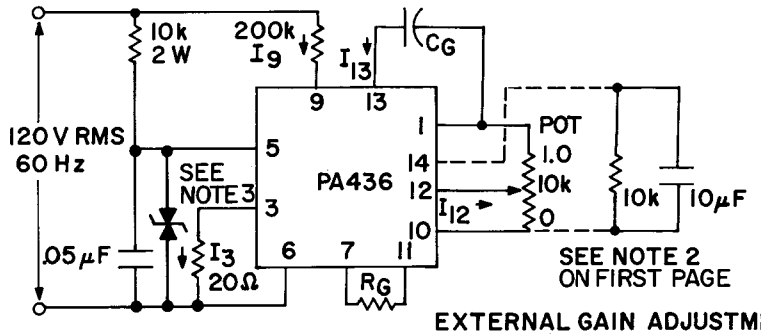
		Min.	Typ.	Max.	
Peak Trigger Pulse Output Current (20 Ohm load) (Note 1)	I_3	250	400	500	mA
Reference Level ($\eta = \frac{V_{12\text{-}10}}{V_{1\text{-}10}}$) (apparent at pin 12)	η	.29	.32	.35	
Enable Current	I_9	60	120	190	μA
Peak Sinusoidal Ramp Current (R_g = 10k)	$I_{13\ ramp}$	60	90	120	μA
Darlington Base Current ($V_{12\text{-}10} = 0.29\ V_{1\text{-}10}$)	$I_{13\ bias}$			3.6	μA
Input (Pedestal) Transistor Current Gain ($R_g = \infty$)	I_{13}/I_{12}	30			
DC Supply Voltage (Note 2)	$V_{14\text{-}10}$	7.5	8.7	11	VDC
Peak Regulated Voltage	$V_{1\text{-}10}$	8.0	9.4	11.5	
Unbalance (DC component in load voltage as a ratio to line RMS voltage)	V_{DC}/V_{line}			.07	

Notes: (1) The PA436 will trigger all GE triac types.

(2) During the measurement of $V_{14\text{-}10}$ (DC supply), the 10k pot between pins 1 and 10 is removed (pin 12 open) and a 10k, 10μF load is placed between pins 14 and 10.



Circuit Diagram



EXTERNAL GAIN ADJUSTMENT VALUES

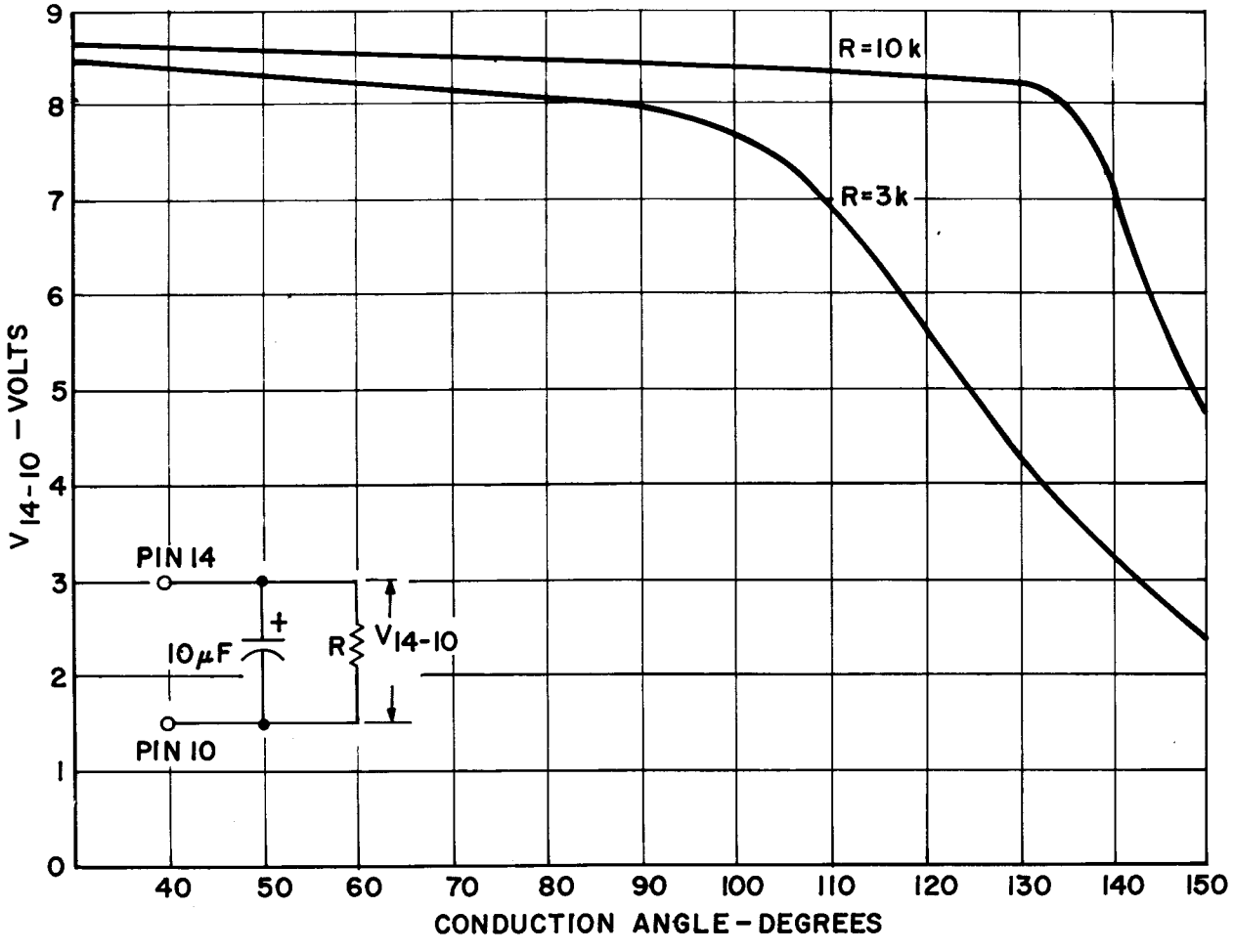
R_G — 7.5k TO 400k

C_G — .01μF TO .1μF

Note 3: To prevent the accidental charging of the 0.05 μF capacitor to voltage and energy levels beyond the range of the PA436 as a result of high contact resistance or during device insertion, a 20-volt back-to-back zener diode is placed across the capacitor in the Test Circuit. This protective device is not required in production after the PA436 has been permanently connected into the circuit.

TEST CIRCUIT

D.C. SUPPLY VOLTAGE VS. CONDUCTION ANGLE



APPLICATIONS OF THE PA436 MONOLITHIC INTEGRATED PHASE-CONTROL TRIGGER CIRCUIT

by E. K. Howell
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INTRODUCTION

The PA436 is a high-gain trigger circuit for phase control of triacs, or SCR's. It is specifically intended for the speed control of AC induction motors, but can also be used on purely resistive loads such as incandescent lamps. This circuit accepts a thermistor signal for temperature control of fans and blowers, or a DC tachometer signal for feedback speed regulation. Adjustable gain, zener-regulated voltage, ambient temperature compensation, and inductive load logic are primary attributes of this integrated trigger circuit.

The PA436 converts an analog input signal to a phase-controlled pulse for triggering thyristors. The signal is compared with a reference and the phase-angle of triggering is obtained by use of the ramp-and-pedestal technique described in Chapter 9 of the GE SCR Manual, 4th Edition.

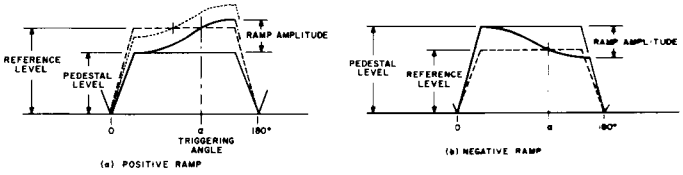

Figure 1. Ramp and Pedestal Waveform

Figure 1(a) shows the typical ramp-and-pedestal waveform, with positive cosine ramp, as is used in unijunction transistor phase control circuits. The PA436 operates with a negative cosine ramp, as shown in Figure 1(b), but with a positive pedestal and reference. A positive input signal establishes the pedestal level and a triggering pulse is generated when the ramp crosses the reference level. A decrease in signal produces a lower pedestal level and therefore, an earlier triggering pulse, hence an increase in load voltage. The "gain" of this type of control can be expressed in terms of change in load voltage per unit change in signal voltage. For convenience in measurement, using a rectifier-type voltmeter, the load voltage is usually expressed as the full-wave-rectified average value. Alternate expressions of "gain" use either the absolute or relative change in signal required to shift the triggering angle from 150° to 30°, which represents changing power in a resistive load from 3% to 97% of full power. The absolute change in signal level required for this triggering range is the same as the ramp amplitude. The relative change in signal is the ratio of ramp amplitude to reference level, usually expressed as a percentage. Since the full range of power is covered by a smaller range of triggering angles with inductive loads, the load power factor can change gain upwards by as much as twice.

Inductive loads, such as induction motors, require a certain logic in the triggering circuit (a detailed description is given in GE Application Note 200.31) in order to achieve reasonable symmetry between the positive and negative portions of the alternating voltage. The PA436 provides this inductive-load logic by taking the time reference for the ramp-and-pedestal waveform from the zero crossing of line voltage and by a lock-out gate that prevents trigger pulses from occurring before the zero crossing of line current.

OPERATION

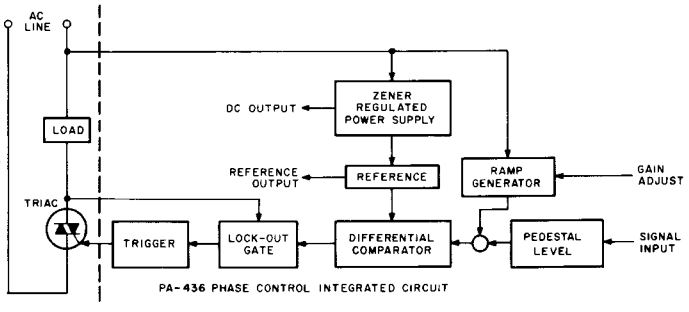

Figure 2. Block Diagram, PA436 Phase Control IC

The block diagram of Figure 2 shows the functions performed within the PA436. The DC input signal establishes a pedestal level to which is added a negative cosine ramp that is derived from the supply voltage and is externally adjustable. The resulting waveform is compared with a zener regulated reference wave in the differential comparator which produces an output signal when the ramp is below the reference level. The lock-out gate blocks this signal from the trigger pulse generator until after line current has passed through zero and voltage has appeared across the triac.

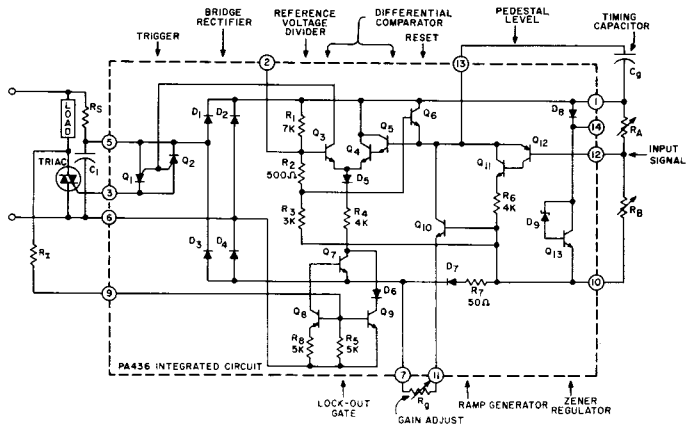

Figure 3. Circuit Diagram, PA436 Phase Control IC

The internal circuit of the PA436 is shown in Figure 3, along with a typical external circuit. Operating supply voltage for the circuit is obtained from the AC line through current-limiting resistor R_S and the bridge rectifier, and is clamped by the zener diode D_9 through transistor Q_{13} and diode D_8. The clamped waveform appearing between terminals 1 and 10 is the supply for the pedestal and reference levels. Note that virtually all circuit current returns through resistor R_7 and diode D_7, and that this current waveshape is a full-wave rectified sinusoid.

A DC signal, such as from external divider R_A and R_B, charges external timing capacitor C_g to the pedestal level through the p-n-p emitter-follower Q_{12}, supplemented by Q_{11}, with current limited by R_6. Capacitor C_g continues charging by a half-sine-wave current through Q_{10} and external emitter resistor R_g, forming the cosine ramp. This current waveshape is obtained by the voltage drop of supply current through R_7, applied to the base of Q_{10}. Amplitude of the ramp charging current is determined by the external emitter feedback resistor R_g, hence this resistor value establishes ramp amplitude. Diode D_7 compensates for the base-emitter voltage of Q_{10}.

The reference voltage level is obtained directly from the zener-clamped supply voltage by divider resistors R_1, R_2 and R_3. Reference voltage is brought out on terminal 2 and can be modified, if necessary, by external resistors to terminals 1 or 10.

The differential amplifier Q_3, Q_4 and Q_5, compares capacitor voltage to the reference voltage. The Darlington connection of Q_4 and Q_5, in addition to presenting a high impedance to the timing capacitor, provides an extra base-emitter voltage offset to compensate for the base-emitter drop of the pedestal emitter-follower Q_{12}. The apparent reference level (i.e. the voltage required at terminal 12 to trigger at the beginning of the ramp) only differs from the voltage at terminal 2 by the relatively small differences in base-emitter voltages of Q_3, Q_4, Q_5, and Q_{12}.

Common mode current of the differential comparator, through D_5 and R_4, is controlled by the lock-out gate D_6, Q_7, Q_8 and Q_9. When load current is flowing through the triac, there is insufficient base drive on either Q_8 or Q_9 to enable conduction of common-mode current, hence the comparator is inhibited from producing an output signal to the trigger. When voltage appears across the triac, current through external resistor R_I enables the lock-out gate and permits normal functioning of the comparator. The value of R_I determines the triac voltage required to enable the comparator.

Trigger pulses are generated by the bilateral switch formed by Q_1 and Q_2 which discharge the external capacitor C_1 into the gate of the triac. Q_1 and Q_2 are triggered by conduction of Q_3, in the comparator, when the ramp voltage drops below the reference level, but only if common mode current can flow through the lock-out gate. Since the trigger pulses alternate with the same polarity as the AC line voltage, they are ideally suited for triggering triacs directly, or pairs of SCR's through a 1:1 pulse transformer.

In order to avoid a carry-over of information from one half-cycle to the next, the timing capacitor must be reset to a fixed level at the end of each half-cycle. This reset function is accomplished by Q_6 which is biased off by dividers R_1, R_2 and R_3 until supply voltage approaches zero. The capacitor voltage then provides a base drive to Q_6, thereby discharging the capacitor to the base-emitter voltage drop.

CIRCUIT DESIGN

Selection of external circuit components is based upon the ratings and characteristics of the PA436, as follows:

R_S: Minimum value is peak line voltage divided by supply current peak rating (I_{5-6}). Maximum value must supply sufficient current to obtain zener clamping over desired triggering range, including current to external loading between terminals 1-10 and 14-10.

C_1: Must store sufficient charge to trigger the external thyristor. 0.05 μf will trigger all GE triacs. Peak discharge current must be limited to pulse rating I_3.

R_1: Minimum value is peak line voltage divided by enable current peak rating, I_9. Maximum value must supply the maximum characteristic enable current over the desired triggering range.

C_g: } R_g: } Select to produce desired gain from peak sinusoidal ramp current specification, I_{13} ramp. Calculate the cosine ramp amplitude by:

$$V_{ramp} = \left(\frac{2\,I_{13}}{\omega C_g}\right)\left(\frac{10{,}000}{R_g}\right) \text{ volts}$$

To this cosine ramp amplitude there must be added a linear ramp amplitude which is caused by the comparator darlington base current, I_{13} bias, where

$$V_{ramp} = \frac{7\,I_{13}}{C} \times 10^{-3} \text{ volts}$$

Normal range of values for C_g is from 0.1 μF to 0.01 μF, and R_g from 7.5k to 100k ohms.

R_A: } R_B: } Normal range of (R_A + R_B) is 10k to 200k ohms. Lower values can produce excessive loading on the supply. Higher values limit charging current for C_g and cause a peak at the leading edge of the pedestal that reduces control gain at the earlier triggering angles. Current gain of the pedestal emitter follower determines this effect.

DC Control Signal Source: When a self-contained DC source is used, such as a tachometer, it should be well filtered and have an output impedance between 2k and 100k ohms. Where a DC supply voltage is needed to create the control signal, a filter capacitor may be connected between terminals 10 and 14. Loading on this capacitor should be 10k ohms or higher to minimize charging current. When such a filter capacitor is used, care should be taken to ensure that triggering cannot occur before the capacitor is charged to zener voltage each half-cycle. This can generally be handled by proper selection of enable current through R_1 and/or by adding a small capacitance between terminals 9 and 6 for a slight phase shift of enable current.

RF Interference Filters: See Chapter 16, GE SCR Manual, 4th Edition.

dv/dt Suppression Circuits: See Chapter 7, GE SCR Manual, 4th Edition.

TYPICAL APPLICATIONS

1. Temperature Control of Fans and Blowers

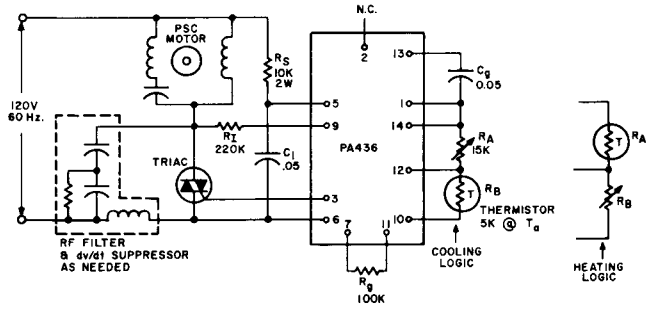

Figure 4. Temperature Control of Fans and Blowers

Figure 4 shows the circuit for controlling speed of a permanent-split capacitor fan motor in response to temperature. For a cooling fan application, R_B is a thermistor having about 5000 ohms resistance at the desired operating temperature. R_A is made variable in order to select the temperature set-point for the control. When temperature increases, fan speed will increase to provide a greater cooling effect. In a heating application, such as a fan-and-coil room heater, the functions of R_A and R_B are reversed so that an increase in temperature will decrease fan speed to provide less heating effect.

The circuit of Figure 4 will control the motor over the full range from zero to 100% speed, hence usually requires a motor with ball bearings. When sleeve bearings are used, it is generally desireable to limit the minimum speed in order to properly maintain bearing lubrication. A low-speed limit may also be wanted in order to maintain a minimum level of air circulation.

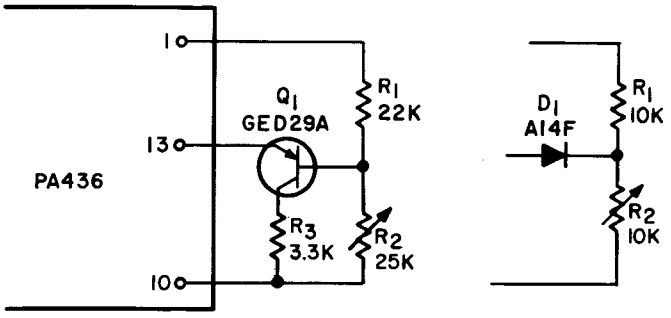

Figure 5. Minimum Speed Clamp

Figure 5 shows a minimum speed clamp circuit that uses an external p-n-p transistor to charge the timing capacitor to an adjustable maximum pedestal voltage. If temperature calls for a speed below the pre-set minimum, the clamp circuit takes over control and holds the motor at the minimum speed desired. In this circuit, the fan never stops. The alternate form of clamp circuit uses a diode instead of a transistor and is better suited for use in low-gain controls where a soft transistion from temperature control to clamping is permissible.

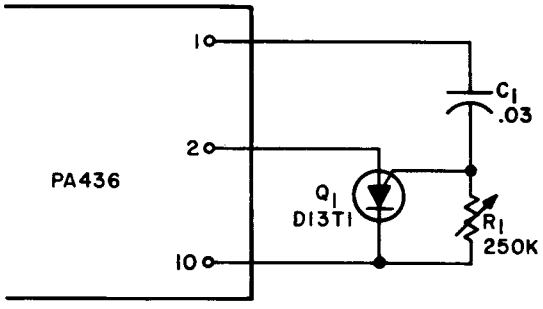

Figure 6. Minimum Speed Cutoff

Figure 6 is a minimum speed cutoff circuit which stops the motor if temperature calls for a speed less than the preset minimum. This is a timing circuit that drops the reference level at a given phase-angle, as set by R_1 and C_1, and prevents triggering beyond that point.

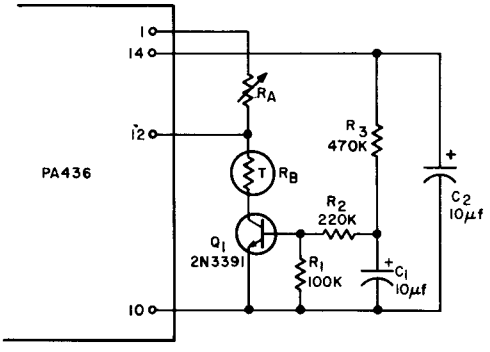

Figure 7. Soft Start Circuit

Motors with high inertia loads may need to be started by the gradual application of power rather than abrupt switching. A soft start circuit is shown in Figure 7 for this purpose. This circuit illustrates the use of a filter capacitor, C_2, to provide a fixed DC voltage for charging the soft-start capacitor C_1. See circuit design section for minimum triggering angle limit.

2. Tachometer Feedback Speed Control

Open loop speed control of AC induction motors is not satisfactory for variable loads. The use of a tachometer for feedback can provide excellent speed regulation under variable load conditions. Whenever feedback control is used, attention must be given to system stability (see Chapter 12, GE SCR Manual, 4th Edition).

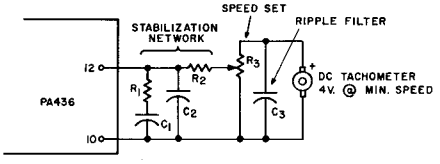

Figure 8. DC Tachometer Circuit

Figure 8 shows the input circuit for a DC tachometer, which may be either a commutator type or an alternator with bridge rectifier. The values of resistors and capacitors depend on specific system requirements. The long term and thermal stability of this system depends heavily on the characteristics and quality of the tachometer.

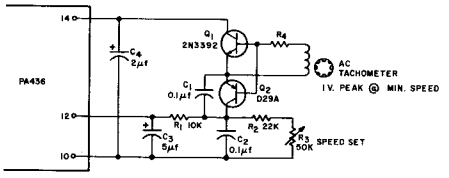

Figure 9. Frequency Sensing AC Tachometer Circuit

The frequency sensing circuit of Figure 9 permits use of a simple, low-cost AC tachometer and is virtually independent of signal amplitude. With each alternation of the tachometer signal, capacitor C_1 is charged and discharged by Q_1 and Q_2. The charging of C_1 also charges C_2 which discharges slowly through R_2 and R_3. The average voltage on C_2 is filtered by R_1 and C_3 and is then the DC control signal for the PA436. Filter capacitor C_4 supplies the DC voltage for the sensing circuit. With the values shown, an 8 pole permanent magnet tachometer, and a 4-pole PSC motor, the circuit had a working speed range from 600 rpm to 1800 rpm.

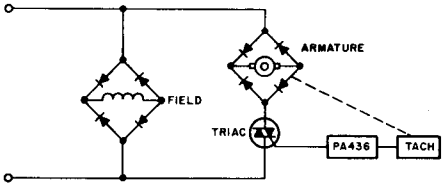

Figure 10. DC Shunt Motor Speed Control

3. DC Motor Speed Control

The same principles of feedback can be used to control the speed of a shunt-wound DC motor also, as shown schematically in Figure 10. The lock-out circuit is important in this application, even though the load is not inductive, in preventing trigger pulse generation until instantaneous line voltage is greater than armature counter EMF.

4. Photoelectric Control of Lamps

The PA436 can provide regulation and control of incandescent lamps by the same circuit of Figure 4, substituting lamps for the motor and a cadmium sulfide photoconductor for the thermistor. For negative feedback control, the "heating logic" connection would be used for the photoconductor. System stability may require the use of an RC stabilizing network similar to that shown in Figure 8.

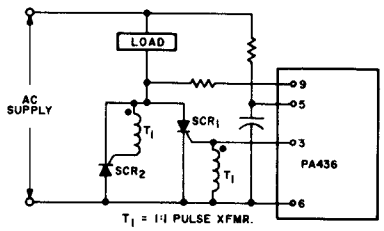

Figure 11. Use of PA436 Driving SCR Pair

5. Triggering SCR's

Although designed specifically for use with a triac, the PA436 is equally capable of triggering a pair of SCR's, as shown in Figure 11. The alternating pulse polarity permits use of a lower-cost 1:1 pulse transformer and avoids the need for balancing gate currents in the SCR's. Magnetizing inductance of the pulse transformer should be low, on the order of 200 µhenries, in order to minimize the possibility of false triggering from the negative transient that can appear at the gate of an SCR as it commutates, particularly at high currents.

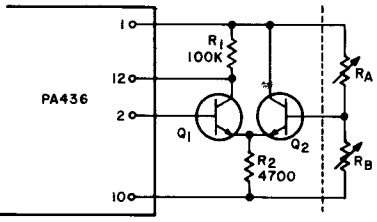

Figure 12. Differential Amplifier Input

6. High Gain Input Pre-Amp

For control systems which need a higher gain than a 10% ramp, the differential amplifier circuit of Figure 12 should be considered. The reference level at terminal 2 is used as one input to the amplifier for stability, temperature compensation, and preservation of apparent reference level at the signal input terminal of the pre-amp. Q_1 and Q_2 may be high-gain transistor, thus permitting use of higher resistances for R_A and R_B. The logic may be inverted by placing R_1 in the collector of Q_2, or by interchanging the functions of R_A and R_B.

7. Transformer-Type Loads

Transformers, reactors and ballasts are distinctly different from other inductive loads such as motors and solenoids in that most transformers have little or no air gap, hence can be easily saturated by a relatively small DC component in the applied voltage wave. An ordinary phase-control circuit, which takes its time reference from either the line voltage or the thyristor voltage alone, can produce gross unbalance, sufficient to damage virtually any inductive load. The PA436 is basically balanced and is very well suited for the control of induction motors. This particular integrated circuit design does have, however, minor irregularities that can produce a small DC component of load voltage (up to a maximum of 0.07 times line voltage). For this reason, the PA436 is not recommended for use with transformers in general, although some specific types may not object to this amount of unbalance.

8. Electric Heat Control

Although phase control has been used many years for electric heating elements, better results can usually be obtained, and at lower cost, by use of the GE PA424 monolithic integrated zero-voltage-switching trigger circuit. Specifications and application information are available in Publication No. 85.21.

CONCLUSION

The PA436 now provides the foundation for a wide variety of flexible, precise, small and low-cost controls for AC power. This monolithic integrated circuit demonstrates that complicated sensing, timing and logic functions can be performed economically in higher voltage, high power thyristor control circuits.

Codes: 40 thru 48, 51, 52, 54, 55, 56, 58

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