SED5032F

CMOS 32-BIT THERMAL HEAD DRIVER

- **Built in 32-bit Static Shift Register**
- **32-bit Latch Circuits**
- **Output Control Circuits and Built in 32-bit Driver**

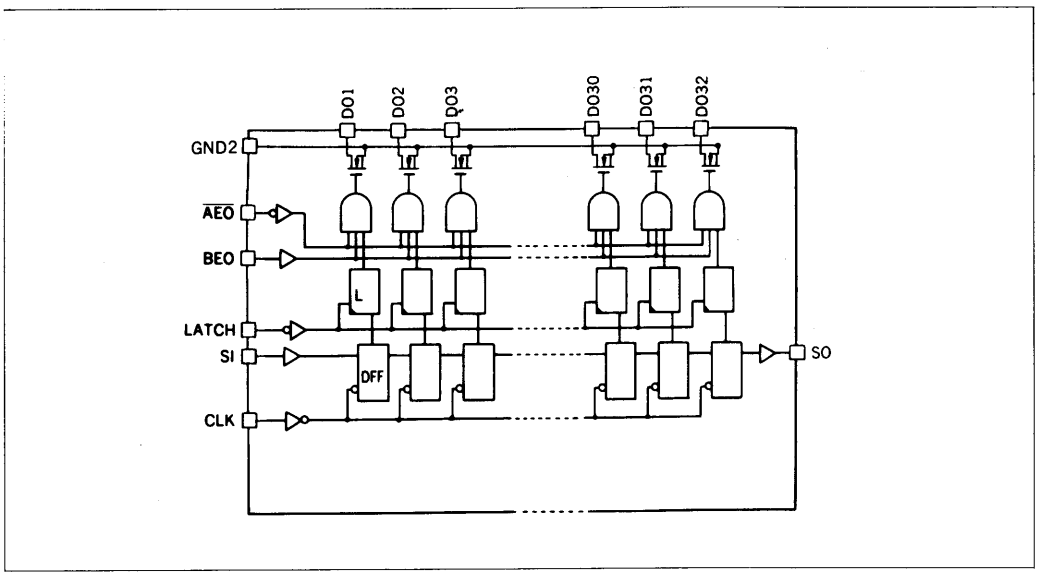
■DESCRIPTION

The SED5032F is a low power CMOS 32-bit thermal head driver. It contains a 32-bit high speed shift register, 32-bit latch, output control circuit and 32-bit driver with a drive capability of 28V/70mA allowing direct connection with thermal heads.

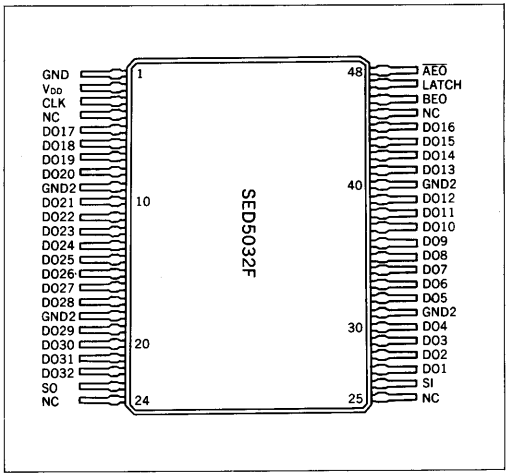
■FEATURES

- Built in 32-bit static shift register
- Built in 32-bit latch
- Built in output control circuit and 32-bit driver
- High supply voltage for driver ····· 28V (Max)
- High output current ····· 70mA (Max)
- Low supply current ····· 0.4mA/2MHz (Typ)
- High speed operation ····· 7MHz (Max)
- Package ····· QFP5-48pin (plastic)

■BLOCK DIAGRAM



■PIN CONFIGURATION



■PIN DESCRIPTION

Pin No.	Pin Name	Function
CLK	3	Clock input for static shift register.
SI	26	Serial data input to shift register.
SO	23	Serial data output from shift register.
LATCH	47	Latch signal input. Data in the shift register is latched when this signal goes low.
$\overline{AEO}$	48	Output enable A. Latched data is enabled for output to the driver when this signal is low. DO terminals are in the high impedance state when this signal is high.
BEO	46	Output enable B. Latched data is enabled for output when this signal is high. DO terminals are in the high impedance state when this signal is low.
DO_n	27~30,32~39 41~44,22~19 18~10,8~5	Parallel data output terminals. (Open drain NMOS transistor output)
V_{DD}	2	Power supply (+5V)
GND	1	Signal ground for input : 0V
GND2	9, 18, 31, 40	Ground for driver output terminals : 0V

■ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Voltage supplied to driver	B_{VDO}	28	V
Driver output current	I_{OLDO}	70	mA
Input voltage	V_I	−0.5 to V_{DD}+0.5	V
Input current	I_I	−20 to 20	mA
Output voltage	V_O	−0.5 to V_{DD}+0.5	V
Power dissipation	P_D	0.25 (Ta=80°C)	W
Operating temperature	T_{opr}	−10 to 80	°C
Storage temperature	T_{stg}	−65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

■RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input voltage	V_I		0	—	V_{DD}	V
Output high voltage DO_n	V_{OHDO}		0	12	24	V
Driver output current	I_{OLDO}		—	45	60	mA
Clock frequency	f_{CLK1}		—	2	7	MHz
	f_{CLK2}*	*for cascade connection	—	2	5	MHz
Clock pulse width	t_{WCLK}		70	—	—	ns
Setup time SI-CLK	t_{setup}		50	—	—	ns
Setup time CLK-LATCH	t_{CL}		100	—	—	ns
Hold time SI-CLK	t_h		10	—	—	ns
Latch pulse width	t_{WLATCH}		50	—	—	ns

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(V_{DD}=5V, Ta=25°C)

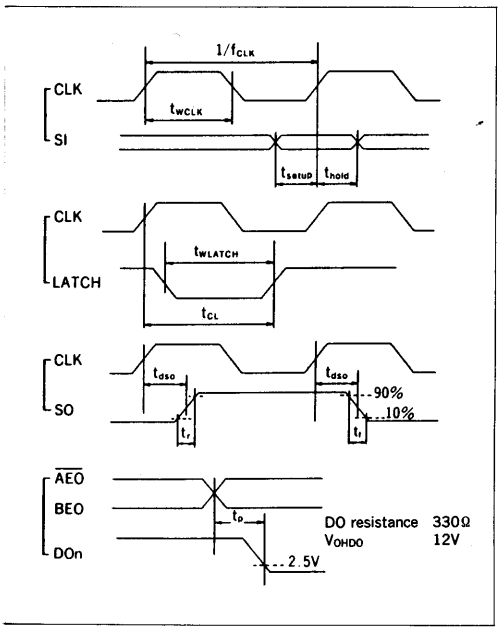
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input high voltage	V_{IH}		3.5	—	5.0	V
Input low voltage	V_{IL}		0	—	1.5	V
Input high current	I_{IH}	V_{IH}=5.3V	—	—	0.5	μA
Input low current	I_{IL}	V_{IL}=−0.3V	—	—	0.5	μA
Output high voltage (SO)	V_{OHSO}	V_{DD}=4.5V, No load	4.45	—	—	V
Output low voltage (SO)	V_{OLSO}	V_{DD}=4.5V, No load	—	—	0.05	V
Output high current (SO)	I_{OHSO}	V_{OH}=4.2V	0.5	2.5	—	mA
Output low current (SO)	I_{OLSO}	V_{OL}=0.4V	0.5	1.5	—	mA
Driver output voltage (DO_n)	V_{OLDO}	I_{OLDO}=60mA	—	0.7	1.0	V
Driver output current (DO_n)	I_{OLDO}	V_{OLDO}= 1.0V	60	80	—	mA
V_{DD} supply current	I_{DD}	V_{DD}=5.5V, f_{CLK}=7MHz	—	1.5	5.0	mA
Output leakage	I_{LO}	V_{DD}=4.5V, V_{OH}=24V	—	—	50	μA

●AC Electrical Characteristics

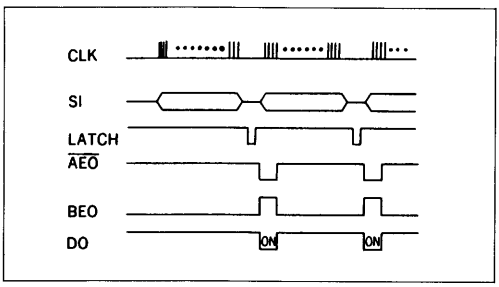
(V_{DD}=5V, Ta=80°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output rise time	t_r	C_L=13pF	—	20	35	ns
Output fall time	t_f		—	20	35	ns
Output (SO) delay time	t_{dso}		—	70	120	ns
Low level propagation time	t_p		—	0.2	1	μs

●Timing Chart

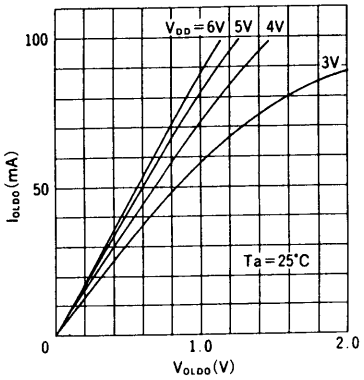


●Signal Sequence

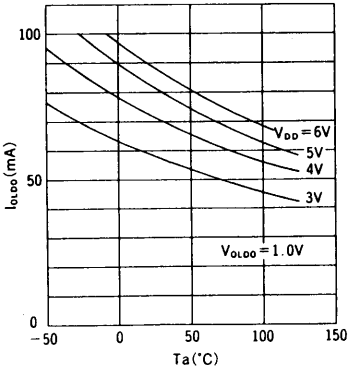


■PERFORMANCE CURVES

Driver output current (I_{OLDO})—Driver output voltage (V_{OLDO})

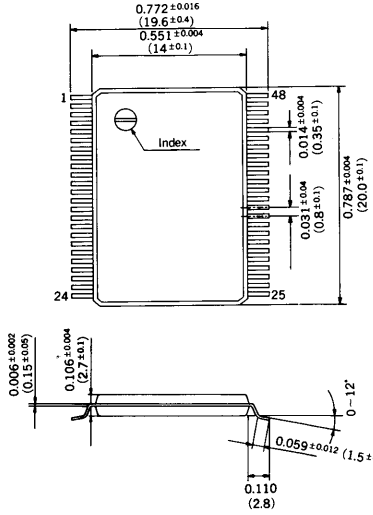


Driver output current (I_{OLDO})—Ambient temperature (Ta)



■PACKAGE DIMENSIONS

Plastic QFP5-48pin



unit : inch
(mm)

SED5064D

CMOS 64-BIT THERMAL HEAD DRIVER

●Built in 64-bit Static Shift Register
●64-bit Latch Circuits
●Output Control Circuits and Built in 64-bit Driver

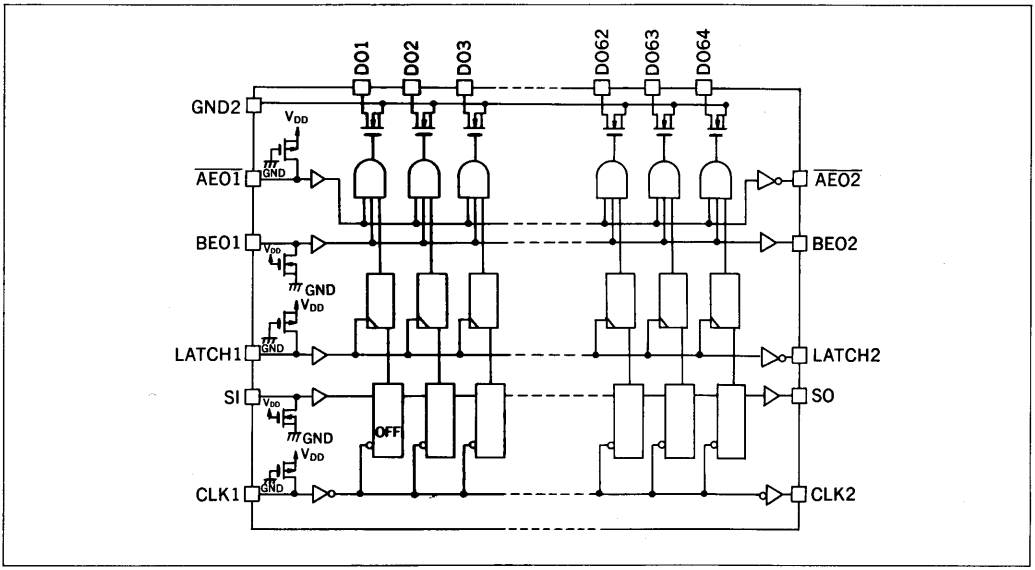
■DESCRIPTION

The SED5064D is a low power CMOS 64-bit thermal head driver. It contains a 64-bit high speed shift register, 64-bit latch, output control circuit and 64-bit driver with a drive capability of 28V/70mA allowing direct connection with thermal heads.

■FEATURES

- ●Built in 64-bit static shift register
- ●Built in 64-bit latch
- ●Built in output control circuit and 64-bit driver
- ●High supply voltage for driver ····· 28V (Max)
- ●High output current ····· 70mA (Max)
- ●Low supply current ····· 0.8mA/2MHz (Typ)
- ●High speed operation ····· 4MHz (Max)
- ●CLK, LATCH, $\overline{AEO}$, BEO

■BLOCK DIAGRAM



■PIN DESCRIPTION

Pad Name	I/O	Functions
CLK1	I	Clock input for static shift register.
CLK2	O	Clock output from static shift register.
SI	I	FF(64-bit) Serial data input to shift register.
SO	O	FF(64-bit) Serial data output from shift register.
LATCH1	I	"H" : through "L" : latched
LATCH2	O	Latch signal output
$\overline{AEO1}$	I	Output enable A. Latched data is enabled for output to the driver when this signal is low. DO terminals are in the high impedance state when this signal is high.

Pad Name	I/O	Functions
$\overline{AEO2}$	O	$\overline{AEO\ 1}$ Output
BEO1	I	Output enable B. Latched data is enabled for output when this signal is high. DO terminals are in the high impedance state when this signal is low.
BEO2	O	BEO 1 Output
DOn	O	Parallel data output terminals. (Open drain NMOS transistor output)
V_{DD}	—	Supply voltage (+5V)
GND	—	Signal ground for input : 0V
GND2	—	Ground for driver output terminals : 0V

■ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	−0.5 to 7.0	V
Voltage supplied to driver	B_{VDO}	28	V
Driver output current	I_{OLDO}	70	mA
Input voltage	V_I	−0.5 to V_{DD}+0.5	V
Output voltage	V_O	−0.5 to V_{DD}+0.5	V
Operating temperature	T_{opr}	−10 to 80	°C
Junction temperature	T_j	−10 to 125	°C
Input current	I_I	−20 to 20	mA

■RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		4.5	5.0	5.5	V
Input voltage	V_I		0	—	V_{DD}	V
Output high voltage DO_n	V_{OHDO}		0	12	24	V
Driver output current	I_{OLDO}		—	45	60	mA
Clock frequency	f_{CLK1}		—	2	4	MHz
	f_{CLK2}*	*for cascade connection	—	2	4	MHz
Clock pulse width	t_{WCLK}		125	—	—	ns
Setup time SI-CLK	t_{setup}		70	—	—	ns
Setup time CLK-LATCH1	t_{CL}		200	—	—	ns
Hold time SI-CLK	t_{hold}		10	—	—	ns
Latch pulse width	t_{WLATCH}		100	—	—	ns
Setup time LATCH-BEO1	t_{LB}		100	—	—	ns

■ELECTRICAL CHARACTERISTICS

●DC Electrical Characteristics

(V_{DD}=5V, Ta=25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input high voltage	V_{IH}		3.5	—	5.0	V
Input low voltage	V_{IL}		0	—	1.5	V
Input high current	I pull down	V_{IH}=5.0V, SI, BEO1	10	33	60	μA
	I_{IH}	V_{IH}=5.0V, $\overline{AEO1}$, CLK1, LATCH1	—	—	0.1	μA
Input low current	I_{IL}	V_{IL}=0V, SI, BEO1	—	—	0.1	μA
	I pull up	V_{IL}=0V, $\overline{AEO1}$, CLK1, LATCH1	10	33	60	μA
Output high voltage	V_{OH}	V_{DD}=4.5V	4.45	—	—	V
Output low voltage	V_{OL}	V_{DD}=4.5V	—	—	0.05	V
Output high current	I_{OH}	V_{OH}=4.6V	0.5	—	—	mA
Output low current	I_{OL}	V_{OL}=0.4V	0.5	—	—	mA
Driver output voltage	V_{OLDO}	I_{OLDO}=50mA	—	0.8	1.1	V
V_{DD} supply current	I_{DD}	V_{DD}=5.5V, f_{CLK}=3MHz	—	1	3	mA
Output leakage	I_{LO}	V_{DD}=4.5V, V_{OH}=24.0V, DOn Pin	—	—	10	μA

●AC Electrical Characteristics

(V_{DD}=5V, Ta=80°C)

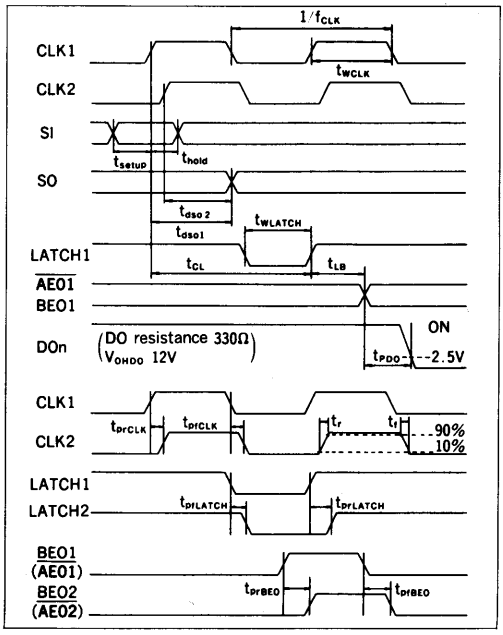
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output rise time	t_r	SO, CLK2, LATCH2	—	20	35	ns
Output fall time	t_f	SO, CLK2, LATCH2	—	20	35	ns
Output (SO) delay time	$t_{dso}1$	CLK1-SO	—	100	160	ns
Output (SO) delay time	$t_{dso}2$	CLK2-SO	10	80	140	ns
Low level propagation time	t_{PDO}	BEO1-DOn($\overline{AEC1}$)	—	0.2	1.0	μs

●AC Electrical Characteristics (Continued)

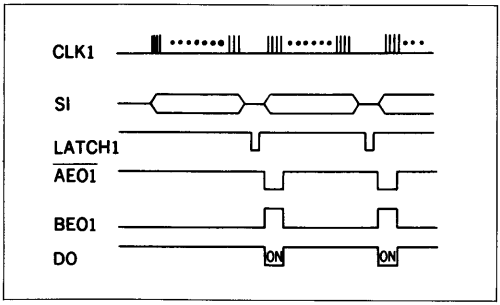
(V_{DD}=5V, C_L=13pF, Ta=80°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Propagation delay time	$t_{pf\ CLK}$ $t_{pr\ CLK}$	CLK1-CLK2	—	15	30	ns
	$t_{pf\ LATCH}$	LATCH1-LATCH2	—	15	30	ns
	$t_{pr\ LATCH}$		—	20	50	ns
	$t_{pf\ BEO}$ $t_{pr\ BED}$	$\overline{AEO1}$-$\overline{AEO2}$ BEO1-BEO2	200	500	1000	ns
	$t_{pf\ CLK}$, $t_{pr\ CLK}$ < $t_{pf\ LATCH}$ < $t_{pr\ LATCH}$					

●Timing Chart

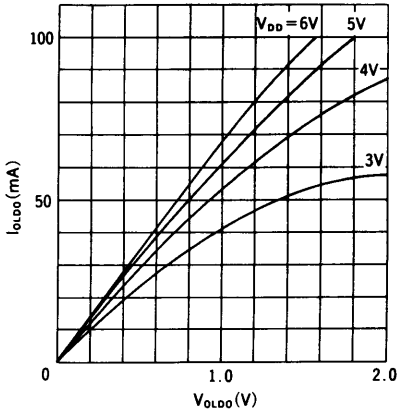


●Signal Sequence

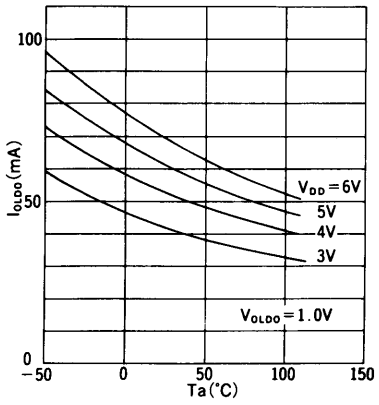


■PERFORMANCE CURVES

Driver output current (I_{OLDO})–Driver output voltage (V_{OLDO})

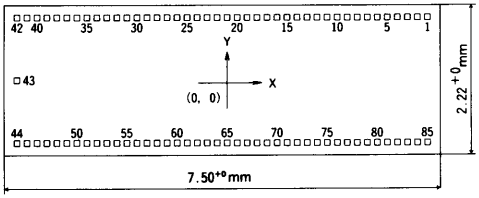


Driver output current (I_{OLDO})–Ambient temperature (Ta)



■PAD LAYOUT OR PAD COORDINATION

●SED5064D



- Bonding Pad Size X×Y=110μm×110μm
- Bonding Pad Pitch X=170μm
- Die Thickness t=250μm

μm

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	DO32	3536	969	44	GND	−3434	−969
2	DO31	3366	969	45	$\overline{AEO2}$	−3264	−969
3	DO30	3196	969	46	CLK2	−3094	−969
4	DO29	3026	969	47	LATCH2	−2924	−969
5	GND2	2856	969	48	BEO2	−2754	−969
6	DO28	2686	969	49	SO	−2584	−969
7	DO27	2516	969	50	DO64	−2414	−969
8	DO26	2346	969	51	DO63	−2244	−969
9	DO25	2176	969	52	DO62	−2074	−969
10	DO24	2006	969	53	DO61	−1904	−969
11	DO23	1836	969	54	GND2	−1734	−969
12	DO22	1666	969	55	DO60	−1564	−969
13	DO21	1496	969	56	DO59	−1394	−969
14	GND2	1326	969	57	DO58	−1224	−969
15	DO20	1156	969	58	DO57	−1054	−969
16	DO19	986	969	59	DO56	− 884	−969
17	DO18	816	969	60	DO55	− 714	−969
18	DO17	646	969	61	DO54	− 544	−969
19	DO16	476	969	62	DO53	− 374	−969
20	DO15	306	969	63	GND2	− 204	−969
21	DO14	136	969	64	DO52	− 34	−969
22	DO13	− 34	969	65	DO51	136	−969
23	GND2	− 204	969	66	DO50	306	−969
24	DO12	− 374	969	67	DO49	476	−969
25	DO11	− 544	969	68	DO48	646	−969
26	DO10	− 714	969	69	DO47	816	−969
27	DO9	− 884	969	70	DO46	986	−969
28	DO8	−1054	969	71	DO45	1156	−969
29	DO7	−1224	969	72	GND2	1326	−969
30	DO6	−1394	969	73	DO44	1496	−969
31	DO5	−1564	969	74	DO43	1666	−969
32	GND2	−1734	969	75	DO42	1836	−969
33	DO4	−1904	969	76	DO41	2006	−969
34	DO3	−2074	969	77	DO40	2176	−969
35	DO2	−2244	969	78	DO39	2346	−969
36	DO1	−2414	969	79	DO38	2516	−969
37	SI	−2584	969	80	DO37	2686	−969
38	BEO1	−2754	969	81	GND2	2856	−969
39	LATCH1	−2924	969	82	DO36	3026	−969
40	CLK1	−3094	969	83	DO35	3196	−969
41	$\overline{AEO1}$	−3264	969	84	DO34	3366	−969
42	V_{DD}	−3434	969	85	DO33	3536	−969
43	NC	−3609	19				

The origin of coordination is center of the chip.