

CURRENT SENSE LATCH

SG1549 / SG2549 / SG3549

DESCRIPTION

This monolithic integrated circuit is an analog latch device with digital reset. It was specifically designed to provide pulse-by-pulse current limiting for switch-mode power supply systems, but many other applications are also feasible. Its function is to provide a latching switch action upon sensing an input threshold voltage, with reset accomplished by an external clock signal. This device can be interfaced directly with many kinds of pulse width modulating control IC's, including the SG1524, SG1525A and SG1527A.

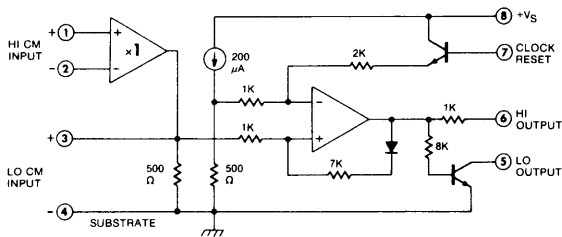
The input threshold for the latch circuit is 100mV, which can be referenced either to ground or to a wide-ranging positive voltage. There are high- and low-going output signals available, and both the supply voltage and clock signal can be taken directly from an associated PWM control chip.

With delays in the range of 200 nanoseconds, this latch circuit is ideal for fast-reaction sensing to provide overall current limiting, short circuit protection, or transformer saturation control.

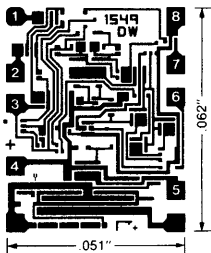
FEATURES

- Current sensing with 100mV threshold
- Common-mode input at ground or to 40V
- Complementary outputs
- Automatic reset from PWM clock
- 180nS delay
- Interface direct to SG1524, SG1525A, SG1527A

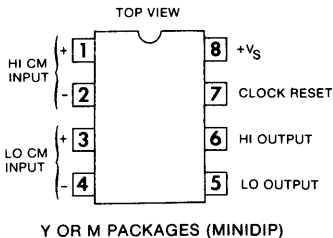
BLOCK DIAGRAM



CHIP LAYOUT



CONNECTION DIAGRAM



SG 1549

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ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, V_S	25V	Operating Temperature Range	
HI CM Input Voltage	40V	SG1549 Y	-55°C to +125°C
LO Output "off" voltage	40V	SG2549 Y or M	-25°C to +85°C
LO Output "on" current	25mA	SG3549 Y or M	0°C to +70°C
Power Dissipation	600mW	Storage Temperature Range	-65°C to +150°C
Derate above 25°C	5.0 mW/°C		

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, these specifications apply over the operating temperature range, with $V_S = +5.0$ volts, and with the circuit unlatched, or reset.)

PARAMETER	TEST CONDITIONS	SG1549/2549			SG3549			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
CM Input	(Note 1)							
Threshold Voltage	Pin 1 & 2 shorted	90	100	110	80	100	120	mV
Input Impedance	$V(\text{Pin } 3) = 50\text{mV}$	400	500	600	400	500	600	Ω
HI CM Input	(Note 1)							
Threshold Voltage	$V_{CM} = 2\text{V}$, Pin 3 open	90	100	110	80	100	120	mV
Threshold Voltage	$V_{CM} = 40\text{V}$, Pin 3 open	90	100	110	80	100	120	mV
Input Current	$V(\text{Pin } 1) = V(\text{Pin } 2) = 40\text{V}$	—	200	300	—	200	300	μA
Clock Reset								
Min. Trigger Voltage		—	2.0	2.5	—	2.0	2.5	V
Input Current	$V(\text{Pin } 7) = 4\text{V}$	—	20	40	—	20	40	μA
HI Output								
Off Voltage		—	0	0.1	—	0	0.1	V
On Voltage	$I_L = 1\text{mA}$	2.8	3.2	—	2.8	3.2	—	V
LO Output								
Off Leakage	$V(\text{Pin } 5) = 40\text{V}$	—	.01	1.0	—	.01	1.0	μA
On Voltage	$I_L = -10\text{mA}$	—	.3	0.5	—	.3	0.5	V
Supply Current	$V(\text{Pin } 8) = 5\text{V}$	—	2	3	—	2	5	mA
	$V(\text{Pin } 8) = 20\text{V}$	—	10	15	—	10	15	mA

Note 1: Input threshold voltages and supply current are directly proportional to supply voltage, V_S .

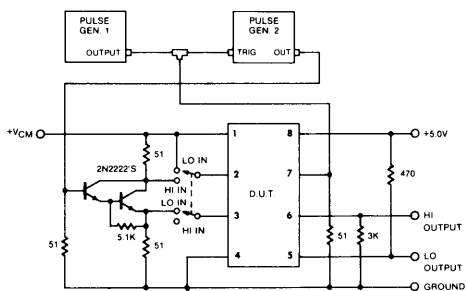
TYPICAL SWITCHING CHARACTERISTICS $V_S = 5\text{V}$, $T_A = 25^\circ\text{C}$

PARAMETER	SYMBOL	CONDITIONS	TYPICAL	UNITS
Reset Minimum Pulse Width	t_{w1}	Amplitude = 3.0V	150	nSec
Delay from Reset to LO Output	t_D (off)	$R_L = 470\Omega$ to V_S	300	nSec
LO Input Minimum Pulse Width	t_{w2}	Amplitude = 200mV	50	nSec
Delay from LO Input to LO Output	t_D (on) LO CM	Amplitude = 200mV $R_L = 470\Omega$ to V_S	180	nSec
Delay from HI Input to LO Output	t_D (on) HI CM	Amplitude = 200mV $V_{CM} = 5\text{V}$	300	nSec
Delay from HI Output to LO Output		LO CM Input = 200mV	30	nSec

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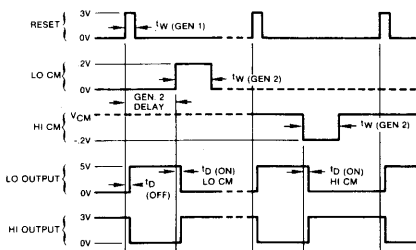
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DYNAMIC TEST CIRCUIT



Note: Pulse Gen. 2 must have triggering, delay and amplitude controls.

SWITCHING WAVEFORMS



Note: HI OUTPUT Precedes LO OUTPUT by approximately 30 nSec.

SCHEMATIC

