PLESSEY
Semiconductors

SL1030C

200MHz WIDEBAND AMPLIFIER

The SL1030 is a silicon integrated circuit designed for use as a general purpose very wideband amplifier. External components enable users to tailor the characteristics of the amplifier for particular applications. The gain can be selected between 20 and 60dB; the input impedance can be 50Ω, 75Ω or 1kΩ, and the compromise between current consumption and output swing can be selected by the external components.

A regulator is provided on the chip, enabling supply voltages from 8 to 15 volts to be used with no variation in characteristics. Alternatively, the regulator can be bypassed and supplies from 4.0 to 10 volts used.

The amplifier is protected against damage from input voltage transients and is stable when driving capacitive and inductive loads.

FEATURES

- Bandwidth up to 200 MHz
- Low Noise
- Single Supply
- Input Impedance Adjustable – 50Ω, 75Ω or 1kΩ
- Gain Programmable between 20dB and 60dB
- Drives Capacitive or Inductive Loads

APPLICATIONS

- Wideband Pulse Amplifiers
- Frequency Selective IF Amplifiers
- Low Noise Preamplifiers

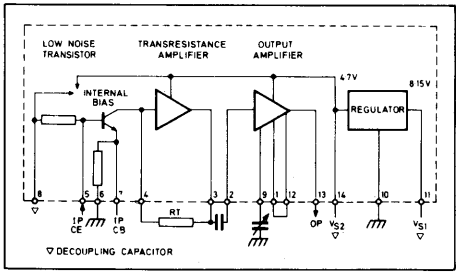

Fig. 1 General schematic

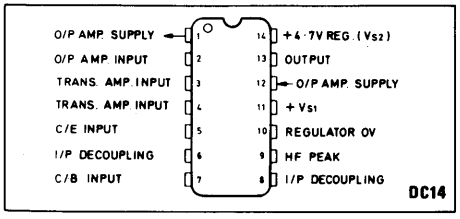

Fig. 2 Pin connections (top)

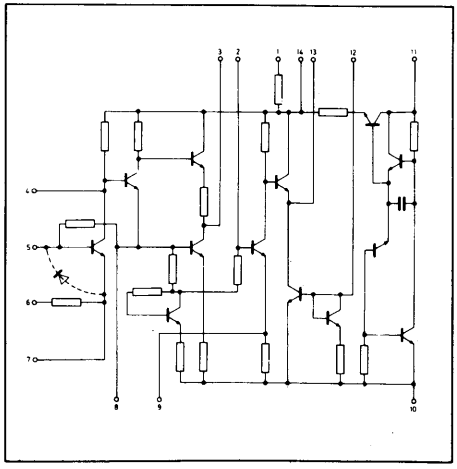

Fig. 3 Circuit diagram

QUICK REFERENCE DATA

Supply Voltage	+4V to +15V
Supply Current at V_S = 10V	20 mA (Typ.)
Voltage Gain at 100 MHz	40dB (Typ.)
Noise Figure at 100 MHz, R_S = 50Ω	3dB (Typ.)
Second Order Intermodulation Distortion	–50dB (Typ.)

SL 1030

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 22°C ±2°C
V_{S1} = 10V
R_1 = 1 kilohm
R_2 = 32 kilohms

Characteristic	Value					Conditions
	Test Cct	Min.	Typ.	Max.	Units	
Voltage gain	A		30		dB	f = 30MHz
	B	35	40	44	dB	f = 30MHz
Gain flatness			±0.5		dB	f=10kHz to 150kHz (Note 1)
Noise figure	A		6.5		dB	f=100MHz, R_S=50Ω
	B		3.0	4.5	dB	
Gain compression	A		0.2	1.0	dB	f=100MHz, load impedance = 50Ω, P_{out}=0dBm
Output voltage	B		1		V p–p	f=10MHz, load impedance =100Ω
Rise time	B		3		ns	V_{out}=1.0V p–p
Input VSWR (See Fig. 16)	A		1.2			f=10kHz to 150MHz wrt 50Ω
Supply current			20	30	mA	V_{S1}=10V or V_{S2}=5V
Regulation $\Delta V_{S2}/\Delta V_{S1}$			1	5	%	V_{S1}=10V to 15V
Intermodulation distortion						
2nd order	A		−60		dB	P_{out}=0dBm, V_{S2}=10V
3rd order	A		−80		dB	(See Fig.6, notes 2 and 3)
Harmonic distortion						
2nd harmonic	A		−30		dB	f=100MHz, P_{out}=0dBm
3rd harmonic	A		−40		dB	V_{S2}=10V, R_L=50Ω (See note 3)
Input impedance						
Common base			16		Ω	f<10MHz
Common emitter			1		kΩ	

NOTES

1. The gain flatness is dependent on layout and on the value of the peaking capacitor. See OPERATING NOTES for details.
2. In each of two tones at 10 and 10.5 MHz, R_L = 50Ω
3. Referred to output.

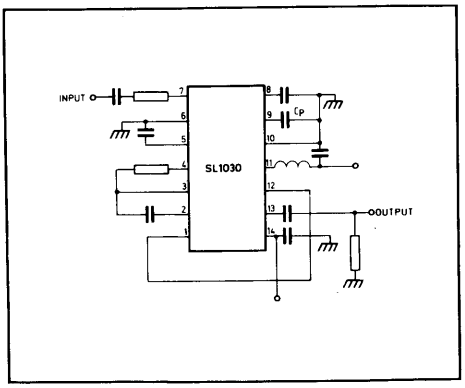

Fig. 4 Test circuit A – common base

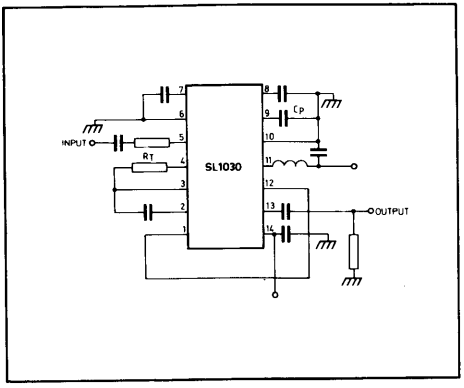

Fig. 5 Test circuit B – common emitter

TYPICAL ELECTRICAL CHARACTERISTICS

The following conditions apply to the characteristics given in Figs. 6 to 16 unless otherwise stated:

Free air temperature	22°C
Load resistance	50Ω
R_T	1 kΩ

Intermodulation products (Fig. 6) are measured with specified output power in each of two tones at 10 MHz and 10.5 MHz.

The values for C_P quoted in Figs. 12 and 13 were selected with R_L = 50Ω but will vary with load impedance and circuit layout.

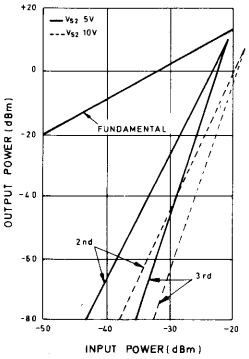

Fig. 6 Intermodulation products

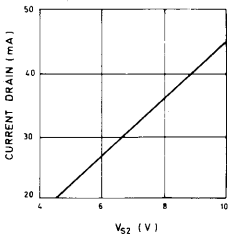

Fig. 7 Supply current v. unreg. supply voltage

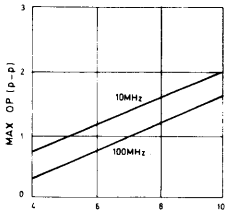

Fig. 8 Max o/p voltage v. unreg. supply voltage

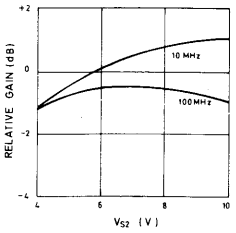

Fig. 9 Common base gain v. unreg. supply voltage

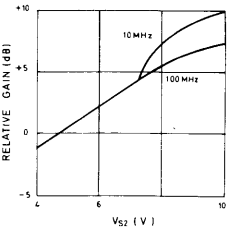

Fig. 10 Common emitter gain v. unreg. supply voltage

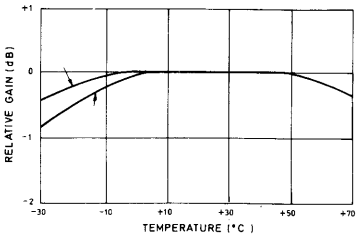

Fig. 11 Gain v. temperature

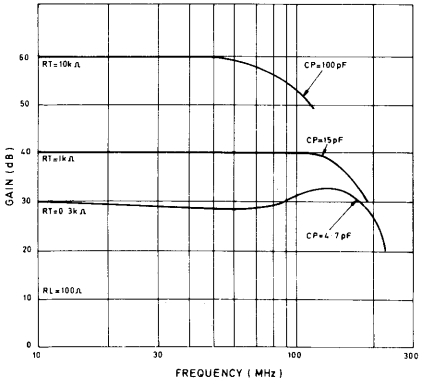

Fig. 12 Common emitter gain v. frequency

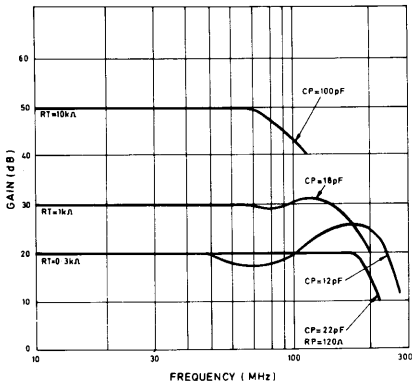

Fig. 13 Common base gain v. frequency

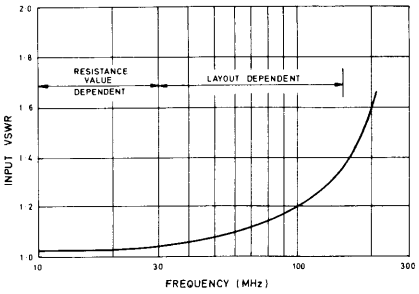

Fig. 16 Input VSWR v. frequency

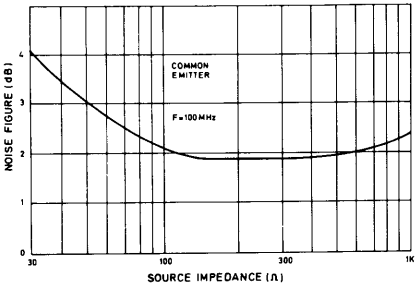

Fig. 14 Noise figure v. source impedance

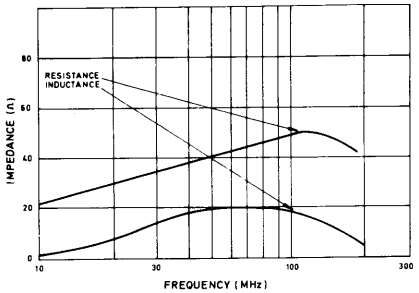

Fig. 15 Output impedance v. frequency

OPERATING NOTES

Low Noise Input Stage

As shown in Fig. 1, the input transistor can be used in common base or common emitter by using either pin 7 or pin 5 as the input, the other pin being decoupled. If a well-defined 50 or 75Ω input impedance is required, then a circuit similar to test circuit A (Fig. 4) should be used. An accuracy of ± 5% can be expected in the input impedance of this circuit since the input impedance of the common base stage is very reproducible and also is to some extent masked by the external resistor. A return loss of 30dB up to 100 MHz can be achieved with careful layout and the use of a physically small, accurate external resistor. The value of the resistor should be 56Ω for 75Ω input impedance and 33Ω if 50Ω input impedance is required.

The noise figure of this transistor is flat from the flicker noise knee around 10 Hz to over 150 MHz.

Transresistance Amplifier

The transresistance amplifier will operate correctly for values of R_T from 200Ω to 10 kΩ. The voltage gain of the complete amplifier is of course directly proportional to R_T. See Figs. 12 and 13.

Output Stage

When the internal regulator is bypassed for applying the supply voltage to pin 14, some control of the quiescent current is possible. The biasing circuitry has been designed so that the individual currents track together with the supply voltage and with each other. This enables a significant improvement to be made in the output swing into low impedance loads at the expense of increased current consumption. See Fig. 7. The quiescent current of the first device also increases, giving an increase in gain in the common emitter configuration. The quiescent current in the output stage can be varied by means of an external resistor. The link between pins 1 and 12 must be removed and a resistor added between pins 14 and 12. The current is 10 mA with 2.5 kΩ and is approximately inversely proportional to the resistor value.

Peaking Capacitor C_P

The frequency response of the amplifier is dominated by the output emitter follower which begins to roll off at about 50 MHz. The high frequency peaking capacitor is used to compensate for this roll-off and also that due to stray inductance and capacity in the external circuitry. The typical curves were measured with an SL1030 directly soldered into a PC board and the values of the peaking capacitor given will be more typical of the normal situation.

Layout and Stability

Since gains of 40dB are available up to VHF frequencies normal high frequency layout precautions are necessary with respect to grounding and decoupling. Decoupling capacitors should be low inductance ceramic types (Erie Weecons are ideal) and to ensure good earth connections a continuous ground plane should be provided around and underneath the circuit. Decoupling of pins 5 or 7 is critical and inadequate decoupling of pin 14 can cause instability. Since no overall feedback is used, the amplifier is very tolerant of load reactance and no instability has been observed even with pure capacitive loads. A certain amount of care is needed when using the internal regulator. If the decoupling on pin 11 is effective above 200 MHz, then instability can occur within the regulator. This can be completely stopped by inserting an inductance of a few hundred nanohenries between the decoupling capacitor and pin 11 as shown on the test circuits.

ABSOLUTE MAXIMUM RATINGS

V_{S1} (Pin 11)	+15V
V_{S2} (Pin 14)	+10V
Storage temperature	−55°C to +150°C
Operating temperature (ambient)	−55°C to +125°C