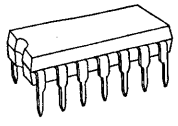
TC35304P/F

DTMF RECEIVER

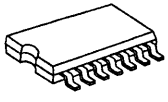
Advance Information

1. GENERAL DESCRIPTION

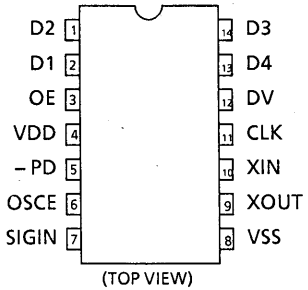
The TC35304P/F is an LSI designed for detecting Dual Tone Multiple Frequency (DTMF) signal used in Touch-Tone dialing. DTMF signal is filtered through high and low group filters and encoded into 4-bit code after a digital detecting circuit. A 3-state data outputs circuit allows its easy interface with other devices.



DIP14 (DIP14-P-300)



SOP14 (SOP14-P-300)



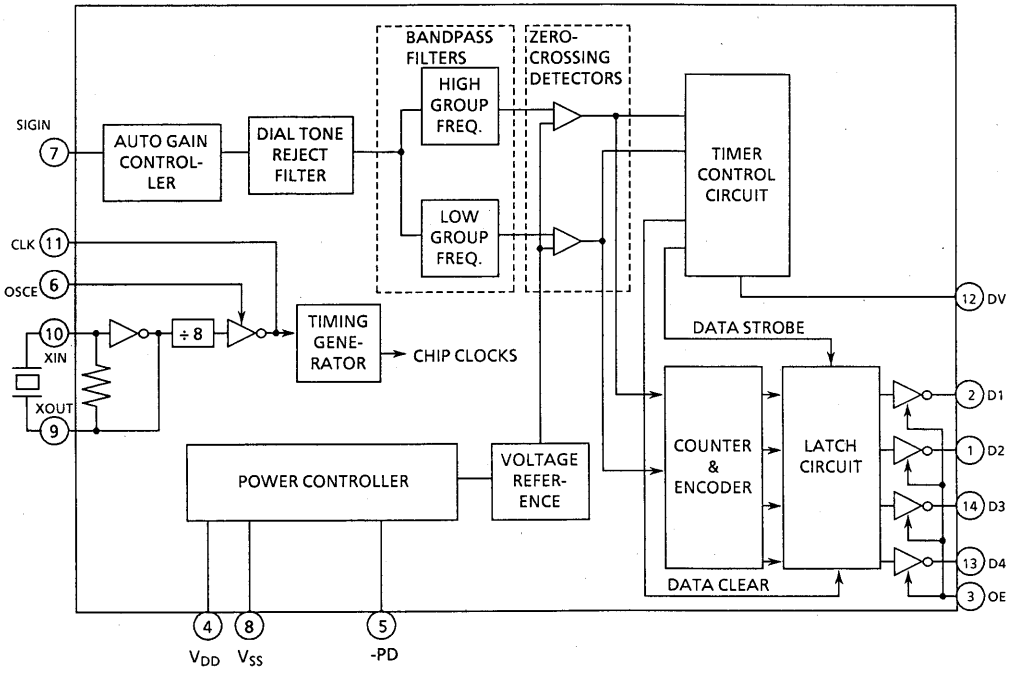
2. FEATURES

- ☐ Wide input dynamic range over 40dB
- ☐ Third tone tolerance under -16dB
- ☐ Zero stand-by power mode
- ☐ 4-bit hexadecimal code output
- ☐ 3-stats data output
- ☐ 3.58MHz crystal oscillator or ceramic resonator
- ☐ CMOS low power
- ☐ +5V single power supply
- ☐ 14-Pin DIP TC35304P
  14-Pin SOP TC35304F

2.1 APPLICATIONS

- ☐ PABX
- ☐ Automatic Answering Telephone
- ☐ Remote Controller

3. TC35304P / F INTERNAL BLOCK DIAGRAM



4. DESCRIPTION OF PIN FUNCTION

NO.	PIN NAME	I/O	PIN FUNCTION
2	D1	O	Output terminal of receiving data.
1	D2	O	
14	D3	O	At OE = "L"; High impedance
13	D4	O	At OE = "H"; Data Output
3	OE	I	3-state control terminal of D1- D4. OE = "H"; Enable OE = "L"; High impedance
4	VDD	V	Power supply terminal + 5V
5	– PD	I	– PD = "L"; Zero stand-by power mode is performed
6	OSCE	I	Oscillator Enable
7	SIGIN	I	Signal-input terminal.
8	VSS	G	Power supply terminal GND.
9	XOUT	O	Connect oscillator of 3.579545MHz.
10	XIN	I	Connect oscillator of 3.579545MHz. Connect to VDD at external clock mode.
11	CLK	I/O	OSCE = "H"; Clock frequency output. OSCE = "L" ; Clock frequency input.
12	DV	O	When a valid DTMF tone-pare is detected continuously for specified time, the level becomes high.

5. FUNCTIONAL DESCRIPTION

5.1 DESCRIPTION OF CIRCUIT CONSTRUCTION AND OPERATION

TC35304P/F consist of Low and High group band pass filters which correspond to the frequency bands used in DTMF signal. The logic circuit verifies the frequency and duration of the received tone to encode into the corresponding binary data.

The outline of each operation is described in the followings.

a) Band Pass Filter and Zero-crossing Detector Circuit

The band pass filter section is composed of high-accuracy switched capacitor filters and an auto gain controller in the first stage.The auto gain controller compresses the input signal, and consequently provides a wide input dynamic range.

The first stage of the switched capacitor filters is a dial tone rejection filter where sufficiently dissipates the frequency components of 350Hz to 440Hz due to suppress error detection.

Removing unnecessary signal components, furthermore, the signal is applied to the high and low group band pass filters. Each filter output is followed by a zero-crossing detector with hysteresis. When each signal amplitude at the output exceeds specified level, the signal is transformed into a full rail logic signal.

b) Decision Circuit and Timer Controlling Circuit

The signal judgment circuit decides that each transformed logic signal is a standard DTMF tone pair or not. When the signal frequency are in an effective range, a timer controlling circuit begins to measure the signal duration and prepares a corresponding 4-bit DTMF code. When the timer reaches the pre-fixed value, the code is transferred to the latch circuit. Then it makes the data valid (DV) output high . The timer controlling circuit also protects against the drop out of the valid signal . When the detected signal is not a DTMF signal or an absence of signal , DV keeps low.

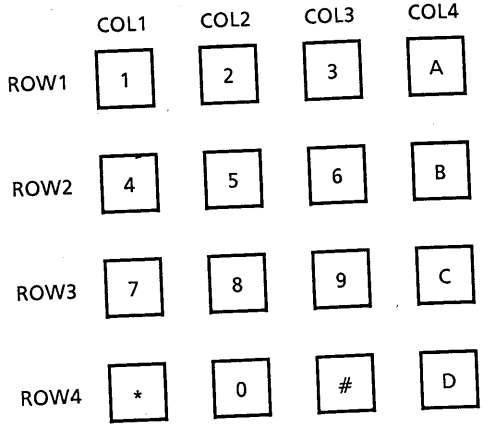
The last DTMF tone pair code remains in D1-D4 outputs, even if the input signal is gone and the DV output becomes low.

5.2 DTMF TO BINARY DECODING (HEXADECIMAL)

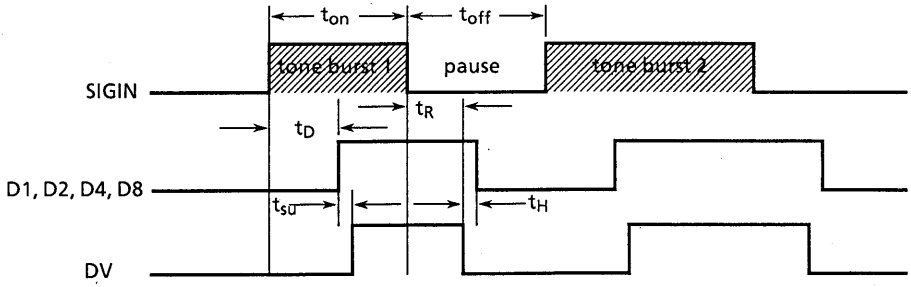
fL	fH	DIGIT	OE	L (HEXADECIMAL)			
				D4	D3	D2	D1
697	1209	1	H	L	L	L	H
697	1336	2	H	L	L	H	L
697	1477	3	H	L	L	H	H
770	1209	4	H	L	H	L	L
770	1336	5	H	L	H	L	H
770	1477	6	H	L	H	H	L
852	1209	7	H	L	H	H	H
852	1336	8	H	H	L	L	L
852	1477	9	H	H	L	L	H
941	1336	0	H	H	L	H	L
941	1209	*	H	H	L	H	H
941	1477	#	H	H	H	L	L
697	1633	A	H	H	H	L	H
770	1633	B	H	H	H	H	L
852	1633	C	H	H	H	H	H
941	1633	D	H	L	L	L	L
–	–	ANY	L	Z	Z	Z	Z

"Z" means high impedance.

5.3 DTMF DIALING MATRIX



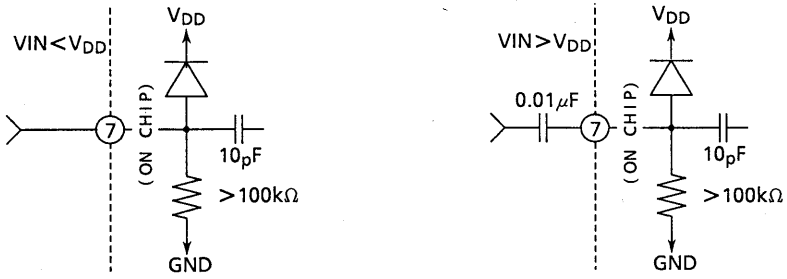
5.4 TIMING CHART



5.5 SIGIN

a) Input Signal Level

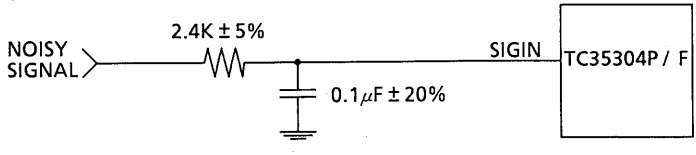
The SIGIN input is an analog pin. This pin is internally AC coupled. When an input signal exceeds the positive supply VDD, the input should be externally AC coupled. Proper input coupling is illustrated below.



The TC35304P/F is designed to operate normally, when accept sinusoidal input wave forms. Furthermore it will still operate satisfactorily with any input that has harmonics less than −16 dB below the fundamental.

b) Analog Input Noise

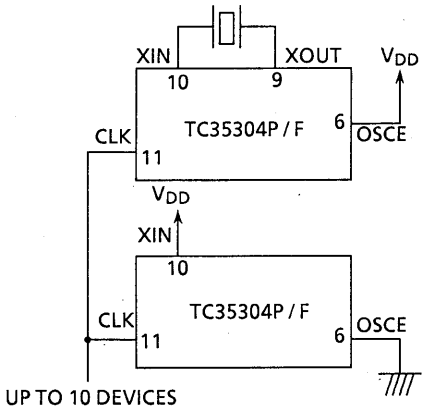
The TC35304P/F will tolerate total input noise up to 12dB below the lowest amplitude tone. For most telephone applications, the combination of the high frequency attenuation of the telephone line and internal band pass filters make special circuitry at the input to the TC35304P/F unnecessary. However, noise near the 37kHz internal switched capacitor filter sampling frequency will be aliased into the voice band, so the simple RC filter as shown below may be employed to band limit the incoming signal.



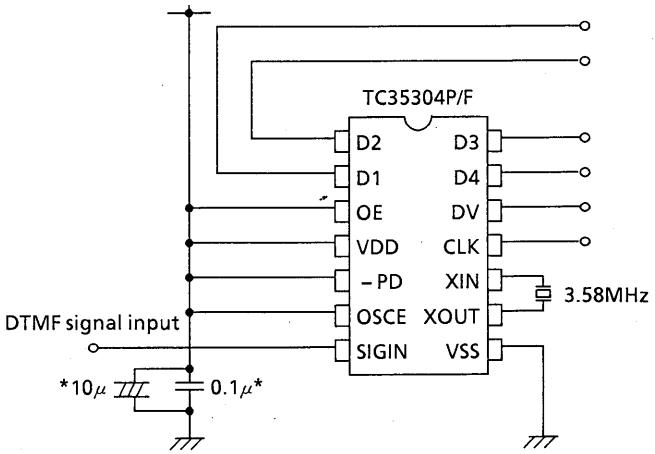
Filter for use in high frequency input noise environment.

5.6 CRYSTAL OSCILLATOR

The TC35304P/F contains an on-chip inverter which keeps stable oscillation when connected to a 3.58MHz crystal or a ceramic resonator. The oscillator is enabled by tying OCSE high. The crystal or resonator is connected between XIN and XOUT. When the OCSE pin is high , the CLK pin is a clock frequency output pin and provides other TC35304P/F with the same frequency reference by tying their CLK pins to the CLK pin of the source device. XIN and OCSE of the auxiliary devices must then be pull up and down respectively. When the OCSE pin is low , the CLK pin is a clock frequency input pin. Ten devices may run off a single oscillator-connected TC35304P/F as shown below.



5.7 TEST CIRCUIT



* The performance of TC35304P/F can be optimized by keeping noise on the supply rails to minimum. The decoupling 0.1uF capacitor should be connected close to the device.

6 ELECTRICAL CHARACTERISTICS

6.1 MAXIMUM RATINGS

Ta = 25°C

ITEM	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{DD}	V_{SS} – 0.5 to V_{SS} + 7.0	V
Input Voltage	V_{IN}	V_{SS} – 0.5 to V_{DD} + 0.5	V
Input Current	I_{IN}	– 10 to + 10	mA
Output Voltage	V_{OUT}	V_{SS} – 0.5 to V_{DD} + 0.5	V
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	– 60 to + 150	°C
Operating Temperature	T_{opr}	– 40 to + 85	°C

6.2 DC ELECTRICAL CHARACTERISTICS

Ta = 25°C, V_{DD} = 5V ± 10%, V_{SS} = 0V

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.**	MAX.	UNIT
Operating Voltage	V_{DD}					
Operating Supply Current	I_{DD} (opr)	– PD = 5.0V		3.0	7.0	mA
Static Supply Current	I_{DD} (Stby)	– PD = 0V		0.01	10.0	μA
High Level Input Voltage	V_{IH}		3.5			V
Low Level Input Voltage	V_{IL}				1.5	V
High level Output Current	I_{OH}	V_{OUT} = 4.6V (Except for X_{OUT})	0.4	0.8		mA
		V_{OUT} = 4.6V (X_{OUT})	0.1	0.2		mA
Low level Output Current	I_{OL}	V_{OUT} = 0.4V (Except for X_{OUT})	1.0	2.5		mA
		V_{OUT} = 0.4V (X_{OUT})	0.25	0.5		mA
High Level Input Current	I_{IH}	V_{IN} = 5.0V			0.1	μA
Low Level Input Current	I_{IL}	V_{IN} = 0V			0.1	μA
Input Impedance (SIGIN)	Z_{IN}	$V_{DD} \geqq V_{IN} \geqq V_{DD}$ – 10V	100kΩ			kΩ

** Typical figures are at 25°C and for design aid only : not guaranteed and not subjected to production testing.

6.3 AC ELECTRICAL CHARACTERISTICS

$Ta = 25°C$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, $f_{CLK} = 3.57954MHz$

ITEM	SYMBOL	TEST CONDITION	MIN.	TYP.**	MAX.	UNIT
Input Signal Level for Reception		Each Tone Composite Signal	−42	−47	−2	dBm*1
Tone Amplitude Ratio	t_{wist}	twist = high tone / Low tone	−10		+10	dB
Frequency Deviation Tone Reception			±1.5 ±2Hz	±2.3		%
Frequency Deviation Tone Rejection			±3.5			%
Third Tone Rejection Ratio				−16		%
Dial Tone Rejection Ratio		350~440Hz		+22		dB
Noise Rejection Ratio		0~3.4kHz		−12		dB
Tone Time for Detection	t_{ON}	Refer to Test Circuit	50			ms
Tone Time for Rejection	t_{ON}				20	ms
Pause Time for Detection	t_{OFF}		50			ms
Pause Time for Rejection	t_{OFF}				20	ms
Detect Time	t_D		25		40	ms
Release Time	t_R		35.5		43.5	ms
Data Hold Time	t_H		4.4		5.1	ms
Data Set-up Time	t_{SU}		7			μs
Output Enable Time		10kΩ // 50pF		50	60	ns
Output Disable Time		10kΩ // 50pF		300		ns
Clock Duty Cycle			40		60	%
Clock Frequency	f_{CLK}	X_{IN}	3.5759	3.5795	3.5831	MHz
Capacitive Load	CLX	X_{OUT}			30	pF
Power Supply Noise		Wide Band			10	mV_{p-p}

* dBm = decibels above or be low a reference power of 1mW into a 600ΩdBm load.

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