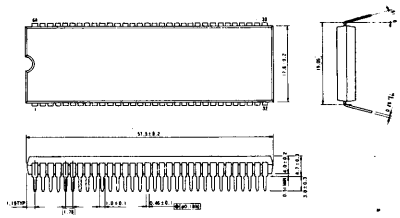
∘ DIGITAL AUDIO SIGNAL PROCESSOR (ASP-I)

Unit in mm



Package width and length do not include mold protrusion.
All owable mold protrusion is 0.15mm.

JEDEC	–
TOSHIBA	SDIP64-P-750

The TC9330N is an audio use single chip Digital Signal Processor for the sound field control. Digital delay of 'High quality and high precision' which is infeasible by the analog approach, and the high through put which realizes the simultaneous Performance of read/write the data and Multiplying/accumulation operations can simulate the various AV Digital sorround. More over convolution arithmetic/logic operations the early sound reflections and arithmetic/logic operation on reverberated sound can simulate the natural reverberation for the various Halls, Stages, Stadiums, and so on.

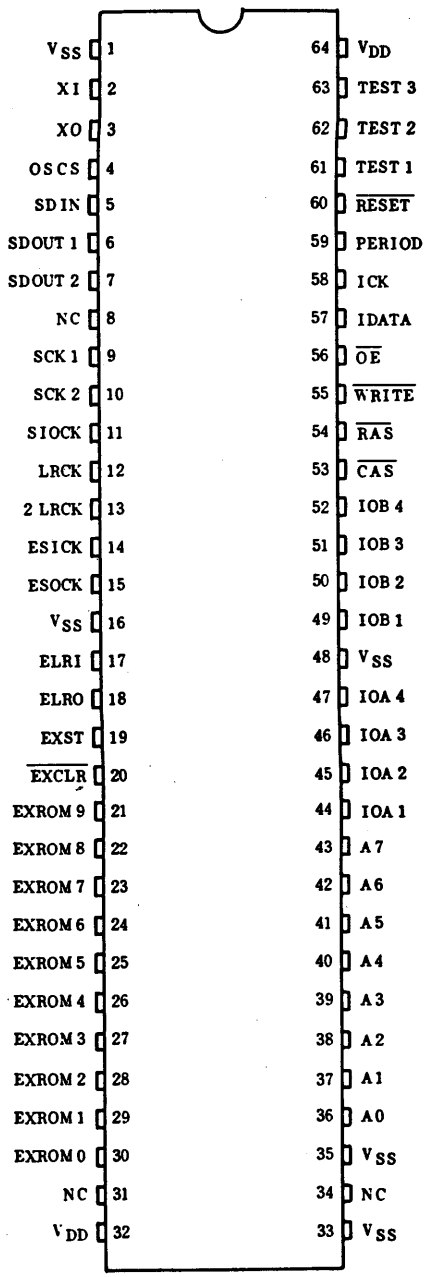
- Direct-coupled with 1 or 2 DRAM (64k×4bits)
- Various digital delay with the external RAM as multiple Ring Buffer (Offset RAM: 14bits ×32words)
- Parallel performance of 'Read/write' and 'multiply/accumulation operation
  - Multiplier (16bits×12bits→24bits)
  - Accumulator (26bits, load expansion 2bits)
  - Coefficiency RAM (12bits×32words)
- 1 or 2 program can be built-in
  Sequence program ROM 39bits ×128step (64step/program)
- Internal parameter, mode, and program can be set up by the CPU etc. with 3 lined serial interface
- Control timing signal for ADC and DAC
- I^2R digital filter operation
- 2 μ CMOS process realizes low power dissipation
- 5V SUM-1 power supply

MAXIMUM RATINGS (Ta=25℃)

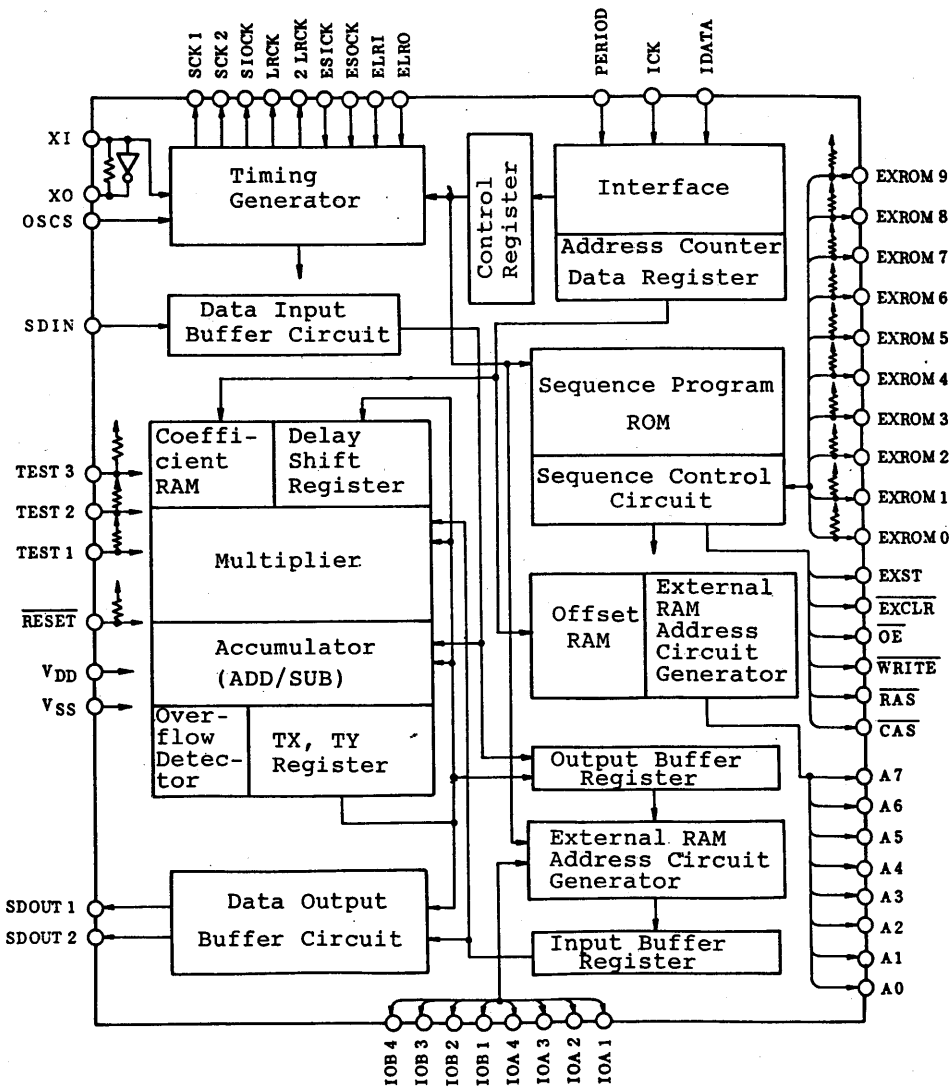
CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	VDD	-0.3～ 6.0	V
Input Voltage	VIN	-0.3～VDD-0.3	V
Input Protection Diode Current	IIK	±10	mA
Output Protection Diode Current	IOK	±10	mA
Power Dissipation	PD	300	mW
Operating Temparature	Topr	-20～75	℃
Storage Temparature	Tstg	-40～125	℃

PIN ASSIGNMENT

TOP VIEW Shrink DIP-64 pin



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (1) (Unless otherwise specified, Ta =25 ℃, VDD=5V)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage		VDD	-			4.5	5.0	5.5	V
Operating Supply Current		IDD	-	CI=100pF, VIN=4V f=13MHz, Square Wave, OSCS="L"			16.0	25.0	mA
Input Voltage (1)	"H" Level	VP	-	IDATA, PERIOD, ICK, SDIN, ESICK,			3.0		V
	"L" Level	VN	-	ESOCK, ELRI, ELRO			2.3		
Input Voltage (2)	"H" Level	VIH	-	Input terminal except for the		3.5		VDD	
	"L" Level	VIL	-	above mentioned and for XI		0		1.0	
Input Current	"H" Level	IIH	-	Except EXROM0 ~9,	VIH=5.0V			1.0	μA
	"L" Level	IIL	-	TEST1 ~3, $\overline{\text{RESET}}$	VIL=0V	-1.0			
Tristate Leak Current	"H" Level	ITLH	-	IOA1 ~4	VIH=5.0V			1.0	
	"L" Level	ITLL	-	IOB1 ~4	VIL=0V	-1.0			
Output Current (1)	"H" Level	IOH1	-	Except	VOH=4.5V		-3.5	-2.0	mA
	"L" level	IOL1	-	EXROM0~7, XI	VOL=0.5V	4.2	7.0		
Output Current (2)	"H" Level	IOH2	-	EXROM0~7	VOH=4.5V		-6.0	-4.0	
	"L" Level	IOL2	-		VOL=0.5V	8.0	13.5		
Ouput Current (3)	"H" Level	IOH3	-	XO (XI=L)		-	-6.2	-3.8	
	"L" Level	IOL3	-	XO (XI=H)		5.8	9.5	-	
Input Clock Amplitude		VCK	-	XI, CI=100pF		2.0		4.0	VP-P
Input Resistance/ Input Ouput Resistance		Rup	-	RESET, TEST1~3, EXROM0 ~9 VIN=0V		70		220	kΩ
Feed Backing Resistance		RFB	-	VIN=0V		30	50	70	

ELECTRICAL CHARACTERISTICS (2) (Unless otherwise specified, Ta=-20 ~75℃, VDD=4.5~ 5.5V, CL=15pF)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Frequency	f opr1	-	OSCS="H"	14.0		26.0	MHz
	f opr2	-	OSCS="L"	7.0		13.0	MHz
Rising & Trailing Time	tr1	-	$\overline{RAS}$, $\overline{CAS}$, $\overline{OE}$, $\overline{WRITE}$			20	ns
	tf1	-	CL=20pF			20	ns
	tr2	-	A0~A7, IOA1~4 , IOB1~4			15	ns
	tf2	-	CL=15pF			15	ns
	tr3	-	Output terminal except for the			15	ns
	tf3	-	above mentioned, CL=15pF			15	ns
Transfering Time	t pLH(1)	-	OSCS="L"		25	35	ns
	t pHL(1)	-	OSCS="L"		25	35	ns
	t pK1(1)	-	OSCS="H"		20	30	ns
	t pK1(2)	-	OSCS="H"		20	30	ns
	t pK2(1)	-	OSCS="H"		25	40	ns
			OSCS="L"		25	40	
	t pK2(2)	-	OSCS="H"		25	40	ns
			OSCS="L"		25	40	
	t pSO(1)	-				25	ns
	t pSO(2)	-				(※)	ns
	t p2LR(1)	-				10	ns
	t p2LR(2)	-				10	ns
	t pLR(1)	-				15	ns
	t pLR(2)	-				15	ns
SDIN Data Input Set Up Time	t set	-		0			ns
SDIN Data Input Holding Time	t hold	-		0			ns

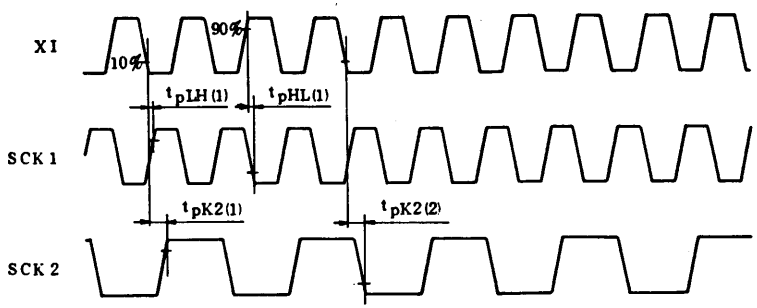
※ 1/f opr2×1.5

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Read/Write Cycle Time	t RC	-	f opr2=13MHz		310		ns
$\overline{RAS}$ Pre-charging Time	t RP	-	f opr2=13MHz		155		ns
$\overline{RAS}$ Pulse Width	t RAS	-	f opr2=13MHz	150	154		ns
$\overline{RAS}$ Holding Time	t RSH	-	f opr2=13MHz	75	77		ns
$\overline{CAS}$ Holding Time	t CSH	-	f opr2=13MHz		230		ns
$\overline{CAS}$ Pulse Width	t CAS	-	f opr2=13MHz		155		ns
$\overline{CAS}$-$\overline{RAS}$ Pre-Charging Time	t CRP	-	f opr2=13MHz		80		ns
Low Address Set Up Time	t ASR	-	f opr2=13MHz		80		ns
Low Address Holding Time	t RAH	-	f opr2=13MHz		40		ns
Column Address Set Up Time	t ASC	-	f opr2=13MHz		40		ns
Column Address Holding Time	t CAH	-	f opr2=13MHz		190		ns
Write Command Holding Time	t WCH	-	f opr2=13MHz		80		ns
Write Command Pulse Width	t WP	-	f opr2=13MHz		155		ns
Data Input Holding Time	t DH	-	f opr2=13MHz		80		ns
Data Input Set Up Time	t DS	-	f opr2=13MHz		80		ns
$\overline{OE}$-$\overline{RAS}$ Delay Time	t ORD	-	f opr2=13MHz		80		ns
$\overline{CAS}$-$\overline{RAS}$ Delay Time	t COD	-	f opr2=13MHz		80		ns
Stand-by Time	t 1	-		1.0			μs
$\overline{RESET}$ Pulse Width	t 2	-		1.0			μs
$\overline{RESET}$-PERIOD Delay Time	t 3	-		1.0			μs
Start Pulse Set Up Time	t 4	-		0.2			μs
ICK Low Level Width	t 5	-		1.0			μs
ICK High Level Width	t 6	-		1.0			μs
Start Pulse Holding Time	t 7	-		0.2			μs
IDATA Set Up Time	t 8	-		0.2			μs
PERIOD-ICK Delay Time	t 9	-		0.2			μs
ICK-PERIOD Delay Time	t 10	-		1.0			μs
End Pulse Width	t 11	-		1.0			μs

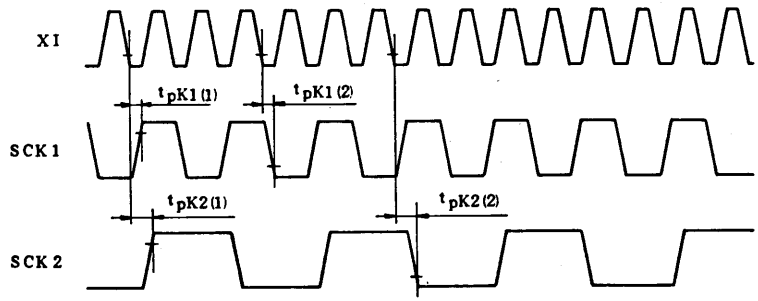
AC CHARACTERISTICS TESTING

(1) Clock Terminal (XI, SCK1, SCK2)

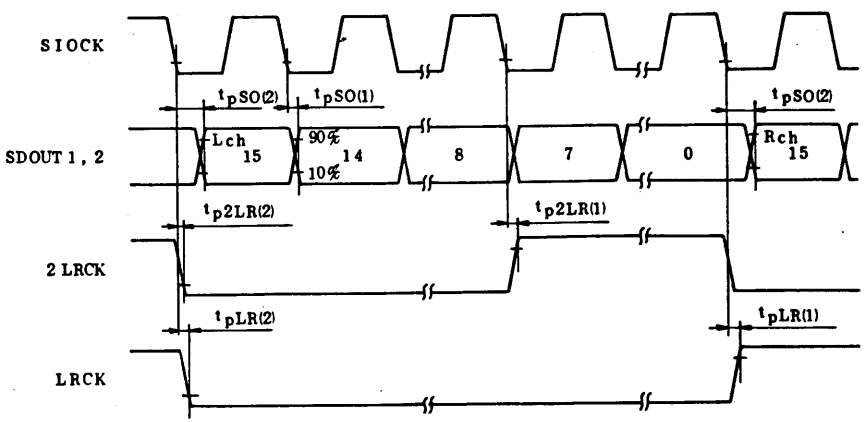
[OSCS = L]



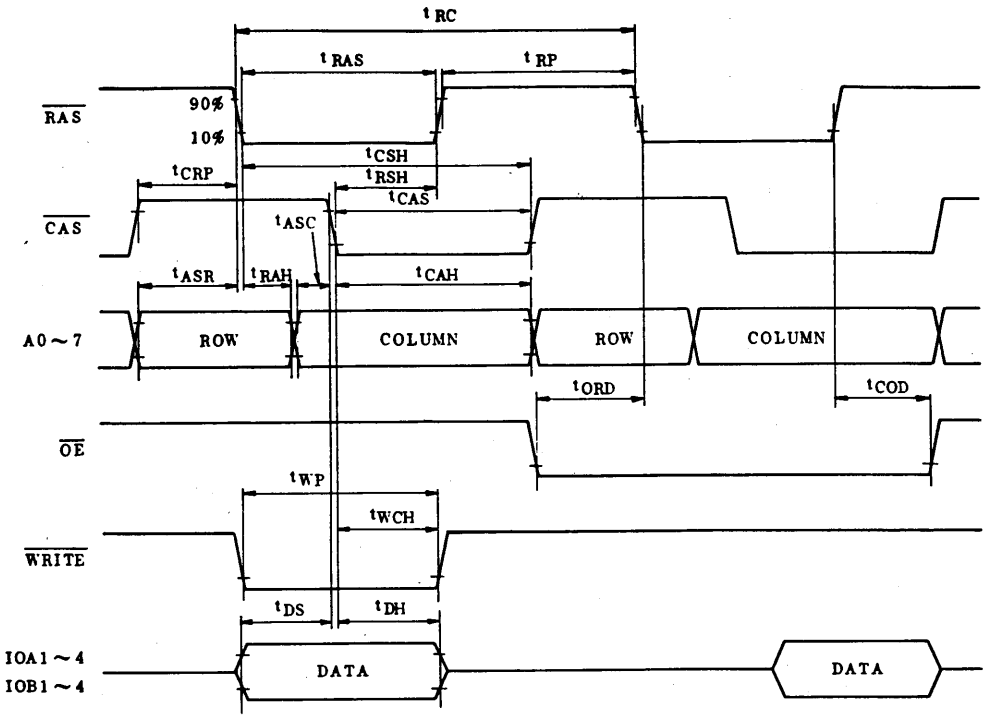
[OSCS = H]



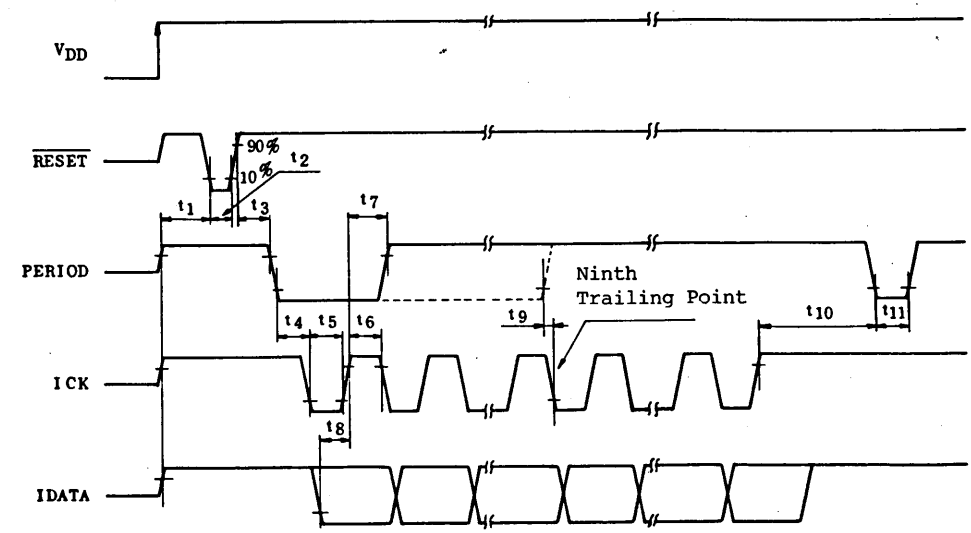
(2) Data Output (SIOCK, SDOUT1, SDOUT2, 2LRCK , LRCK)



(3) .External RAM Control Terminal ($\overline{RAS}$, $\overline{CAS}$, $\overline{OE}$, $\overline{WRITE}$, A0 ~7, IOA/B1 ~4)



(4) I/F Input (PERIOD, ICK, IDATA, $\overline{RESET}$)



TERMINAL LIST

PIN NO.	SYMBOL	I/O	FUNCTION	NOTE
1	VSS	-	GND	
2	XI	I	X'tal connection or external clock input (XI). Bulit-in feedbacking resistor.	
3	XO	O		
4	OSCS	I	Oscilator/external clock deviding terminal.	
5	SDIN	I	Lch, Rch Serial data input.	Schmitt input
6	SDOUT1	O	Lch, Rch Serial data output.	
7	SDOUT2	O		
8	NC	-	Non connection.	
9	SCK1	O	OSCS="L": XI clock Buffer output OSCS="H": XI clock 1/2 devided output	
10	SCK2	O	OSCS="L": XI clock 1/4 devided output OSCS="H": XI clock 1/4 devided output	
11	SIOCK	O	Data shift clock output for ADC, DAC.	Internal generation Mode
12	LRCK	O	Channel clock output for ADC, DAC.	Ditto
13	2LRCK	O	Clock with 2 times frequency of LRCK.	Ditto
14	ESICK	I	Shift clock input for Lch, Rch serial input data.	External input Mode Schmitt input
15	ESOCK	I	Shift clock input for Lch, Rch serial output data.	Ditto
16	VSS	-	GND	
17	ELRI	I	Channel clock input for Lch, Rch serial input data.	External input Mode Schmitt input
18	ELRO	O	Channel clock input for Lch, Rch serial output data.	Ditto
19	EXST	O	Program sequence ROM starting pulse output.	External ROM Mode
20	$\overline{\text{EXCLR}}$	O	System clear signal output.	
21	EXROM9	I	External ROM data input. Built-in pull up resistor.	Ditto
22	EXROM8	I		

PIN NO.	SYMBOL	I/O	FUNCTION	NOTE
23 ~ 30	EXROM7 ~ EXROM0	I/O	External ROM input terminal. Output terminal at test. Built-in pull up resistor.	External ROM Mode
31	NC	-	Non connection.	
32	VDD	-	Power terminal.	
33	VSS	-	GND	
34	NC	-	Non connection.	
35	VSS	-	GND	
36 ~ 43	A0 ~ A7	O	Address output for external DRAM.	
44 ~ 47 49 ~ 52	IOA1 ~ IOA4 IOB1 ~ IOB4	I/O	Data input/output for external DRAM. 4 times acceess mode: IOA1~IOA4 only.	
48	VSS	-	GND	
53	$\overline{CAS}$	O	Column Address strobing output for external DRAM.	
54	$\overline{RAS}$	O	Low Address strobing output for external DRAM.	
55	$\overline{WRITE}$	O	Read/write pulse output for external DRAM.	
56	$\overline{OE}$	O		
57	IDATA	I	Interface Data input.	Schmitt input
58	ICK	I	Interface clock input.	Ditto
59	PERIOD	I	Interface period pulse input.	Ditto
60	$\overline{RESET}$	I	Reset signal input. Built-in pull up resistor.	
61 ~ 63	TEST1 ~ TEST3	I	Test terminal. Usually "H" or open. Built-in pull up resistor.	
64	VDD	-	Poewr terminal.	

[1] Timing Generator

(1) X'tal connection

The clock for LSI internal is generated by the following.

- X'tal, capacitors connected as shown in Fig. 1.
- External clock input to terminal 'XI'.

And the frequency is to be determined with the terminal 'OSCS'.

<EXAMPLE OF fx'tal>

MODE	SAMPLING	OSCS="L"	OSCS="H"
CD	44.1kHz	11.2896MHz	22.5792MHz
DAT	32 kHz	8.192 MHz	16.384 MHz
	48 kHz	12.288 MHz	24.576 MHz

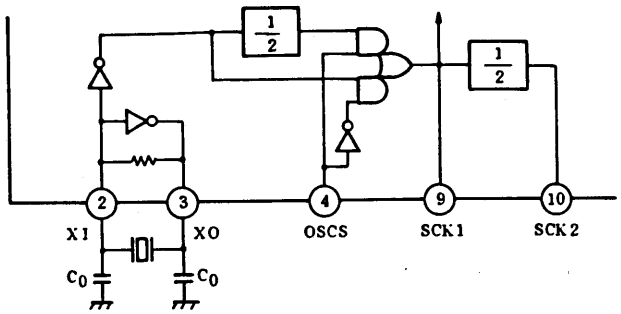


Fig. 1

X'tal is to be of low CI value and good starting characteristics.

(2) Channel clock, data shift clock for data input/output

- Internal generation mode and extenal input mode for channel clock for 16bit serial data input/output (LRCK, ELRO, ELRI) and Data shift clock (SIOCK, ESICK, ESOCK).
- And the Mode is set up with the interface (control data).

CONTROL DATA		CHANNEL CLOCK/SHIFT CLOCK			
SISEL	SOSEL	For Data Input		For Data Output	
1	1	Internal generation	LRCK/SIOCK	Internal generation	LRCK/SIOCK
1	0	Internal generation	LRCK/SIOCK	External input	ELRO/ESOCK
0	1	External input	ELRI/ESICK	Internal generation	LRCK/SIOCK
0	0	External input	ELRI/ESICK	External input	ELRO/ESOCK

(2LRCK : double velocity LRCK clock output)

[2] Data Input/Data Output

- Input/output data is of 2's compliment Representation and MSB first, 16bit serial data (L, R-altanative input/output).
- SDIN for 16bits serial data input port. Fig. 2 shows the timing.
- SDOUT1, SDOUT2 for 16bits serial data output port. This LSI can generate 2 kinds of operation data (ex. forward/backward reflection). Fig. 3 shows the timing.

[3] Sequence Controller

(1) Sequence program ROM

- Program ROM is composed of siquence Bit of 39bits and program step of 128 step.
- Usable 64 step per a sampling (32 step/ch). The ROM can stores two kinds of program.
- The program selection is to be performed with the interface (Control data: PSEL).

PSEL=0→Program A	PSEL=1→Program B

(2) Sequence controller

- Parallel performance of the read/write and multiply/accumulation operation by the 39bit Sequence Bit.
- The 'END' signal in the Sequence Bit reset the sequence counter to the initial state, and stop the program. Program is to be started at the rising or trailing edge of the channel clock. The starting edge is determined with the interface (Control data: LEN, REN).
- The following 5 commands are prepared.
  ① Operational processing (2 step)
  ② External RAM Read/Write Processing (2 step: 2DRAM Application, 4 step: 1DRAM Application)
  ③ Delay shift registor Load Processing (1 step)
  ④ Data output processing (1 step)
  ⑤ Program stop processing (1 step)

CONTROL DATA		PROGRAM START MODE
LEN	REN	(Channel clock edge)
1	0	Trailing edge
0	1	Rising edge
1	1	Start at trailing/rising edge

[4] External RAM Address Signal Generator

- Offset Write Address and Offset Read Address are generated to treat the external RAM as multiple Rising Buffer.
- 1 or 2 external DRAM can be direct-coupled.
- 14bits offset is written into the Offset RAM with the interface.
- Offset RAM constructure is of 14bits×32words, and the offset of "0" is required from the first, so Max. 31 offset value can be set up altogether the Read/Write offset. And 8bit Refreshing Counter refreshs external DRAM at the beggining of each Lch and Rch signal processing.

[5] External RAM I/O Controller

- The data for the external RAM is of 16bits, the Access Mode is to be 4-times in case of 1DRAM or to be 2-times in case of 2 DRAM.
- Each of SDIN (Serial input) data and operational data is to be of the data for the external RAM.

[6] Operational Circuit

- Operational Circuit is compose of followings.
  - Coefficiency RAM (12bits×32words)
  - Delay registor
  - Multiplier (16bits×12bits→24bits)
  - Accumulator (26bits: expansion by 26bits)
  - Temporary registor (TX, TY: 26bits)
  - Overflow detector
- Coefficiency RAM→Multiplier→Accumulator →Temporary registor (TX, TY←A ×B +C) operation requires for 2 step of sequence step.

[7] Interface Circuit

- Interface is composed of 3 lined Serial Bus.
- All of 3 lines are to be "H" at the idle state.
- 'IDATA' should be recieved at ICK using timing.
- Each of 'Control data', 'Write address of offset data', 'Offset data', and 'Coefficient data' has an identifying code.

(1) I/F data

IDENTIFYING CODE	D A T A	BIT-TRANSFERING
80H	Control Data	8
81H	Offset/Coefficiency RAM Write Address	8
82H	Offset Read/Write Data	16
83H	Coefficiency Data	16

(2)Data description

① Control Data

Control data is 7bit from LSB of transfering 8bit.

	LSB 0	1	2	3	4	5	6	MSB 7
SYMBOL	2/4	REN	LEN	SOSEL	SISEL	SCLR	PSEL	×
0	DRAM 4 ACCESS	Start disable	Start disable	External input	External input	normal	Program -A	Dummy
1	DRAM 2 ACCESS	R edge start	L edge start	Internal generation	Internal generation	System clear	Program -B	

② Offset RAM, Coefficiency Write Address

Offset RAM and coefficient RAM have a write address in common. And the write address is 5bit from LSB of transfering 8bit.

S Y M B O L	EFFECTIVE BIT	DUMMY BIT
Offset/Coefficiency Write Address	LSB 0~4 bit	MSB 5~7 bit

③ Offset Read/Write Data

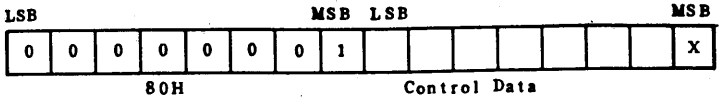
Offset Read/Write data is 14bit from MSB of transfering 16bit.

④ Coefficiency Data

Coefficiency data is 12bit from MSB but for 2bit of transfering 16bit.

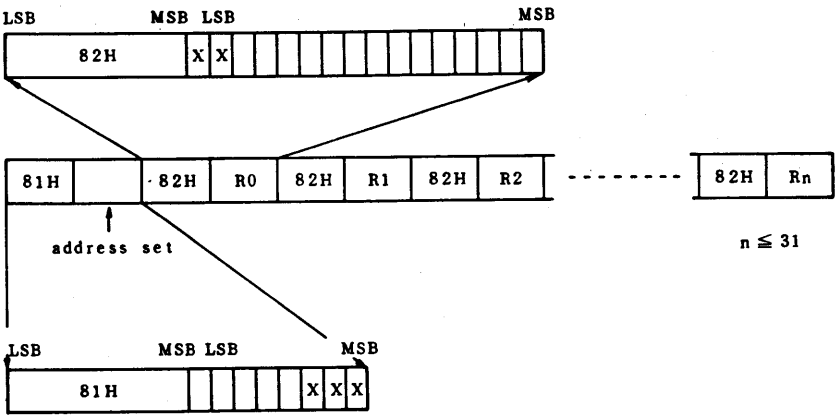
(3) Data setting

① Control Data Setting

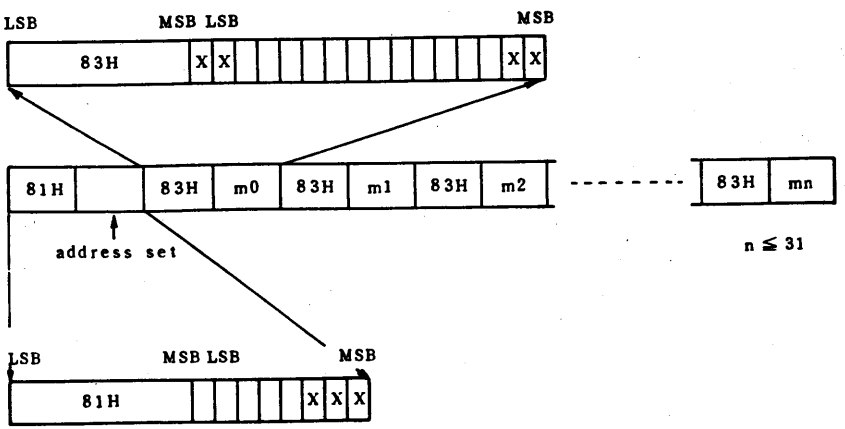


② Offset Data Setting

In case that the Write Address for the offset RAM is initially set up. (this is same in case of ③) the Address is incremented every time of transfering the offset data.

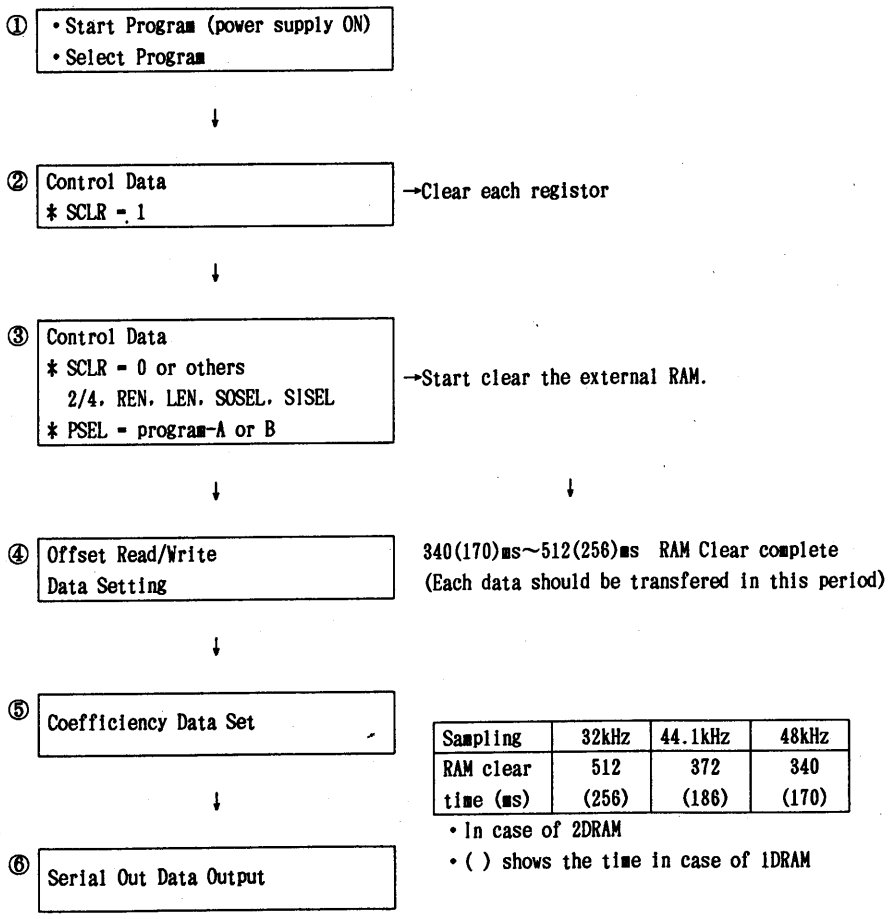


③ Coefficiency Data Setting



(4) Program staring, selection

- TC9330N can be provided with 2 programs, and the program is to be selected with the interface.
- Before set up or start the program, the data of each registor and external RAM should be cleared. The following is an external for transfering the control data.



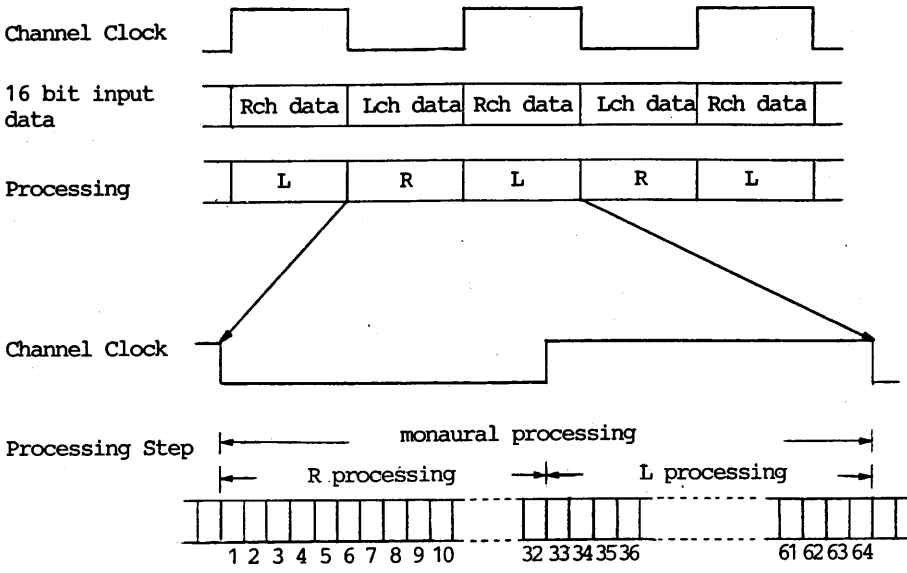
Sampling	32kHz	44.1kHz	48kHz
RAM clear time (ms)	512 (256)	372 (186)	340 (170)

- In case of 2DRAM
- ( ) shows the time in case of 1DRAM

(NOTE) ④, ⑤are replacable with each.

[8] Signal Processing Flow

• The following show the signal processing flow and signal processing example.



< Ex.: Early Sound Reflection Processing>

```
step 1    : DRAM Refresh
step 2, 3 : TX←m11 x RAMDATA (R11) + 0 ; Input REG ← RAMDATA (R10)
step 4, 5 : TX←m10 x RAMDATA (R10) + TX; Input REG ← RAMDATA (R 9)
step 6, 7 : TX←m 9 x RAMDATA (R 9) + TX; Input REG ← RAMDATA (R 8)
step 8, 9 : TX←m 8 x RAMDATA (R 8) + TX; Input REG ← RAMDATA (R 7)
    :
step 33   : DRAM Refresh
    :
step 64   : END ← 1
```

Serial Data Input Timing

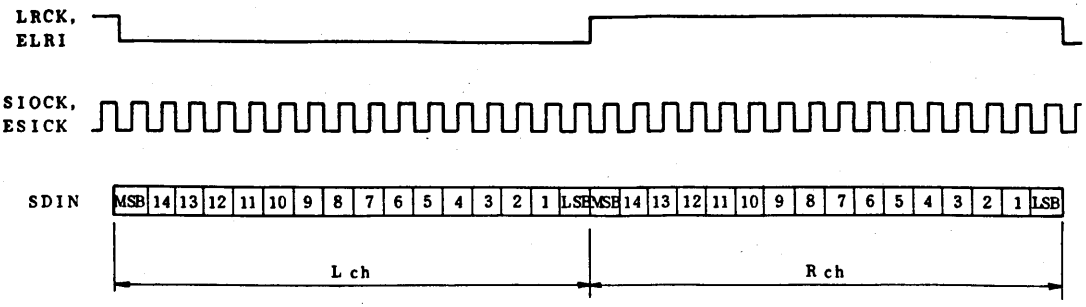


Fig. 2

Serial Data Output Timing

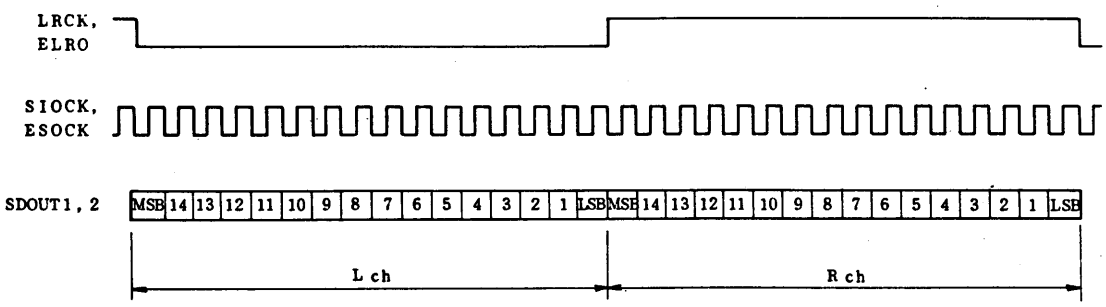


Fig. 3

Interface Input Timing

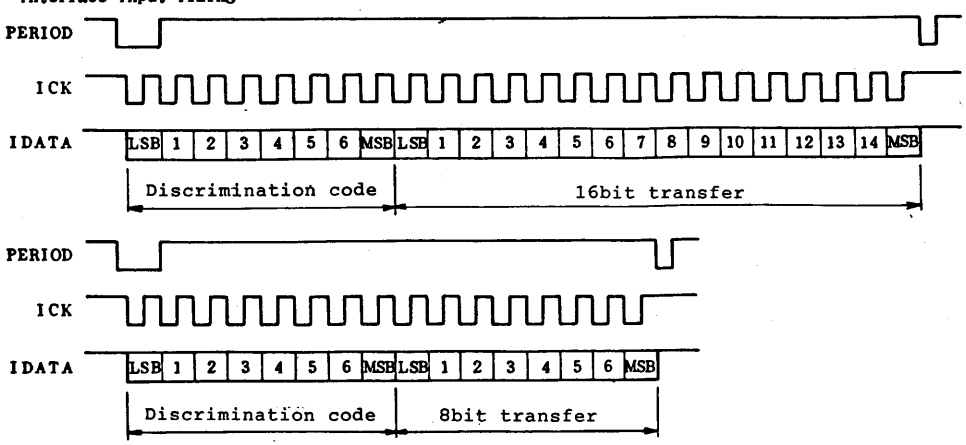
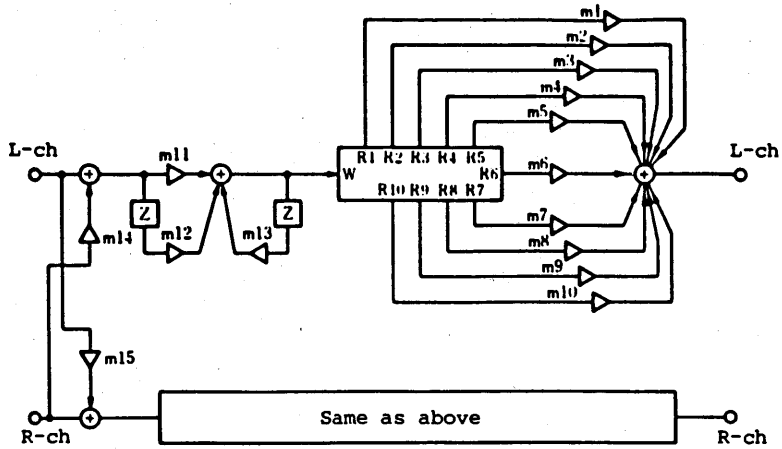


Fig. 4

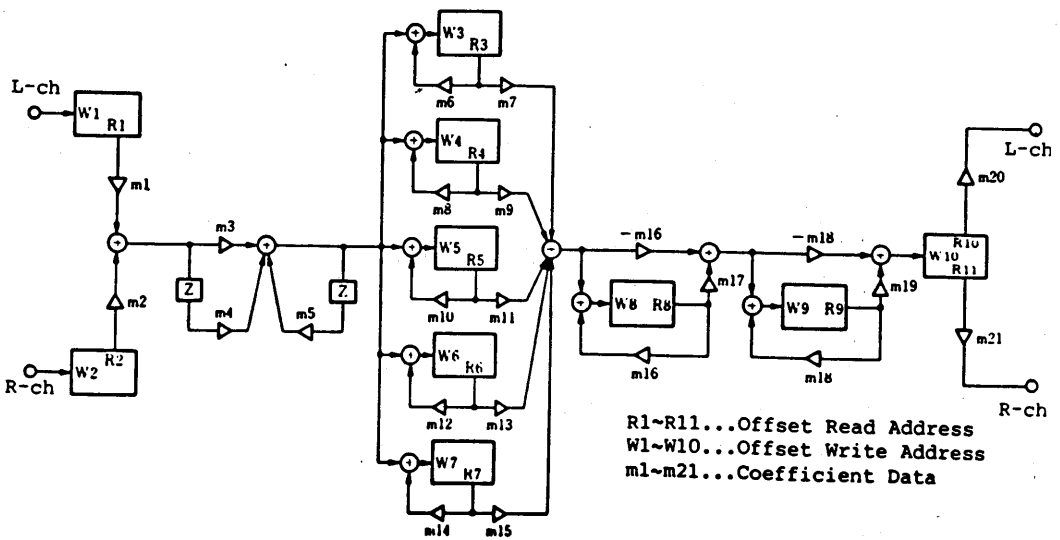
Example of Early Reflection Program



R1~R10...Offset Read Address
m1~m15...Coefficient Data

Fig. 5

Example of Reverberation Porgram



R1~R11...Offset Read Address
W1~W10...Offset Write Address
m1~m21...Coefficient Data

Fig. 6

Typical Configuration of Sound Feld Control Syste